New!

Model 5352

32-Channel DDC with Four 200 MHz, 16-bit A/Ds - 3U VPX

ReadyFlow Board Support Package

Features

- 32 channels of DDC in banks of 8 channels
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor with ruggedized and conduction-cooled versions available

General Information

Model 5352 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/Ds are supported by a high-performance 32-channel installed DDC (digital downconverter) IP Core, and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 5352 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 5352 SX95T FPGA employs an advanced FPGA-based digital down-converter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four attached A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting ranging from DC to f_s (f_s is the A/D sample rate).

Decimation and Filtering

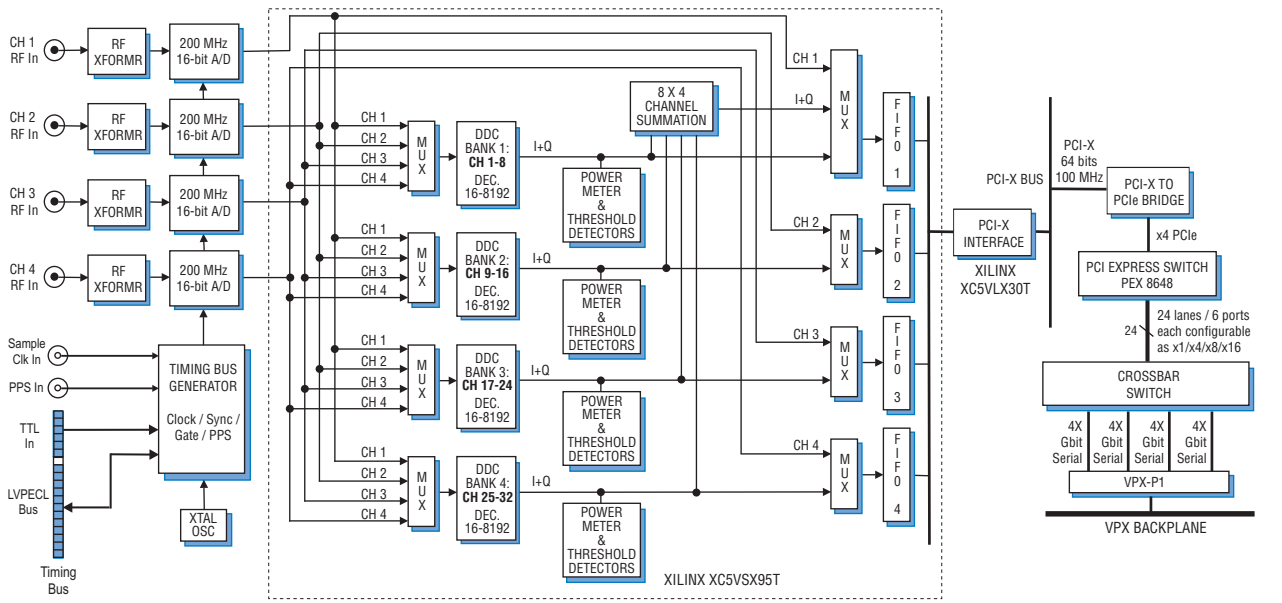
All of the eight channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have a unique decimation setting supporting up to four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. Rejection of adjacent-band components within the 80% bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 5352 features 32 power meters that continuously measure the individual average power output of each DDC channel. The time constant of the averaging interval is programmable up to 16 kilosamples. In addition, threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458

Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

Model 5352

32-Channel DDC with Four 200 MHz, 16-bit A/Ds - 3U VPX

Output Multiplexers and FIFOs

Four output MUXs in the SX95T FPGA can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application. Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 5352 architecture includes a flexible timing and synchronization circuit for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5352's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

Fabric-Transparent Crossbar Switch

The 5352 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5352 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Internal Clock: 200 MHz crystal osc.
External Clock: 10 to 200 MHz
Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T dedicated to digital downconverters and output
Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch
PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:
Forced-Air Cooled: 0° to 50° C std; -20° to 65° C (Level L2)
Conduction-Cooled: -40° to 70° C (Level L3)
Storage Temperature:
Forced-Air Cooled: -20° to 90° C std; -40° to 100° C (Level L1, L2)
Conduction-Cooled: -50° to 100° C (L3)
Relative Humidity: 0 to 95%, non-cond.; 0 to 100% with conformal coating

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5352	32-Channel DDC with four 200 MHz, 16-bit A/D s - 3U VPX
Options:	
-703	Level L3 Conduction-Cooled Version
-731	Two-slot heat sink

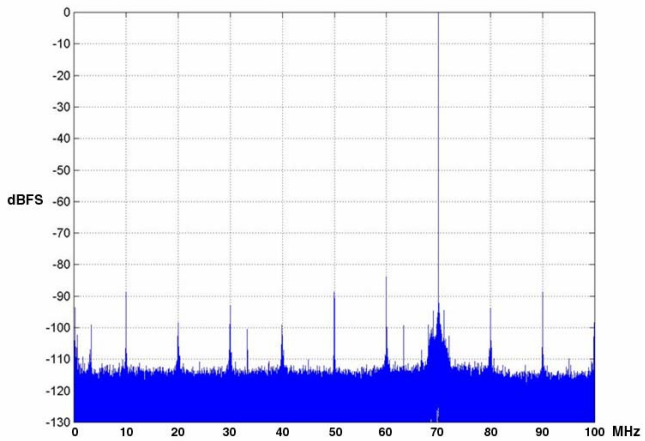
Contact Pentek for additional available options.

PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

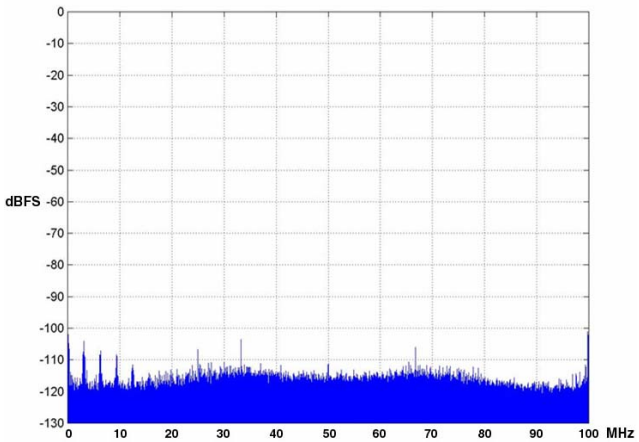
A/D Performance

Spurious-Free Dynamic Range



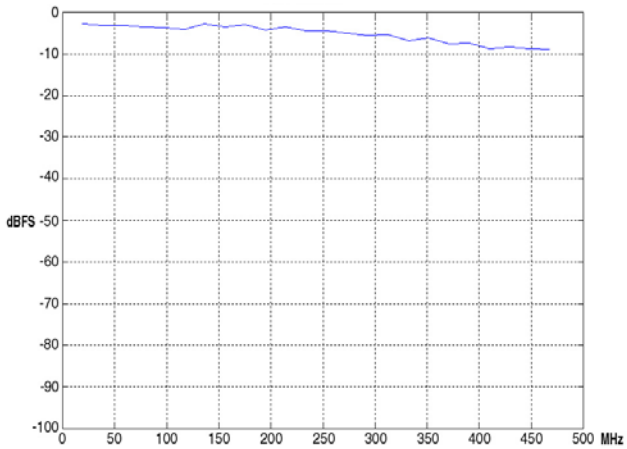
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



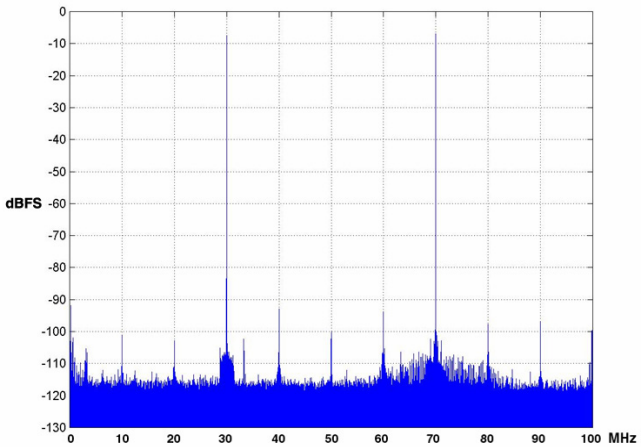
f_s= 200 MHz, Internal Clock

Input Frequency Response



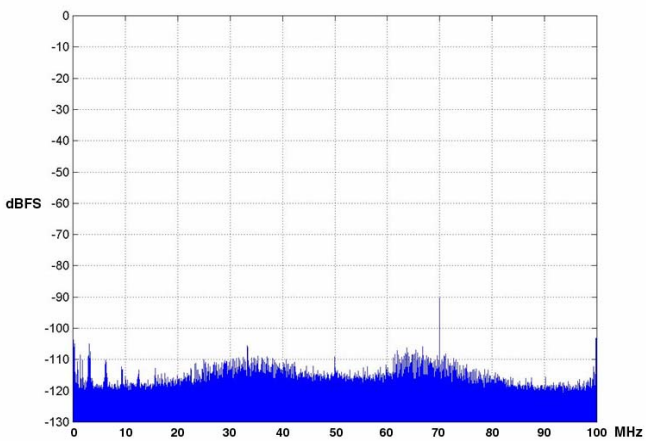
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



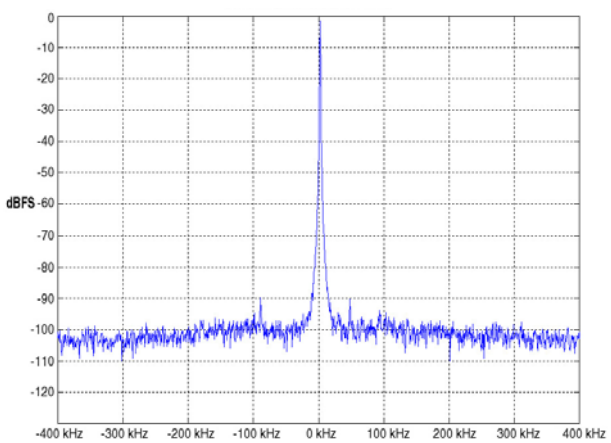
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock