New!

Model 5342

Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 125 MHz 14-bit A/Ds
- One digital upconverter
- One 500 MHz 16-bit D/A
- Two Xilinx Virtex-4 FPGAs
- Up to 768 MB of DDR2 SDRAM
- LVDS clock/sync bus for multiboard synchronization
- Optional factory-installed IP Cores available
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
  VITA-46 (VPX Baseline Standard)
  VITA-48 (VPX REDI)
  VITA-65 (OpenVPX™ System Specification)

General Information

Model 5342 is a multichannel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter.

The 5342 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

The 5342 features a TI DAC5686 digital upconverter (DUC) and D/A. It accepts a baseband real or complex data stream from its FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

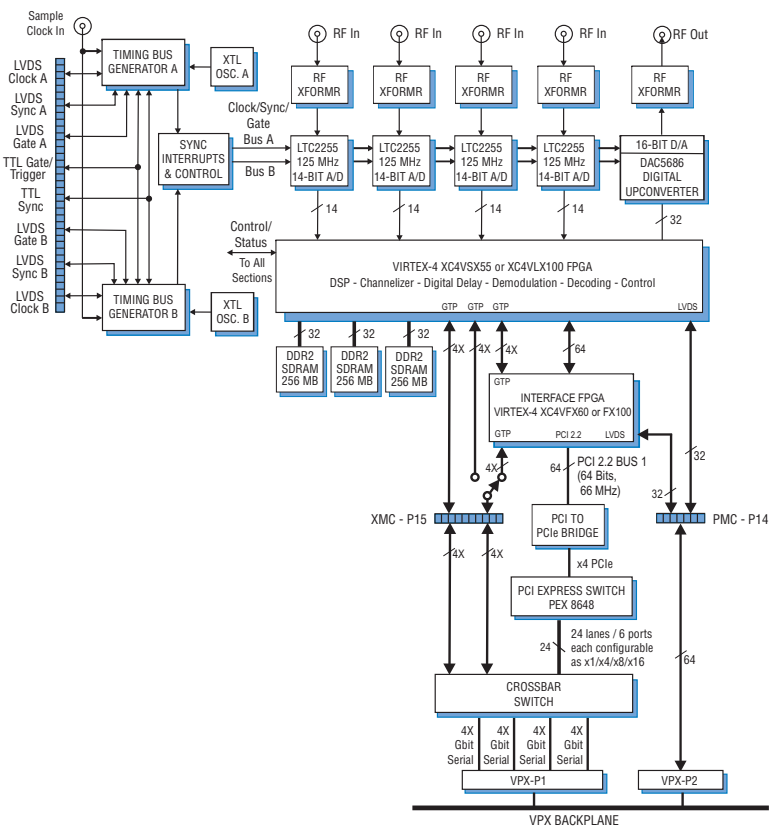
Virtex-4 FPGAs

The 5342 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP, and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.

The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for implementing functions such as demodulation/modulation, digital delay and channelization. For applications requiring more FPGA logic cells, the Model 5342 can be optionally configured with XC4VLX100 for up to 221,184 logic cells.

A Virtex-4 XC4VFX60 Interface FPGA provides board interfaces including PCI ➤



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Model 5342 — Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX

Fabric-Transparent Crossbar Switch

The 5342 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5342 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model	Description
5342	Multichannel Transceiver with four A/Ds, one D/A and Virtex-4 FPGAs - 3U VPX

Options:

-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O to VPX-P2
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core in the processing FPGA
-5xx	Gigabit Serial I/O to VPX-P1- four full-duplex 4X paths

➤ and serial I/O.

The interface FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 5342 can be optionally configured with XC4VFX100 in place of each FX60.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, upconverter and D/A. Internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, each LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 5342s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +10 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 300 MHz

A/D Converters
- **Type:** Linear Technology LTC2255
- **Sampling Rate:** 1 MHz to 125 MHz
- **Internal Clock:** 125 MHz crystal osc.
- **External Clock:** 1 to 125 MHz
- **Resolution:** 14 bits
- **A/D Data Reduction Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output
- **Output Type:** Transformer-coupled, front panel female MMCX connector
- **Full Scale Output:** +4 dBm into 50 ohms (other options available)
- **3 dB Passband:** 60 kHz to 300 MHz (other options available)

Digital Upconverter
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array
- **Type:** Xilinx Virtex-4 XC4VSX55 & Xilinx Virtex-4 XC4VFX60
- **Option -100:** XC4VFX100 replaces XC4VFX60
- **Option -110:** XC4VLX100 replaces XC4VSX55

Custom I/O
- **Option -104:** Adds GPIO connector with 32 lines to the XC4VFX60/100 FPGA

Memory
- **DDR2 SDRAM:** 768 MB in three banks to SX55/LX100 FPGA

PCI to PCIe Interface
- **PCI Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:
- **Processing FPGA:** Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA
- **VPX-P1**: Four 4X ports to Fabric-Transparent Crossbar Switch
- **PCI Express:** Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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