New!

Model 5341-430 Installed Core

GateFlow Transceiver, 256-Channel Narrowband DDC - 3U VPX

ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- 3U VPX form factor
- GateFlow Core 430 with 256 channels of narrowband digital downconverters factory-installed
- 256 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256
- LVDS clock/sync bus for multiboard synchronization

General Information

Model 5341-420 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters with built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch bridges numerous interfaces and components on the board with no latency.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 5341-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

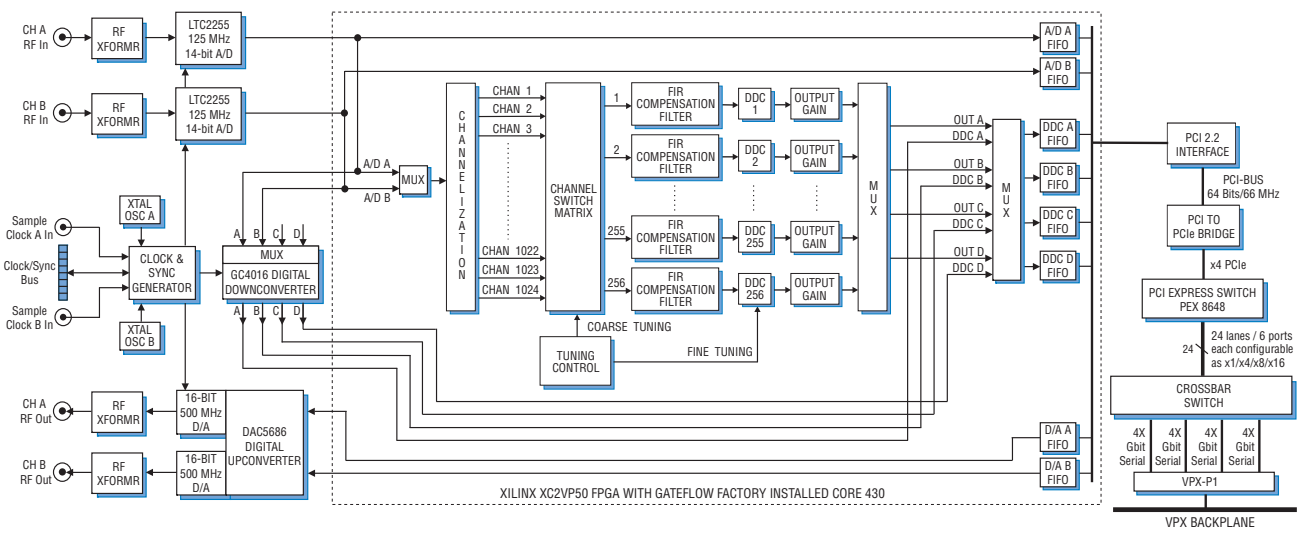
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2^{32}
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in this Model. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



PENTEK

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Model 5341-430 Installed Core

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Fabric-Transparent Crossbar Switch

The 5341-430 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

Ordering Information

Model	Description
5341-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 3U VPX

Contact Pentek for available options

➤ Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 5341-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Switch

Model 5341-430 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters
Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 1 to 125 MHz
Resolution: 14 bits

Digital Downconverter
Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter
Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array
Type: Xilinx Virtex-II Pro XC2VP50

Memory
DDR SDRAM: 512 MB in three banks

PCI to PCIe Interface
PCI Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller

Gigabit Serial I/O
VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch
PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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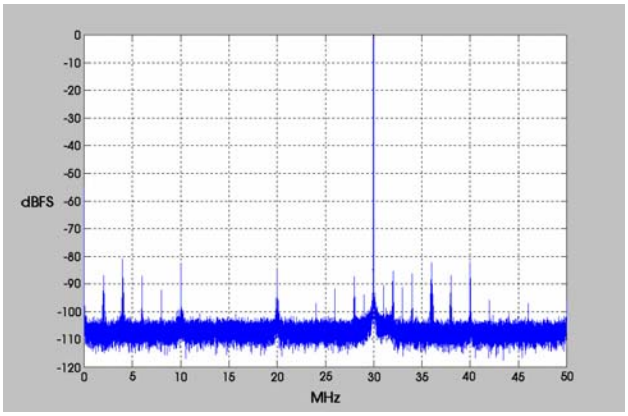
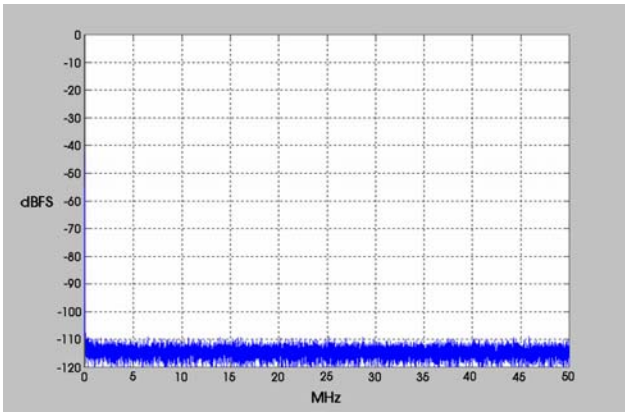
A/D Performance

Spurious Free Dynamic Range



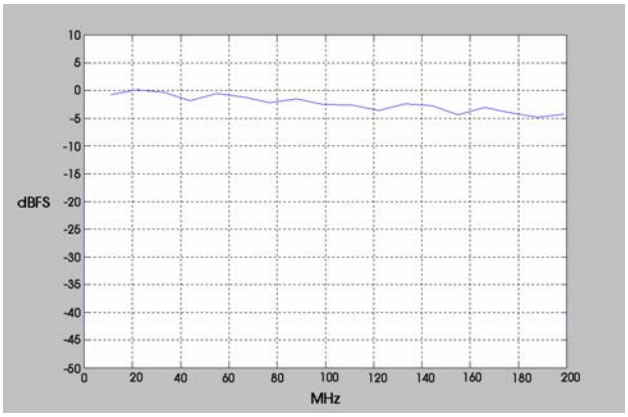
f_{in} = 70 MHz, f_s = 100 MHz

Spurious Pick-up



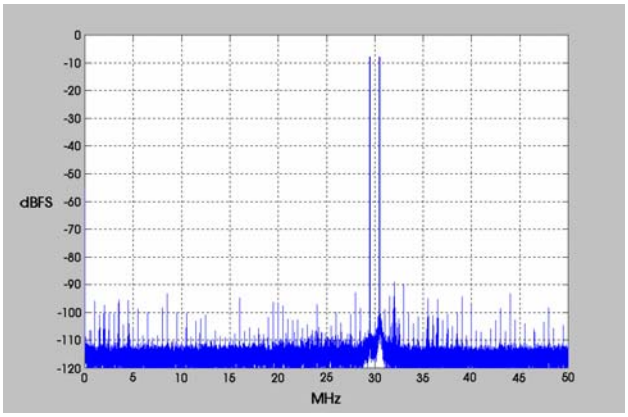
f_s = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



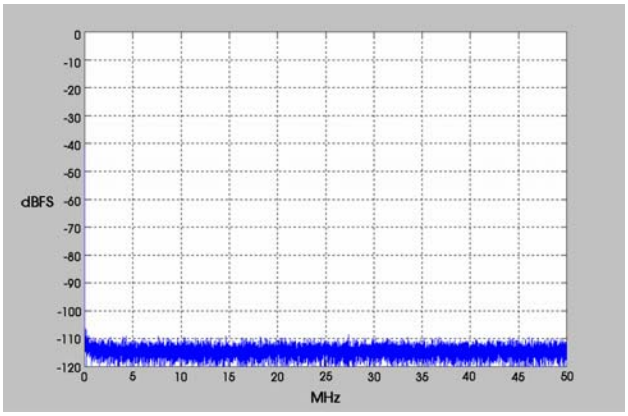
f_s = 100 MHz

Two-Tone SFDR



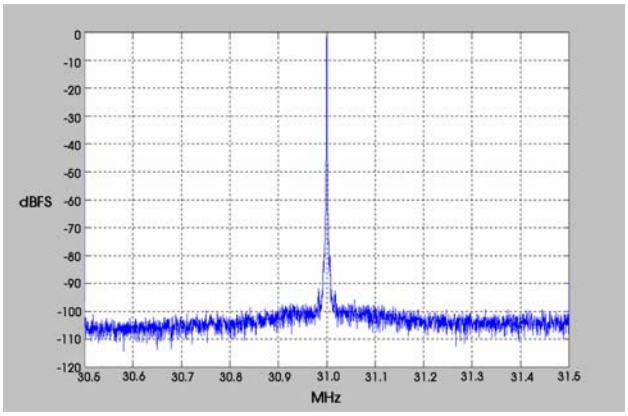
f_1 = 29.5 MHz, f_2 = 30.5 MHz, f_s = 100 MHz

Crosstalk



$f_{in\ Ch2}$ = 69 MHz, f_s = 100 MHz, Ch 1 shown

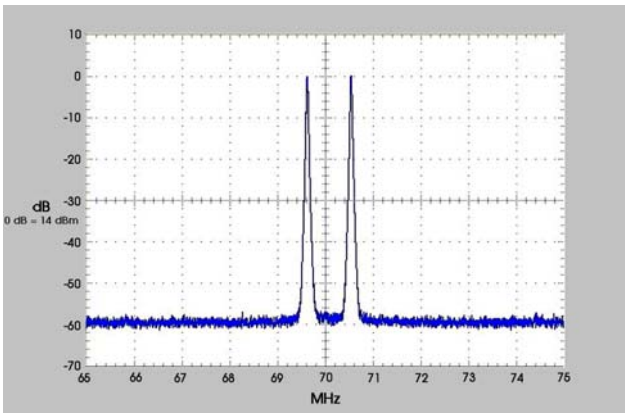
Phase Noise



f_{in} = 69 MHz, f_s = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz

D/A Performance

Two-Tone Intermodulation Distortion



f_1 = 69.5 MHz, f_2 = 70.5 MHz, f_s = 100 MHz