Model 5331

16-Channel Multiband Receiver with A/Ds and FPGA - 3U VPX

ReadyFlow Board Support Package

GateFlow

Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 80 or 105 MHz, 14-bit A/D converters
- 16 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for f_S = 100 MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGA
- Custom FPGA I/O through the VPX P-2
- Bypass path allows direct capture of A/D data
- LVDS clock/sync bus for multiboard synchronization
- Compatible with several VITA standards including:
  VITA-46 (VPX Baseline Standard)
  VITA-48 (VPX REDI)
  VITA-65 (OpenVPX™ System Specification)

General Information

Model 5331 is a general-purpose 16-channel multiband digital receiver 3U VPX board. It includes both a Virtex-II FPGA and two 14-bit A/Ds for signal processing. The 5331 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane.

Front End

The Model 5331 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

The two inputs are transformer coupled and digitized by AD6645 14-bit A/D converters. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz for option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector or the front panel sync bus.

Digital Downconverters

The 5331 includes four TI/Graychip GC4016 quad multiband digital downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency tuning from DC to $f_S/2$, where f_S is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A crossbar switch in each GC4016 allows all 16 channels on the board to select either of the two A/D inputs for flexible switching.

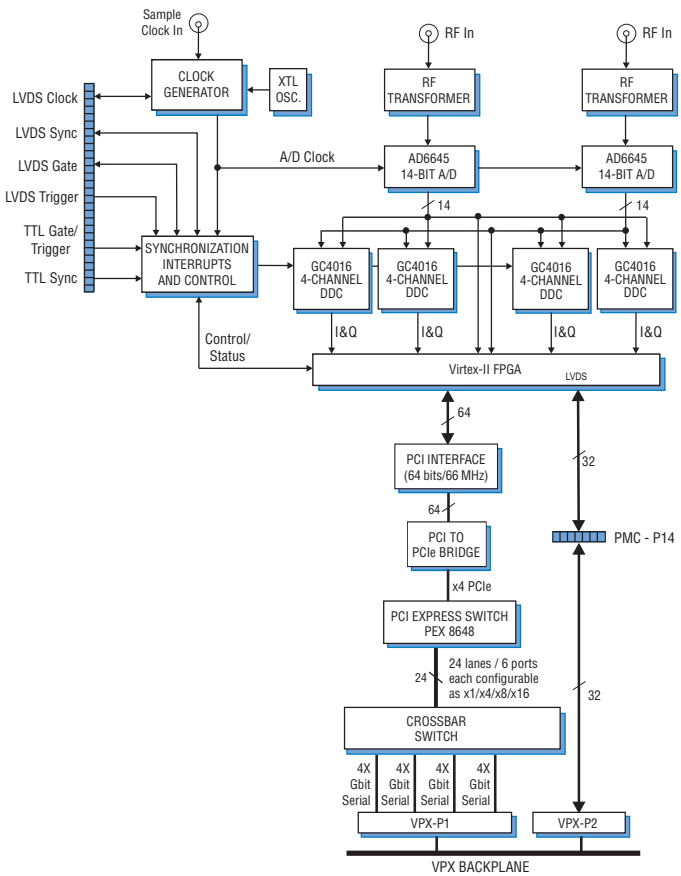
Output Bandwidth

With a 100 MHz sample clock, the useable output bandwidth of each of the downconverter channels is 2.5 MHz. However, since the Model 5331 delivers parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since both A/D converters connect directly to the FPGAs, signals with even wider bandwidths can be accommodated.

FPGA

The downconverter outputs are delivered to a Xilinx Virtex-II XC2V1000 FPGA (XC2V3000 with option -300) which is factory configured to perform various modes of data packing, formatting and channel selection. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 5331

16-Channel Multiband Receiver with A/Ds and FPGA - 3U VPX

Fabric-Transparent Crossbar Switch

The 5331 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

Ordering Information

Model	Description
5331	16-Channel Multiband Receiver with A/Ds and FPGA - PMC
Options:	
-100	105 MHz A/D with 100 MHz crystal oscillator
-104	FPGA I/O to VPX-P2
-300	XC2V3000 FPGA
-5xx	Gigabit Serial I/O to VPX-P1 - four full-duplex 4X paths

➤ Dual-port memories in the FPGA provide efficient transfers by buffering receiver and A/D data. The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the downconverters. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is any integer between 1 and 4096. This overcomes the lower frequency limit on the A/D sample clock.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the FPGA. Option -5xx adds four full duplex 4X gigabit serial paths to VPX-P1 connector.

Synchronization

The front panel clock and sync bus allow one 5331 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple boards.

Up to eight slave 5331's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. In addition to the LVDS timing bus, the Model 5331 can receive front panel TTL input signals for gate or trigger functions.

Interrupt Sources

The Model 5331 has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, or a programmable over-temperature condition or faulty power supply voltage. The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user programmable over the VPX backplane.

PCI Express Switch

Model 5331 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMA connectors
- **Transformer Type:** Mini-Circuits ADT4-6T
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 60 kHz to 270 MHz

A/D Converters, Standard
- **Type:** Analog Devices AD6645-80
- **Sampling Rate:** 30 MHz to 80 MHz
- **Internal Clock:** 80 MHz crystal osc.
- **External Clock:** 30 to 80 MHz
- **Resolution:** 14 bits

A/D Converters, Option -100
- **Type:** Analog Devices AD6645-105
- **Sampling Rate:** 30 MHz to 105 MHz
- **Internal Clock:** 100 MHz crystal osc.
- **External Clock:** 30 to 105 MHz
- **Resolution:** 14 bits

Clock Source: Onboard crystal oscillator, front panel ext clock, or LVDS clock

External Clock
- **Type:** Front panel female SMA connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms impedance

Sync/Gate Bus
- **Type:** 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals

Digital Downconverters
- **Type:** TI/Graychip GC4016
- **Decimation:** 32 to 16,384; with channel combining mode: 8 or 16
- **Data Source:** A/D outputs are connected to all GC4016's
- **Output:** Parallel complex data

Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Field Programmable Gate Array
- **Type:** Xilinx Virtex-II XC2V1000 standard
- **Option -300:** Virtex-II XC2V3000
- **Option -104:** Installs the P4 connector with 37 lines to the XC2V1000 or 64 lines to the XC2V3000 FPGA

Dual Port RAM Data Buffers
- **Size:** 4k x 32 DPRAM expandable to 8k x 32 with option -300 FPGA

PCI to PCIe Interface
- **Type:** PLX Technology PCI 9656
- **PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Gigabit Serial I/O:
- **VPX-P1**: Four 4X ports to Crossbar Switch
- **PCI Express:** Six ports to Crossbar Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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