New!

Model 52650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

Model 52650 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52650 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52650 includes two A/Ds, one DUC (digital upconverter), two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

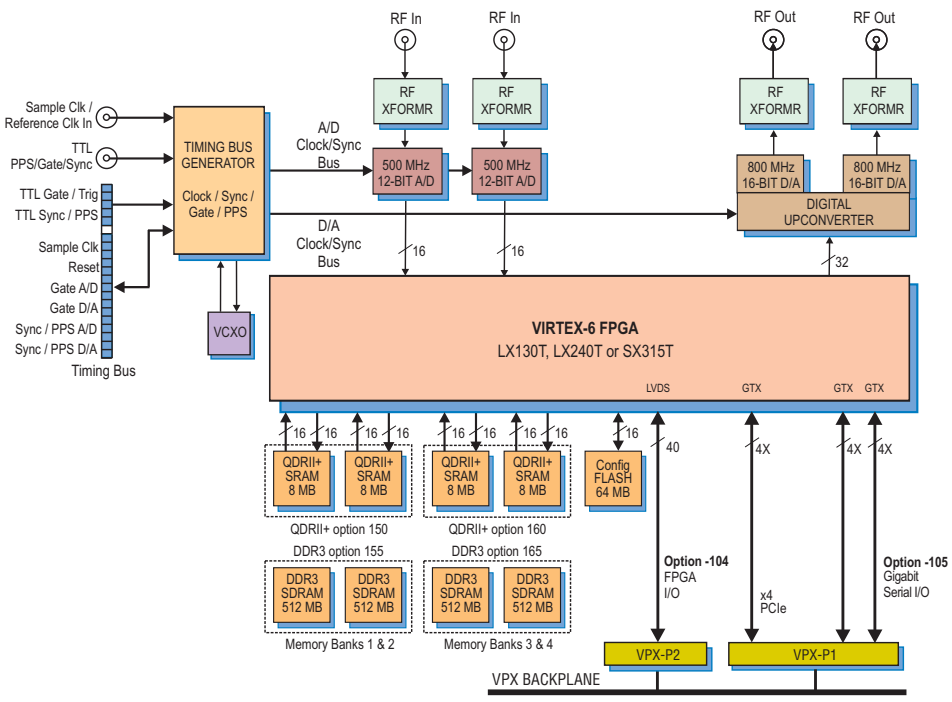
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

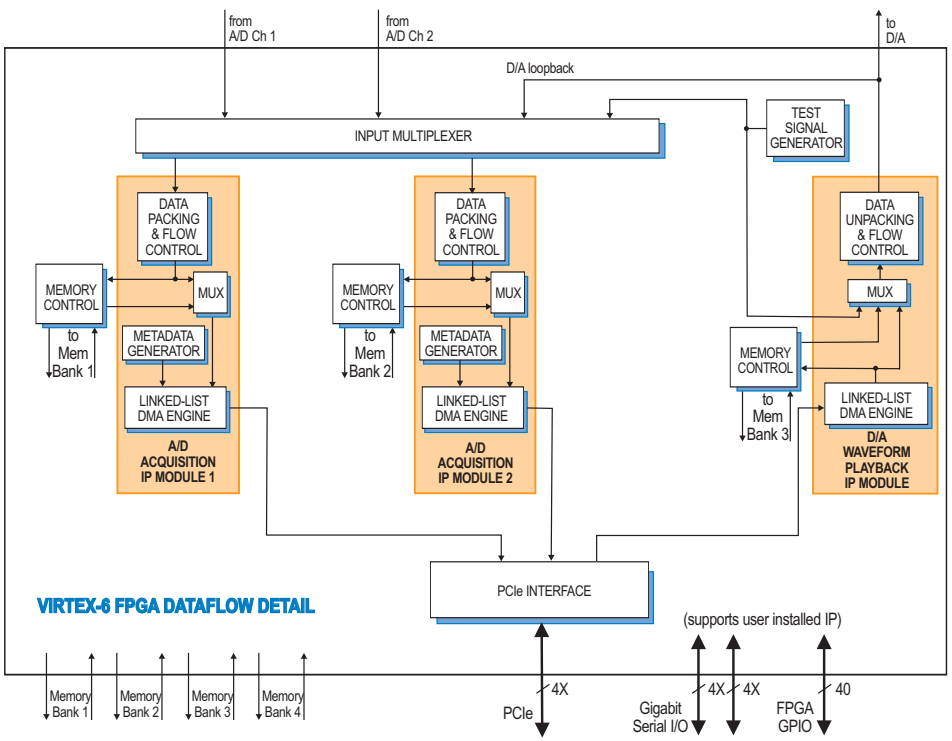
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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PCI Express Interface

The Model 52650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52650	Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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