

GateFlow® is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

The Pentek Model 4953 GateFlow FPGA Design Kit provides the user with design information, software files and utilities for extending FPGA functions in these products.

Users can implement a variety of custom preprocessing functions such as convolution, framing, pattern recognition, decompression, FFT, delay, decoding, time stamping, averaging, summation and many more.

For the latest GateFlow information go to: pentek.com/fpga

Using the FPGA Design Kit

The **GateFlow** FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt and Onyx architectures configure the FPGA with standard factorysupplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt or Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.









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Using the FPGA Design Kit

The **GateFlow** FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

FPGA Design Kit User Block

Shown below is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it.

The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.







GateFlow FPGA Design Kit

GateFiew

FPGAs in Pentek Products

These charts show the Xilinx FPGA families as used in the various Pentek board-level products. These products use some FPGA resources to implement standard factory functions as well as installed IP cores.

These charts show the percentage of unused system slices and RAM available to the user for extending the FPGA to include custom algorithms.

			Available FPGA Resources for Pentek Hardware												
	Xilinx Virtex-II Pro				Xilinx Virtex-4										
	-۷	'P50	-VP70		-FX60		-FX100		-SX55		-LX100				
Logic Cells			53,136 74,448		56,880		94,986		55,296		110,592				
CLB Slices			23,616 33,088		88	25,280 42,176		24,576		49,152					
CLB Flip-Flops			47,232		66,1	66,176		50,560		84,352		49,152		98,304	
Max. Block RAM (kb)			4,176		5,904		4,176		6,768		5,760		4,320		
Multipliers / DSP Blocks			232		328		128		160		512		96		
PowerPC Processor Blocks			2		2		2		2		-		-		
Pentek	Board	No. of	%	Availab	le to Use	ər	% Available to User								
Model	Туре	FPGAs	Slices	s RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	
4207	VME/VXS	1	-	-	-	-	38%	71%	61%	82%	-	-	-	-	
6821	VME/VXS	2	98%	100%	-	-	-	-	-	-	-	-	-	-	
6822	VME/VXS	2	98%	100%	-	-	-	-	-	-	-	-	-	-	
6826	VME/VXS	1	-	-	75%	72%	-	-	-	-	-	-	-	-	
7142*	PMC/XMC	2	-	-	-	-	77%	92%	86%	95%	54%	78%	77%	71%	

			Available FPGA Resources for Pentek Hardw						vare									
	Xilinx Virtex-5					Xilinx Virtex-6					Xilinx Virtex-7							
			-S)	(50T	-SX	95T	-LX1	155T	-LX	130T	-LX2	240T	-SX3	315T	-VX	330T	-VX6	690T
Logic Cells		52	,224	94,208		155	,648	12	8,000	241,152		314,880		326,400		693,120		
CLB Slices		8,	160	14,720		24,320		20	20,000 37,680		49,200		51,000		108,300			
CLB Flip-Flops			32	,640	58,880		97,280		160,000		301,440		393,600		408,000		866,400	
Max. Bloc	k RAM (kb)		4,	4,752 8,784		7,632		9,504		14,976		25,344		27,000		52,920		
DSP48E Blocks			2	288 640		128		480		768		1,344		1120		3,600		
PCI Express Support			_			-	-	Gen2,x8 Gen2,x8		Gen2,x8		Gen 3, x8		Gen3,x8				
Pentek Board No. of		No. of	% Available to Us			ser			%	Availab	e to Us	er		% Available to User				
Model	Туре	FPGAs	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM
7150*	PMC/XMC	2	7%	75%	36%	86%	64%	84%	-	-	-	-	-	-	-	-	-	-
7153*	PMC/XMC	2	N/A	N/A	42%	45%	N/A	N/A	-	-	-	-	-	-	-	-	-	-
7156*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	-	-	-	-	-	-	-	-	-	-
7158*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	-	-	-	-	-	-	-	-	-	-
71620**	XMC	1	-	-	-	-	-	-	68%	75%	83%	82%	TBD	TBD	-	-	-	-
71621**	XMC	1	-	-	-	-	-	-	-	-	66%	63%	TBD	TBD	-	-	-	-
71630**	XMC	1	-	-	-	-	-	-	55%	64%	76%	77%	81%	86%	-	-	-	-
71640**	XMC	1	-	-	-	-	-	-	8%	64%	46%	77%	59%	86%	-	-	-	-
71650**	XMC	1	-	-	-	-	-	-	66%	74%	82%	84%	86%	90%	-	-	-	-
71651**	XMC	1	-	-	-	-	-	-	-	-	47%	65%	58%	79%	-	-	-	-
71660**	XMC	1	-	-	-	-	-	-	69%	75%	76%	85%	88%	92%	-	-	-	-
71661**	XMC	1	-	-	-	-	-	-	-	-	43%	67%	TBD	TBD	-	-	-	-
71662**	XMC	1	-	-	-	-	-	-	-	-	TBD	TBD	48%	62%	-	-	-	-
71670**	XMC	1	-	-	-	-	-	-	24%	46%	58%	65%	68%	80%	-	-	-	-
/1690**	XMC	1	-	-	-	-	-	-	80%	87%	89%	91%	91%	95%	-	-	-	-
/1720***	XMC	1	-	-	-	-	-	-	-	-	-	-	-	-	IRD	IBD	IBD	IBD
71760***	XMC	1	-	-	-	-	-	-	-	-	-	-	-	-	IBD	IRD	IBD	IRD

* Other form factors: 72xx = 6U cPCI; 73xx = 3U cPCI; 76xx = PCI; 77xx = Full-Length PCIe; 78xx = Half-Length PCIe; 53xx = 3U VPX **Cobalt form factors: 716xx = XMC; 726xx = 6U CPCI; 736xx = 3U cPCI; 746xx = 6U CPCI (Dual XMC); 786xx = Half-Length PCIe;

536XX = 3U VPX - Format 1; 526XX = 3U VPX - Format 2; 566xx = AMC

***Onyx form factors: 717xx = XMC; 727xx = 6U CPCI; 737xx = 3U cPCI; 747xx = 6U CPCI (Dual XMC); 787xx = Half-Length PCIe; 537XX = 3U VPX - Format 1; 527XX = 3U VPX - Format 2; 567xx = AMC

%Available to User: Applies to the Processing FPGA(s) of certain products; % Available can vary slightly due to rounding



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Ordering Information

Model	Description
4953	GateFlow FPGA
	Design Kit

Options:	Supported Product w/ FPGA option
-142-055*	7142 w/ XC4VSX55
-142-060*	7142 w/ XC4VFX60
-142-100*	7142 w/ XC4VFX100
-142-110*	7142 w/ XC4VLX100
-150-083*	7150 w/ XC5VLX155T
-150-084*	7150 w/ XC5VSX50T
-150-085*	7150 w/ XC5VSX95T
-153-085*	7153 w/ XC5VSX95T
-156-083*	7156 w/ XC5VLX155T
-156-084*	7156 w/ XC5VSX50T
-156-085*	7156 w/ XC5VSX95T
-158-083*	7158 w/ XC5VLX155T
-158-084*	7158 w/ XC5VSX50T
-158-085*	7158 w/ XC5VSX95T
-620-061**	71620 w/ XC6VLX130T
-620-062**	71620 w/ XC6VLX240T
-620-064**	71620 w/ XC6VSX315T
-621-062**	71621 w/ XC6VLX240T
-621-064**	71621 w/ XC6VSX315T
-630-061**	71630 w/ XC6VLX130T
-630-062**	71630 w/ XC6VLX240T
-630-064**	71630 w/ XC6VSX315T
-640-061**	71640 w/ XC6VLX130T
-640-062**	71640 w/ XC6VLX240T
-640-064**	71640 w/ XC6VSX315T
-641-064**	71641 w/ XC6VSX315T
-650-061**	71650 w/ XC6VLX130T
-650-062**	71650 w/ XC6VLX240T
-650-064**	71650 w/ XC6VSX315T
-651-062**	71651 w/ XC6VLX240T
-651-064**	71651 w/ XC6VSX315T

Options: Supported Product w/ FPGA option

-660-061**	71660 w/ XC6VLX130T
-660-062**	71660 w/ XC6VLX240T
-660-064**	71660 w/ XC6VSX315T
-661-062**	71661 w/ XC6VLX240T
-661-064**	71661 w/ XC6VSX315T
-662-062**	71662 w/ XC6VLX240T
-662-064**	71662 w/ XC6VSX315T
-670-061**	71670 w/ XC6VLX130T
-670-062**	71670 w/ XC6VLX240T
-670-064**	71670 w/ XC6VSX315T
-671-062**	71671 w/ XC6VLX240T
-671-064**	71671 w/ XC6VSX315T
-690-061**	71690 w/ XC6VLX130T
-690-062**	71690 w/ XC6VLX240T
-690-064**	71690 w/ XC6VSX315T
-720-073***	71720 w/ XC7VX330T
-720-076***	71720 w/ XC7VX690T
-760-073***	71760 w/ XC7VX330T
-760-076***	71760 w/ XC7VX690T
-207-060	4207 w/ XC4VFX60
-207-100	4207 w/ XC4VFX100
-821-022	6821 w/ XC2VP20
-821-052	6821 w/ XC2VP50
-822-022	6822 w/ XC2VP20
-822-052	6822 w/ XC2VP50
-826-072	6826 w/ XC2VP70

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Example:	Model	Description	Form Factor
	71660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	XMC
	72660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	6U cPCI
	73660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	3U cPCI
	74660	Cobalt Octal 200 MHz, 16-bit A/D with Virtex-6 FPGAs	6U cPCI w/ Two XMCs
	78660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	x8 PCIe
	53660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	3U VPX - Format 1
	52660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	3U VPX - Format 2
	56660	Cobalt Quad 200 MHz, 16-bit A/D with Virtex-6 FPGA	AMC

Contact Pentek for the latest products and FPGA options.



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