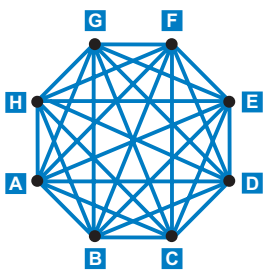
RACEway and FPDP: High-Speed Interfaces for Optimizing I/O

RACEway Features

- 160 MB/sec data transfer
- Up to 267 MB/sec with new **RACE++** technology
- 32-bit word transfers
- Multiple simultaneous data transfers
- Unique crossbar technology
- Priority control
- Adaptive routing
- Data broadcast to multiple slaves
- Completely independent of VMEbus
- Low power consumption



RACE++ Crossbar Switch

FPDP Features

- 160 MB/sec data transfer
- Up to 400 MB/sec with new **FPDP II** technology
- 32-bit word transfers
- 80-pin flat ribbon cable front panel connectors
- Can be used across multiple VME chassis
- Completely independent of VMEbus

RACEway

RACE 1.0 and RACE++

Created by Mercury Computer to solve demanding backplane interconnection requirements, RACEway is a high-speed synchronous interface capable of delivering 32-bit word transfers between VME boards. Transfer rates are as high as 160 MB/sec for the original RACE 1.0 technology, and 267 MB/sec for the new RACE++.

The high-speed data channel provided by RACEway utilizes the 64 user-defined pins of the VMEbus P2 connector and is completely independent of the VMEbus. Transfers occur in the form of 2 kB data packets, each containing the necessary routing and delivery address information to steer it to a unique destination.

RACEway uses Interlink modules, commonly referred to as ILKs (or ILKPs for RACE++), to connect VME boards to the RACEway interface. The ILKs provide multiple, simultaneous high-speed communication paths between VME boards. Features such as priority control and automatic free path selection (adaptive routing) make the RACEway ILK a valuable asset to real-time applications.

The Interlink module is a circuit board assembly that mates with the 64 pins of the P2 connector to provide RACEway communication between boards. ILKs and ILKPs are both available in sizes that bridge 4, 8, 12 and 16 VMEbus slots. RACEway Interlink Modules use unique crossbar switches for data routing.

The RACE 1.0 Crossbar contains six independent 32-bit bidirectional data ports. Each data port controls arbitration, direction, priority, handshaking and all other aspects of protocol operation. The RACE 1.0 Crossbar can perform up to three simultaneous transfers for a total of 480 MB/sec.

The RACE++ Crossbar contains eight independent 32-bit bidirectional data ports, each controlling the same aspects of protocol operation as the RACE 1.0 Crossbar. It can perform four simultaneous transfers totalling 1.07 GB/sec.

More detailed information is contained in the Pentek RACEway Handbook, available free of charge upon request. Visit **www.pentek.com/raceway** for a list of our RACEway products. The RACEway Specification approved by ANSI is available for purchase from **www.vita.com/pubslist.html**.

FPDP

FPDP and FPDP II

The Front Panel Data Port (FPDP) bus provides data transfers between two or more VMEbus boards with transfer rates as high as 160 MB/sec for FPDP technology, and 400 MB/sec for the new FPDP II technology. Data transfers are accomplished without compromising existing VMEbus and other connections on the P1 and P2 connectors.

The FPDP and FPDP II bus are both connected by means of an 80-conductor ribbon cable connector on the front panel of the VME board. The same connector is used for both FPDP and FPDP II systems, ensuring backwards compatibility. Multiple FPDP buses may coexist in a single VMEbus enclosure.

The FPDP bus is a 32-bit parallel synchronous bus. A single master device generates a free-running clock, the frequency of which defines the maximum data transfer rate of the bus. While transfers occur in one direction only, FPDP interfaces may be configured as transmitters or receivers through hardware such as links or switches, or under software control.

The bus protocol does not include address or arbitration cycles, so the data transfer rate is fully defined by the clock frequency. A mechanism is provided to allow a receiver to hold off the transmitter if its memory is full. A mechanism is also provided to allow synchronization of the receiver to the transmitted data stream to provide for memory initialization and correct interpretation of data.

FPDP II features increased bandwidth using double-edged clocking. Using a 50 MHz PECL clock, data rates are increased to as high as 400 MB/sec. The user can switch between single and double-edged clock settings for backwards compatible systems.

Each VME board may have more than one FPDP interface, to support separate input or output data paths. Furthermore, FPDP buses may be used to connect between separate VME card cages, subject to maximum cable length limitation.

Visit **www.pentek.com/fpdp** for a list of our FPDP products. The FPDP Specification approved by ANSI is available for purchase from **www.vita.com/pubslist.html**. ❑