Model 7642

Multichannel Transceiver with Virtex-4 FPGAs - PCI

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- Four 125 MHz 14-bit A/Ds
- One digital upconverter
- One 500 MHz 16-bit D/A
- 768 MB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- Up to 2.0 seconds of delay or data capture at 125 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-4 FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Model 7640 is a half-length PCI multichannel transceiver. It consists of one Model 7142 transceiver mounted on a PCI carrier board. The Model 7642 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

The Model 7642 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can include their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

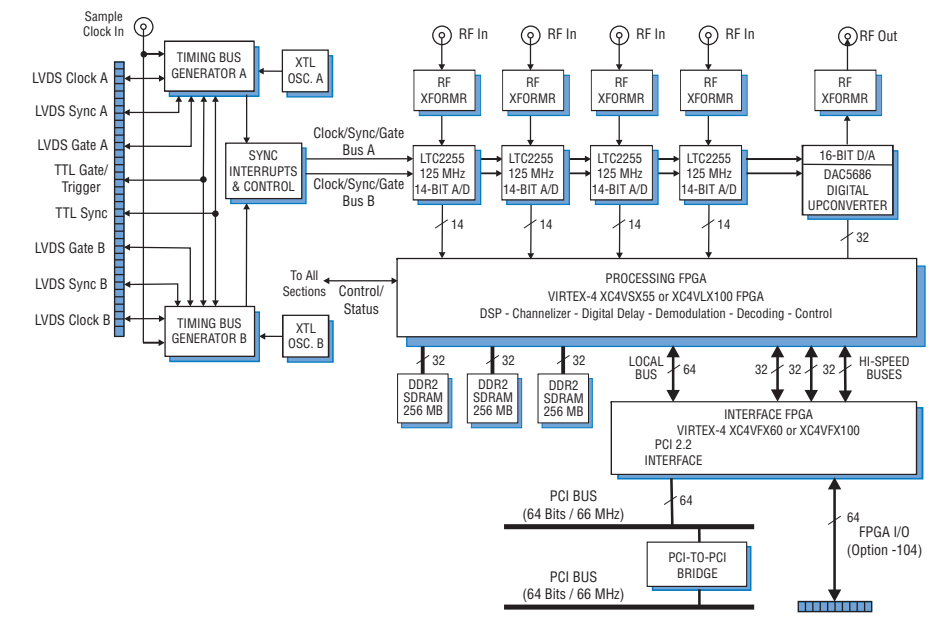
The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission.

For applications requiring more FPGA logic cells, the Model 7642 can be optionally configured with an XC4VLX100 in place of the XC2VSX55 for 110,592 logic cells.

A second Virtex-4 FPGA provides board interfaces including PCI and serial I/O. The XC4VFX60 FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 7642 can be optionally configured with a XC4VFX100 in place of the XC4VFX60.

Option -104 installs a 64-pin DIN connector with 32 pairs of LVDS lines to the XC4VFX60/100 FPGA for custom I/O. ➤



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Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds and the upconverter and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7642s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

The Model 7642 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +10 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 300 MHz

A/D Converters
- **Type:** Linear Technology LTC2255
- **Sampling Rate:** 1 MHz to 125 MHz
- **Internal Clock:** 125 MHz crystal osc.
- **External Clock:** 1 to 125 MHz
- **Resolution:** 14 bits
- **A/D Data Reduction Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output
- **Output Type:** Transformer-coupled, front panel female MMCX connector
- **Full Scale Output:** +4 dBm into 50 ohms (other options available)
- **3 dB Passband:** 60 kHz to 300 MHz (other options available)

Digital Upconverter
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array
- **Type:** One Xilinx Virtex-4 XC4VSX55 & one Xilinx Virtex-4 XC4VFX60
- **Option -100:** XC4VFX100 replaces XC4VFX60
- **Option -110:** XC4VLX100 replaces XC4VSX55

Custom I/O
- **Option -104:** Installs 64-pin DIN connector with 64 lines to the XC4VFX60/100 FPGA

Memory
- **DDR2 SDRAM:** 768 MB in three banks

PCI Interface
- **PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
- **Local Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model	Description
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI
Options:	
-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O through 64-pin DIN connector
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core

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