New!

Model 7190

Multifrequency Clock Synthesizer - PMC

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –125 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 or 10 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 500 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7190	Multifrequency Clock Synthesizer - PMC
Options	
	Specify frequencies of four factory-installed quad VCXOs between 50 and 500 MHz

* Contact Pentek to order specific frequencies

General Information

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from an input reference signal using phase-locked oscillators.

Clock Synthesizer Circuits

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 includes phase-locking circuitry that locks the frequency of its associated quad VCXO (Voltage Controlled Crystal Oscillator) to the input reference clock. This reference is a 5 or 10 MHz signal supplied to a front panel SMC connector. Each quad VCXO is programmed to generate one of four base frequencies.

Each CDC7005 generates five output signals. Each signal is independently programmable as a submultiple of the associated VCXO base frequency using divisors of 1, 2, 4, 8 or 16.

The five clock output signals from each of the four CDC7005s are joined into five clock buses. Each CDC7005 output can be independently enabled to drive each bus, thereby allowing any combination of output signals from the four CDC7005s.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock buses, as shown in the block diagram. This supports a single identical clock to all eight outputs or five different clocks to various outputs; numerous other combinations are possible.

PCI Interface

The Model 7190 uses an industry-standard 32 bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Power Up Auto Configuration

The 7190 is equipped with a non-volatile memory. Once configured, the settings return to the saved configuration upon power up. Once a configuration is saved, the 7190 does not require PCI access; this is convenient for deployed applications that do not include a host computer.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 or 10 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizer & Jitter Cleaner
- **Quantity:** 4
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

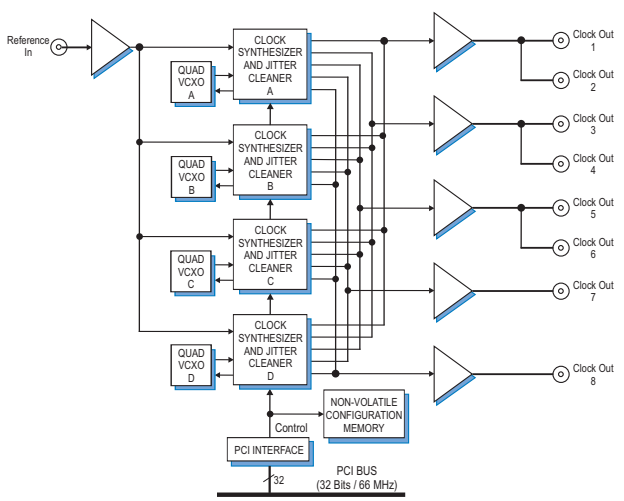
Quad VCXOs
- **Quantity:** 4
- **Frequencies per VCXO:** 4*, software-programmable
- **Unlocked Accuracy:** +/– 20 ppm

Front Panel Clock Outputs
- **Quantity:** 8
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +4 dBm
- **Typ. Phase Noise:** –125 dBc/Hz @ 1 kHz (dependent on source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: standard PMC module, 2.91 in. x 5.87 in.



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