

New!

Model 6826

Dual 2 GHz, 10-bit A/D VME Board with Virtex-II Pro FPGA



Features

- One or two 10-bit, 2 GHz A/D converters
- Dual 4x full duplex VXS links
- Two or four front panel FPDP or FPDP II outputs
- Up to 1 GB DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Multiboard synchronization

Ordering Information

Model	Description
6826	Dual 2 GHz, 10-Bit A/D VME board with Virtex-II Pro FPGA, VMEbus

Options:

- 001 Single A/D Converter
- 002 Dual A/D Converters
- 070 XC2VP70 FPGA
- 100 XC2VP100 FPGA
- 121 LVDS I/O through P2
- 222 2nd-Slot LVDS I/O
- 224 2nd-Slot FPDP I/O
- 340 1 GB DDR SDRAM
- 501 VXS with Xilinx Aurora
- 502 VXS Interface with Serial RapidIO (VITA-41.2)

General Information

The Model 6826 is a high-frequency single or dual channel A/D converter in a 6U VMEbus form factor. It accepts one or two front panel analog inputs and delivers digital output samples over two or four FPDP connectors utilizing FPDP or FPDP II standards. The 6826 is an ideal high-speed data acquisition front end for real-time recorders, digital receivers and DSP systems.

Input Stage and A/D Converter

The 6826 features one or two Atmel AT84AS008 2 GHz, 10-bit A/D converters driven from single-ended or differential RF signals applied through front panel MMCX female connectors at -2 dBm full scale into 50 ohms. Although the standard transformer-coupled input circuitry accepts signals to 1 GHz, higher frequency input options are also available.

An innovative dual-stage demultiplexer circuit packs groups of eight data samples into 80-bit words for delivery to the FPGA at one eighth the sampling frequency ($fs/8$). This advanced circuit features the Atmel AT84CS001 Demultiplexer, representing a significant improvement over previous technology.

Clocking, Gating and Triggering

The A/D converter sample clock is an externally supplied sinusoidal clock at a frequency from 150 MHz to 2 GHz. This clock is accepted through a front panel MMCX connector with 50 ohm termination, and applied to a power splitter for distribution to both A/D converters (dual-channel version) and the Sync/Gate circuit.

Synchronization and triggering circuitry supports synchronous data acquisition across multiple boards. Additional front panel MMCX connectors are provided for the

application of a $fs/8$ clock to support multiboard synchronization.

Virtex-II Pro FPGA

The 6826 utilizes a Model XC2VP70 or XC2VP100 Xilinx Virtex-II Pro FPGA. The FPGA is equipped with 512 MB of DDR SDRAM (optionally expandable to 1 GB) and 16 MB of FLASH memory.

Several data packing modes allow formatting output data across multiple FPDP ports. The FPGA also acts as a controller for board functions such as gate/trigger. Optional LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

Optional VXS Interface

The 6826 provides two optional 4x full duplex VITA-41 links to the VXS P0 connector, each capable of peak rates to 1.25 GB/sec. These links support Gigabit fabrics such as Xilinx Aurora, Serial RapidIO and PCI Express.

FIFOs and FPDP Outputs

Following the FPGA are two or four 32-bit wide FIFO buffers with a standard depth of 32k words each. These FIFOs are useful as elastic memory to support hard disk latencies in recording applications.

A total of four FPDP output ports are available, each supporting data transfers of up to 400 MB/sec. Two FPDP ports are attached to the 6826 front panel, and two additional ports optionally attach to a second slot front panel.

FPGA Programming

Optionally available GateFlow FPGA Design Kits allow the FPGA to be configured by the user for implementation of custom preprocessing functions.

Block Diagram, Model 6826

