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PRODUCT HOW-TO: Building an FPGA-based Digital Down Converter

By Richard Kuenzler and Robert Sgandurra
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The digital downconverter (DDC) has become a cornerstone technology in communication systems. Similar to its analog receiver counterpart, the DDC provides the user with a means to tune and extract a frequency of interest from a broad radio spectrum.

Over the past few years, the functions associated with DDCs have seen a shift from being delivered in ASICs to operating as IP (intellectual property) in FPGAs.

For many applications, this implementation shift brings advantages such as design flexibility, higher precision processing, higher channel density, lower power and lower cost per channel. With the advent of each new higher performance FPGA family, these benefits continue to increase.

This article explores some of the key advantages of implementing DDC designs in FPGAs and describes some of the situations when ASICs can still offer the best solution.

DDC fundamentals
To understand how FPGAs play a key role in implementing DDCs that perform the function of a receiver, it's important to break the DDC down into its individual functional blocks.

Figure 1 below shows a classic DDC. Whether it's implemented in an ASIC or an FPGA, this is the common architecture of the DDC function.

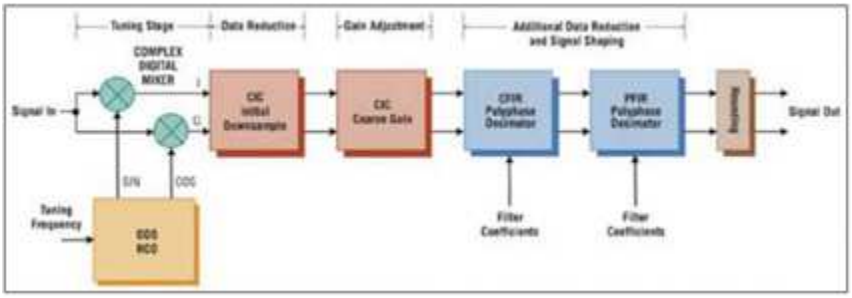

Figure 1: Regardless of whether it's implemented in an ASIC or an FPGA, this is the common architecture of the DDC function.

The first stage of the DDC uses a complex digital mixer to translate the frequency of interest down to baseband. It uses a pair of multipliers and a direct digital synthesizer as the numerically controlled oscillator.

This function enables the user to tune the receiver to the desired frequency of interest. The second stage of the DDC reduces the sampling frequency of the signal to match the desired output bandwidth. It uses a cascaded integrator comb (CIC) filter to decimate the data.

A second CIC filter provides a coarse gain adjustment stage. The signal is then passed to a pair of additional polyphase filters—first, a compensation FIR filter then a programmable FIR filter. This filter pair provides additional decimation and final signal shaping prior to the rounding stage and final output.

When we get past all the acronyms, we realize that most of the individual function blocks of the DDC are implemented using multipliers. Thus, it becomes apparent how the DDC might map into current FPGA families.

Most new FPGAs include a wealth of DSP function blocks that are primarily multipliers. The general purpose logic resource and onchip memory of FPGAs also match the requirements of the DDC for implementing the required FIR filters and filter coefficient tables.

DDCs as IP cores

As part of its IP library series, Xilinx provides a free DDC core. The core serves as a good general reference design, following the classic DDC architecture shown in **Figure 1 above**.

While this core can be used as a building block for general-purpose DDCs, the real advantages of an IP-based implementation can be best seen in optimized custom cores that are designed to match the requirements of a specific application.

Pentek offers a series of high-performance IP-based DDCs, available preinstalled in software radio modules. Each is optimized to match a specific range of application requirements. These cores range from the high-channel count/narrow bandwidth of the 430 Core installed in the Model 7141 to the wider bandwidths and excellent spurious free dynamic range (SFDR) of the core installed in the Model 7153.

Table 1 below lists the range of DDC cores available from Pentek as software radio modules. For each core, pertinent specifications are listed. All products are available in industry-standard PMC/XMC modules as well as 3U and 6U CompactPCI, PCI and PCIe form factors.

DDC Implementation	Number of Channels	Decimation Range	Input Rate (MHz)	SFDR (dBFS)	Decimation Steps	Area per Channel (mm²)[1]	Power per Channel (W)[2]	Cost per Channel ($)[3]
TI GC4016 ASIC	4	32–16,384	160	115	1	72.3	0.25	41
Pentek 7141-420	2	2–64	110	118	Binary	612.5	2.5	204
Pentek 7141-430	256	1,024–9,984	110	110	256	4.7	0.01	2
Pentek 7142-428	4	2–65,536	125	108	1	206.2	2.0	102
Pentek 7151	256	128–1,024	200	105	64	4.7	0.04	6
Pentek 7152	32	16–8,192	200	105	8	38.3	0.25	44
Pentek 7153	4	2–256	200	120	1	206.2	1.25	29
Pentek 7153	2	2–65,536	200	120	1	612.5	2.5	57

Note [1]: Area per Channel = IC area ÷ number of channels.

Note [2]: GC4016 Power per Channel = Total IC power ÷ number of channels. IP Core Power per Channel = (FPGA power with IP core – FPGA power without IP core) ÷ number of channels.

Note [3]: GC4016 Cost per Channel = cost of IC ÷ number of channels. IP core Cost per Channel = cost of FPGA resources used ÷ number of channels.

Table 1: Listed are the performance characteristics of ASIC and FPGA IP DDC Cores.

In addition to the IPbased solutions, a popular ASICbased DDC solution from Texas Instruments—the GC4016—is included as a reference. When compared on a size/ power/cost per channel basis, it becomes apparent that narrowband, high channel-count DDC cores can

be very efficiently implemented in FPGAs. Implementation of wideband DDCs consumes many more FPGA DSP and logic resources.

As a result, the number of channels that can be fit into a single FPGA is limited. Even with less cost-effective wide-band DDCs, the custom IP approach can sometimes provide the only viable solution when a specific performance characteristic is required. The improved SFDR of the Pentek 420 core is an example of such a requirement.

Flexible implementation
An additional benefit of IP-based solutions is the flexible nature of their implementation. The Models 7141-420 and 7141-430 are created by using the same hardware base with different installed IP cores.

Similarly, the Models 7151, 7152 and 7153 are all based on the same 4-channel, 200MHz, 16bit A/D PMC/XMC with different FPGA IP cores. All share the same software base allowing migration between different applications to be accomplished with minimum software porting.

Additionally, some applications like joint tactical radio system need to operate across a wide spectrum to handle the diverse signal types. Such applications can benefit greatly by IP-based solutions.

Figure 2 below shows the six optimized Pentek cores across a range of applications and the number of channels and bandwidth they typically require.

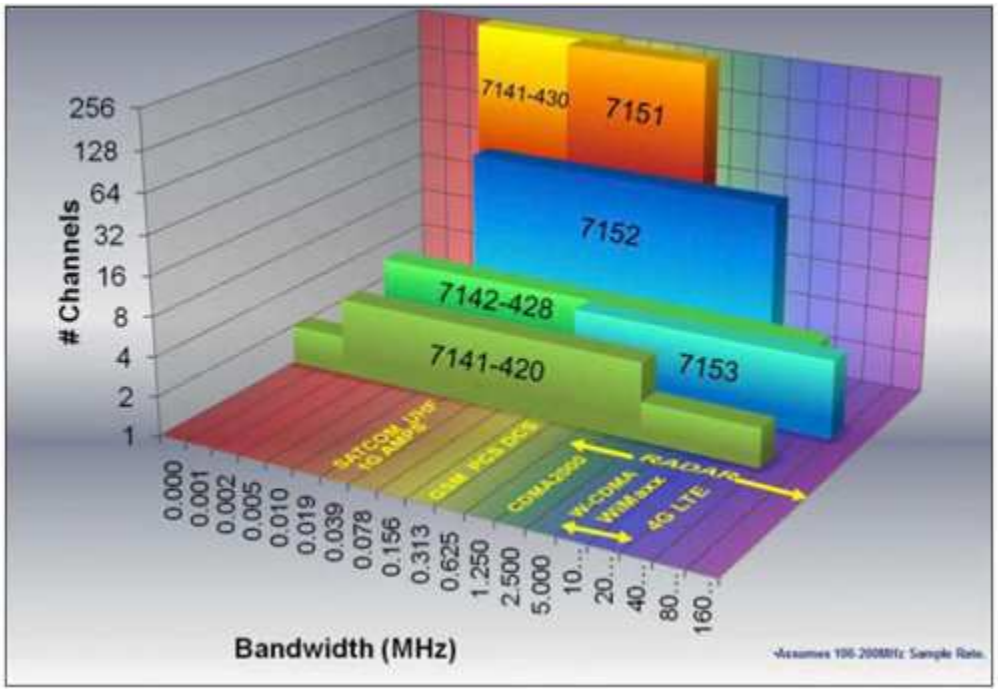

Figure 2: Shown are the six optimized Pentek cores across a range of applications and the number of channels and bandwidth they typically require.

Again, this wide range of applications can be satisfied by using a small set of hardware with different, optimized IP cores. This is one of the fundamental concepts of SDR, and it's difficult—if not impossible—to achieve with ASIC-based solutions.

System-level savings
Let's now take a look at a complete receiver system. One common application is GSM 2G, a

high channel count, low bandwidth system. An E-GMS receiver requires 174 channels spaced 200kHz apart. Just three or four years ago, a viable solution would have used the TI/Graychip 4-channel GC4016 ASIC-based DDCs.

A common board form factor for these types of application is PMC such as the Pentek Model 7131. One PMC can house two 100MHz A/Ds and four GC4016s, and all of the required interface and support circuitry. For a 174-channel system, this would require 11 Model 7131's.

By comparison, an IP DDC with 174 channels and similar performance to the 4016 can fit in a single Virtex-5 XC5VSX95T FPGA that can be housed on a single PMC, along with 2 channels of 200MHz A/Ds and all support circuitry such as the Pentek Model 7151. A visual comparison of these two solutions is shown in **Figure 3 below**.

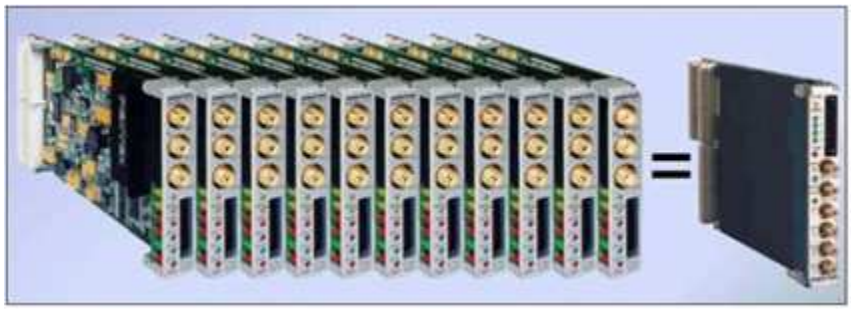

Figure 3: An IP DDC with 174 channels and similar performance to the 4016 can fit in a single Virtex-5 XC5VSX95T FPGA that can be housed on a single PMC.

FPGAs vs. ASICs

FPGAs continue to offer new possibilities and performance when addressing processing tasks like DDC. With each new generation of higher performance FPGAs, processing precision continues to increase. This enables IP-based DDCs to outperform their ASICbased cousins with specifications like better SFDR.

As shown in **Figure 4 below**, it's easy to understand how packing many channels of DDCs into one or two FPGAs can reduce the board count, power requirements and cost over a solution that requires 30 or 40 individual ASIC DDC chips.

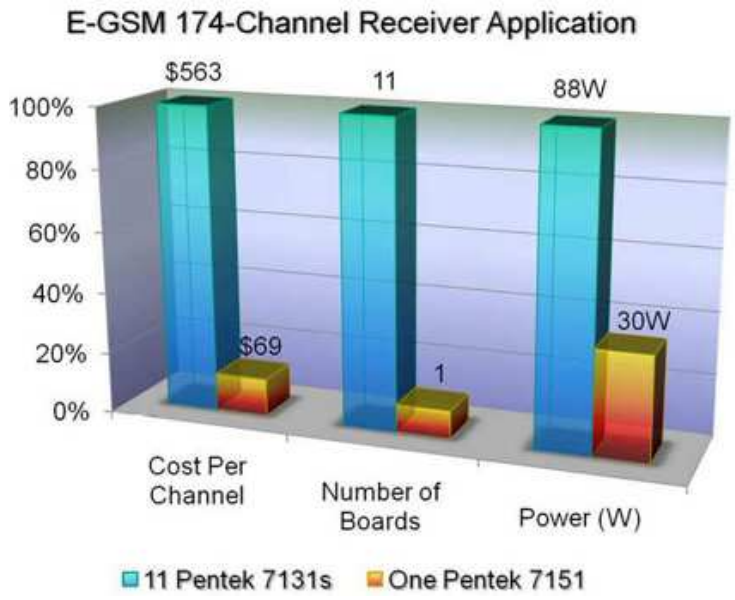

Figure 4: A comparison of cost, board count and power.

Additionally, FPGA solutions are extremely flexible since they can support vastly different signals with the simple loading of a different IP core while using the same hardware platform.

FPGA solutions are not a perfect match for all requirements. They show the greatest advantages in systems with high channel densities and, typically, narrower bandwidths. In systems with just one or two channels and bandwidths in the range of 100MHz or greater, the higher cost of the FPGAs needed can quickly exceed the cost of designing the system with a single multichannel DDC ASIC.

Again, while cost, size and power are important factors in designing a receiver system, ultimately the technical requirements may require the choice of an ASIC or FPGA solution.

Richard Kuenzler *is a Senior Design Engineer and* ***Robert Sgandurra*** *is a Product Manager at Pentek Inc.*

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