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Technology Focus

Signal Processing IP Cores

Signal Processing Rides the IP Core Wave

IP cores are proving the perfect platform for military signal processing functions. FPGA and embedded board vendors are leading the charge with a comprehensive set of solutions.

Jeff Child, Senior Editor

Like any significant idea, the idea of Intellectual Property (IP) cores has run through phases of over-hype, burst expectations, and consolidation before settling into reality. At one time, many envisioned a panacea where armies of small firms could sustain themselves by selling pieces of on-chip functions in the form of IP cores that would live merrily side by side other vendors' IP on the same chip.

While that Utopia never fully took hold, a very diverse set of IP is now available on today's advanced FPGA devices. These let system designers mix and match various computing, DSP and I/O functions on an FPGA. Rather than depending on IP from small design shops, the vast majority of those IP cores are created and owned by either the FPGA vendors themselves or licensed from microprocessor vendors. That said, FPGA vendor Xilinx has a formidable list of third-party IP core offerings through its AllianceCORE Program (Figure 1). A comparable number of third-party cores are available through the Altera Megafunction Partner Program.

For years vendors of DSP boards from the standard bus board industry have been making heavy use of that IP core technology, particularly for products targeted at communications, radar/sonar and signal intelligence. Over the past couple of years, those same board vendors have emerged as a new source of IP core technology, especially in the area of signal processing IP cores.

Perfect Fit for Military Radios

The trend toward signal processing IP cores fits perfectly into the needs of defense system designers,

Figure 3

A cooperative effort between Xilinx and independent third-party core developers, the AllianceCORE program offers a broad selection of industry-standard solutions dedicated for use in Xilinx programmable logic. Xilinx takes an active role with its partners in the process of productizing AllianceCORE products.

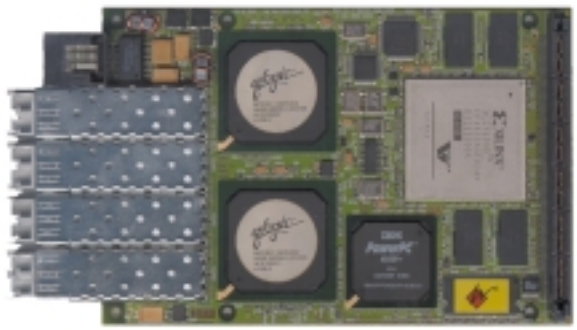

Figure 2

Annapolis Micro Systems supports its FPGA-based board products, like this Fibre Channel daughtercard, with its IP core technology via its CoreFire Design Suite. The tool combines a Graphical User Interface (GUI) with libraries of IP cores, Board Support Packages (BSPs) and a Hardware In the Loop Debugger (HILD), which allows the application programmer to operate on the conceptual, data flow level throughout the whole development process.

particularly makers of government or military radios. Using FPGAs with signal processor IP cores lets designers accommodate waveforms that are rather specialized for the military market—waveforms that aren't generally available in an ASIC. Because such waveforms are often proprietary, creating it as an IP core is more secure. In contrast, implementing the scheme as an ASIC would require it to pass through many more hands and would therefore be more difficult to keep secure.

The ease of field upgrades is another advantage of IP cores and FPGAs. Radios with an FPGA inside could be upgraded to prolong the service lifetime of the radio. As new communication schemes emerge, and as defense waveforms evolve commensurately, updates can be downloaded into the radio. During a conflict, a new communication scheme might be needed to replace one that's been compromised by the enemy. Or, conversely, if our forces acquired an enemy's communications scheme we could upgrade our radios to enable them to eavesdrop on the enemy and listen to his broadcasts.

The combination of signal processing IP cores and FPGAs offers huge performance advantages over programmable DSP solutions. Newer FPGA devices that are coming out now, like the Xilinx C2VP-50, provide 232 hardware (18x18) multipliers in silicon. Contrast that to a conventional programmable DSP like a PowerPC AltiVec G4, which has a mere 4 or 8 hardware multipliers on-chip. That's two orders of magnitude of difference. That means that where a programmable processor would have to process a complex algorithm sequentially—going through a loop of instructions—an FPGA could do it all in parallel, dramatically lowering the computation time.

Growing Selection of IP Cores

While many FPGA DSP board vendors offer IP as part of their board-level products, some are even productizing the cores themselves. A few years ago Pentek began offering a selection of FFT IP cores inside FPGAs as factory installed options on its mezzanine board products. Starting in February of this year, the company began making the IP cores available to customers directly. Pentek now has three classes of IP cores: high-performance FFTs, high-performance digital receivers and a complete pulse compression core for radar.

The cores are part of Pentek's GateFlow IP Core Library. Designed for Xilinx Virtex-II and Virtex-II Pro FPGAs, these cores take full advantage of the numerous hardware multipliers on those chips. Each core of the GateFlow IP Core Library is available separately under the standardized Xilinx SignOnce IP Project License, a multi-vendor common license for FPGA-based IP, which allows unlimited use of each core for any given project.

Mercury Computer Systems developed a back-projection algorithm as an FPGA-based IP core for a medical imag-

Figure 3

Designers can combine Megafunctions IP Cores from Altera with communications IP cores from Nova Engineering, to program the functionality of this PC/104-based Constellation board. The card's USB connectivity allows designs to be directly downloaded from a PC into the PLD and then simulated using real-time hardware.

ing application. Although back-projection is most applicable to the medical imaging market, there's been interest from the military side in back-projection techniques applied in synthetic aperture radar (SAR). The idea was implemented into a product earlier this year in the VantageRT FCN, a new design for Mercury's VantageRT PCI product family.

Annapolis Micro Systems delivers its IP core technology via its CoreFire Design Suite. Offered as a support tool for its FPGA-based board products (Figure 2), the tool combines a Graphical User Interface (GUI) with libraries of IP cores, Board Support Packages (BSPs), and a Hardware In-the-Loop Debugger (HILD). These enable the application programmer to operate at a conceptual data flow level throughout his whole development process, quickly providing correct, reconfigurable and reliable FPGA designs (see Annapolis Micro Systems article "From Algorithm to Hardware—The Great Tools Disconnect", on p. 48, October 2001, *COTS Journal*).

Focus on Comms

Specializing in communications IP cores, Nova Engineering's line of IP core offerings range from digital IF receivers and adaptive equalizers, to Viterbi decoders and numerically controlled oscillators. Nova's

PC/104-based Constellelation-20KE card (Figure 3) hosts an Altera million-gate PLD. The boards can be configured with Megafunction IP Cores from Altera's Megafunction Partner Program (AMPP), along with cores from Nova.

Targeting military communications applications like JTRS and ACN, as well as commercial wireless markets, Spectrum Signal Processing makes a line of board-level products it calls FPGA processing engines. These reconfigurable computing systems facilitate intermediate frequency (IF) processing using the Xilinx Virtex II FPGAs. The user-programmable FPGAs are supplied with a level of programming that abstracts the user from board-level glue logic. Called the "FPGA wrapper", the abstracted functions can include control of on-board buses, SDRAM, the inter-FPGA bus links and switch fabric links. That means users can configure the board without dealing with low-level hardware issues. Verilog source is supplied with the wrapper, allowing the firmware programmer to make customizations if required. ▮▮

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