C6000 vs. PowerPC for signal processing application development

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While both, C6000 DSP family and the fourth generation PowerPC processors, are capable of handling the requirements of high-throughput, and calculation intensive applications, there are inherent differences, as this article explains

Model 4295 - four MPC7410 PowerPC processors on a single-slot 6U VME board

The C6000 DSPs from TI and PowerPC G4 procerssors from Motoroa can deliver some of the highest performance processing power currently available in silicon today. And while these two processor can deliver similar benchmarks in many applications, the fact still remains that the C6000 family is based on a DSP architecture and the PowerPC is multipurpose RISC chip. With that come the inherent differences in the processing cores, I/O interfaces, software development environments and in general, the design philosophy that comes with each family.

The C6000 DSP family features VelociTI, a highly parallel architecture that allows up to eight instructions to be executed on eight functional units with every clock cycle. Each of the eight units uses a 32-bit instruction, so a 256-bit very long instruction word (VLIW) is fetched on every clock cycle. With the help of an optimizing C compiler and assembler, a user's C language application code can be "parallelized" and pipelined, to make most efficient use of the functional units. Motorola's fourth generation (G4) PowerPC architecture combines the existing RISC design found in the third generation family with the AltiVec vector parallel processing engine. The AltiVec unit operations are performed on multiple data elements by a single instruction. This is often referred to as SIMD (single instruction, multiple data) parallel processing. The unit operates on 128-bit data and supports the following data types: 16-way parallel operations for 8-bit signed and unsigned integers and characters; 8-way parallel operations for 16-bit signed and unsigned integers; 4-way parallel operations for 32-bit signed and unsigned integers and IEEE floating-point numbers. To support the AltiVec technology, 162 new instructions have been added to the PowerPC's instruction set. These new instructions fully utilize the single instruction, multiple data and vector manipulation design.

When choosing a processor, a fundamental question to ask is whether the application can be best addressed using a fixed-point or floating-point processor. The C6000 series is available in both fixed- and floating-point varieties. Fixed-point processors are identified by C62xx and C64xx, and floating-point by C67xx. The 7410 contains both fixed- and floating-point units on the same chip. Some general guidelines for making the choice between fixed- or floating-point include:

Fixed-point advantages: Fixed-point arithmetic units are less complex and require less silicon than equivalent floating-point units. Because fixed-point processors are typically lower cost than floating- point processors. They are usually available in higher CPU clock rates. In general, fixed-point architectures require less power. The advantages of using fixed-point processors can be seen in high volume, heavily embedded applications because of their lower cost and power. While additional code complexity because of scaling for fixed-point arithmetic may increase design time, in applications where the code will not need to be modified often, this additional software investment might be easily offset by the cost savings of the silicon.

Floating-point advantages: Better dynamic range can eliminate the need for scaling and error detection, reducing code complexity. Reduced code complexity usually translates to reduced product development time. The advantages of using floating-point processors can be seen in applications that require extensive floating-point arithmetic, or in custom applications where the code will continue to change and the user can exploit the faster code development effort.

An initial view of performance can be obtained by comparing clock speeds and peak processing power (see table 1). All of the processors are capable of parallel processing. Instructions per cycle, lists the minimum and maximum number of parallel instructions that can be executed during each clock cycle. Peak MIPS (millions of instructions per second) is calculated by multiplying the maximum number of instructions per cycle by the clock rate. Similarly, peak

	C6415	C6203	C6701	7410
Clock (MHz)	600	300	167	500
Instruction Per Cycle	1 – 8	1 – 8	1 – 8	1 – 3
Peak MIPS	4800	2400	1336	917
Floating-Point Operations Per Cycle	–	–	1 – 6	4
Peak MFLOPS	–	–	1000	2000

Table 1. Comparison of clock speeds and peak processing power

	C6415	C6203	C6701	7410
Program Memory (L1)	16 kB	384 kB	64 kB	32 kB
Data Memory (L1)	16 kB	512 kB	64 kB	32 kB
On-chip Cache (L2)	1024 kB	–	–	–
Total Memory	1066 kB	896 kB	128 kB	64 kB

Table 2. Comparison of on-chip memory

MFLOPS (millions of floating-point operations per second) is calculated my multiplying the maximum number of parallel floating-point operation that can be performed per cycle by the clock rate. One thing to remember when looking at MFLOPS and MIPS is that the numbers listed are peak. That assumes that compiled code can take full advantage of the parallel architecture of the processor, meaning that on every cycle, the maximum number of parallel operations are executing. Optimizing the code for the specific architecture becomes a critical factor in overall performance and the code generation tools quickly become as important as the hardware.

On-chip memory provides the fastest resource for program, data and cache memory. The larger the internal memory, the less often the processor needs to go off-chip to access slower memory for program fetches. With larger on-chip memory comes faster execution and in general higher performance. While the 7410 has a relatively small internal memory, it does support a fast, tightly coupled level 2 (L2) external cache. The L2 cache is typically 64-bit synchronous SRAM and can be as large as 2 MB (see table 2).

As processor cores become faster, the real bottleneck to performance quickly becomes the paths for data to get on and off chip. In most embedded systems the I/O requirements are as critical as the processing requirements. The C6701 has a single 32-bit external memory interface (EMIF), that can be programmed to run at processor clock speed, 167 MHz, or 1/2 of the processor clock. The C6701 can hit a maximum data transfer rate of 667 MB/sec when reading and writing to SBSRAM. The C6701 is equipped with a four-channel DMA controller to off load the data transfer tasks from the CPU (see table 3).

		C6415	C6203	C6701	7410
Number Of Buses		3	2	1	2
Bus 1	Type	EMIFA	EMIF	EMIF	MPX
	Data Width (bits)	64	32	32	64
	Bus Clock Rate (MHz)	133	150	167	133
	Bus Data Rate (MB/sec)	1064	600	667	1064
Bus 2	Type	EMIFB	XBUS	–	Cache
	Data Width (bits)	16	32	–	64
	Bus Clock Rate (MHz)	133	150	–	500
	Bus Data Rate (MB/sec)	266	600[1]	–	4000[1]
Bus 3	Type	PCI	–	–	–
	Data Width (bits)	32	–	–	–
	Bus Clock Rate (MHz)	33	–	–	–
	Bus Data Rate (MB/sec)	132	–	–	–
DMA Channels		64	4	4	0

Note: These are theoretical data bus rates and will be limited my the speed of available memory components.

Table 3. Comparison of architecture for external memory

While the C6203 has a higher processor clock speed (300 MHz), the EMIF always operates at 1/2 of the processor clock (150 MHz). In addition to the EMIF, the C6203 has a second 32-bit expansion bus (XBUS) for I/O. It provides an interface to a variety of peripherals, FIFOs, PCI bridges, and other external devices. The EMIF, XBUS combination makes the C6203 an ideal match for real-time streaming applications where the XBUS handles streaming data and the EMIF provides program and random data access. The C6203 also is equipped with a four-channel DMA controller. The C6415's three bus architecture includes: a 64-bit EMIFA bus running at 133 MHz, a 16-bit EMIFB bus also running at 133 MHz, and a 32-bit / 33 MHz PCI Bus. The C6415's DMA controller has been upgraded from the four channels available on the C62xx and C67xx family to a 64-channel controller.

The 7410 also has dual buses. The primary MPX bus is a 64-bit architecture and supports bus clock speeds up to 133 MHz. Unlike the C6000, the 7410 primary bus requires a companion chip, sometimes called a system or node controller, to interface between the MPX bus and to memory and I/O resources. Numerous types of system controllers are available from different manufacturers. Because the system controller is responsible for all data transfers to off-chip resources, the selection of the appropriate controller becomes a critical system design decision. The 7410's secondary bus provides a dedicated interface for 64-bit SDRAM L2 cache memory. The 7410's best performance is achieved by operating out of L2 and up to a 2 Mbyte cache is supported.

Signal processing systems can be developed with or without an operating system. Real time operating systems provide the application developer with a variety of sophisticated features, but some of these features do come with a cost.

■ Advantages of using an operating system: An OS dynamically schedules tasks, as the application requires. In large systems where tasks can occur at indeterminate times, this can be a complex process. OSs allow the user to prioritize each task based on the requirements of the application. As each task is initiated, the OS can choose to run it, queue it up behind another higher priority task, or suspend a lower priority task to allow it to run. The OS allocates and de-allocates resources like memory, and handles system level services like communication mechanisms and interrupt handling, as each task requires. In general, some of the major advantages of using an OS can be seen in large mul-

tiprocessor systems where it can organize and optimize data flow and task management, and in real-time systems where task scheduling can become critical.

■ Advantages of not using an operating system: OSs typically introduce latency when the software needs to respond to hardware interrupts. This is due to the time needed to switch tasks. While many OSs are actually very good at performing in real-time applications, latency can be a problem in closed loop control systems where the software must very quickly respond to system changes and provide a response. In these systems, a "bare metal" solution using no OS can very often provide superior performance. OSs can cause the run-time code size to increase due to the additional functions linked into the code by the OS. Some OSs require a run-time license to be purchased for each node that runs the OS. This can introduce additional cost to the system.

C6000s and DSPs in general, have been successfully used in applications with and without an OS. DSP programmers have been typically handling data flow and processing without an OS in applications where data rates and the time it takes for processing tasks are deterministic. Conversely, in applications with multiple asynchronous data streams that may have widely varying rates and where processing times can also vary depending on the data set or external conditions, an OS can be extremely useful for scheduling processing tasks to maintain real-time performance. The operating system most commonly used on the C6000 is TI's license free DSP/BIOS and is included with Code Composer Studio. In embedded PowerPC application the most common OS is Wind River's VxWorks, a real-time, scalable OS. VxWorks is licensed on a per node basis.

The premier C6000 code development tool is Texas Instrument's Code Composer Studio, a complete development environment that runs on Windows workstations The most common development tools for embedded applications on the PowerPC are Wind River's Tornado tools, a complete development environment designed to work with VxWorks. In addition to the application development tools, a board support package (BSP) is also recommended for code development. This is usually provided by the hardware manufacturer and includes hardware support specific to the architecture of the board. For C6000 development, Pentek provides ReadyFlow Board Support Libraries. These consist of C-callable libraries for processor I/O module initialization, set-up, control and operation. For PowerPC based development, Pentek provides the functionality of ReadyFlow in a traditional board support package with device drivers, specifically for VxWorks. ■