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FPGAs Revolutionize Mezzanine Boards

FPGAs are changing the architectures of mezzanine cards and extending their functions. Using them to implement real-time signal processing, high-level local control functions and high-speed interfaces is revolutionizing both mezzanine and system design.

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For many decades, mezzanine boards, also called daughter cards, have proven to be an essential and highly effective strategy for configuring embedded systems to meet the specific needs of a wide range of applications. System designers regularly exploit their modularity by using them to add various types of interfaces to processor boards, thus creating custom systems from standard COTS products. In the past, mezzanine boards consisted mainly of specialized connectors, driver/receiver circuits, modems, UARTS and ASICs dedicated to a particular interface. Board programmability was limited to a few fixed, pre-defined functions.

In recent years, FPGAs have dramatically changed the architectures and extended the functions of mezzanine boards in many different ways. Not only can FPGAs be configured to implement numerous electrical interface standards, they can also implement a variety of protocol engines. In this way, one FPGA-based product can replace several legacy products. Through reconfiguration, that FPGA-based product can also be adapted to new standards and protocols to help safeguard against product obsolescence, at the level of both board and deployed system.

Although these are laudable gains, the real benefits FPGAs bring to mezzanine boards stem from their ability to implement real-time signal processing, high-level local control functions and high-speed interfaces. By doing so, FPGAs have revolutionized both mezzanines and embedded system design.

Advanced Digital Signal Processing Functions

Data rates at the front end of the mezzanine board are often quite high, especially for new network and storage interface standards with multiple channels and gigabit signaling rates. For these standardized interfaces, such as between a host processor and a communication channel like Ethernet, an ASIC is usually the best solution for handling the necessary protocol tasks.

However, acquisition of wideband analog signals for radar, satcom and communication systems requires A/D converters operating at sampling rates of 100 MHz and often much higher.

Because of the variety of signal types and frequency characteristics, signal processing tasks tend to be quite unique for each system. As a result, there is no standard ASIC available that can handle a wide range of applications.

This forces the system designer to find the best way to process the tremendous amount of data generated by these data converters. If that data cannot be handled on the mezzanine card, the task of processing it must fall squarely on the shoulders of the CPU or DSP board that hosts the mezzanine card. But performing these data extraction and protocol processing tasks at the interface data rates often consumes a major portion of a processor's horsepower, thereby increasing the number of processors and causing an immediate impact on system size and cost.

Fortunately, FPGAs provide a nearly ideal solution to this dilemma. Consistent with advances in silicon technology, each new generation of FPGA devices delivers faster speeds, improved density, larger memory resources and more flexible interfaces. One major watershed event for FPGAs was the recent incorporation of hardware multipliers. Because multiplication is an essential operation in nearly every digital signal processing algorithm, hardware multipliers have afforded FPGAs a strategic entry into DSP applications.

Some of the most popular functions of mezzanine boards include digital downconversion for narrowband communication systems, FFT processing for radar applications and coding/decoding for broadband wireless networks. These tasks are tailor-made for FPGAs: they are well-defined, processing-intensive tasks that can take advantage of the parallel structures within the FPGA to achieve real-time processing at rates matching those of high-speed data converters.

Unlike general-purpose processors that must perform multiplications serially, FPGAs can be configured to execute hundreds of multiplications in parallel. This makes them highly complementary companions to programmable CPUs and DSPs, which are far better at handling more complex high-level tasks executing through a C program.

Fortunately, because of their ability to handle diverse logical and electrical interface signals, the natural place for FPGAs on mezzanine cards is between the high-speed converters and the mezzanine bus. This is also precisely the best point for front-end DSP processing, further fueling the adoption and acceptance of FPGAs for performing signal processing on mezzanines.

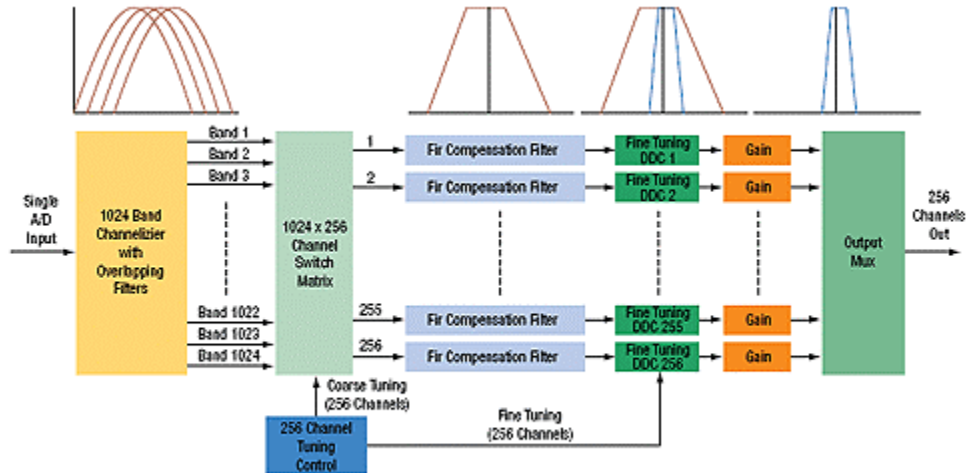


Figure 1 An FPGA-based 256-channel narrowband digital down-converter exploits parallelism of DSP resources. FPGAs can be used to implement advanced signal processing functions at the front end of the mezzanine board.

For example, a 256-channel narrowband digital down-converter IP core can fit within a single Virtex-II Pro FPGA (Figure 1). When these cores are installed on FPGA-based PCI mezzanine card (PMC) modules, the modules can achieve a tremendous channel density with all frequency translation and baseband filtering performed ahead of the host processor. In this example, not only does the FPGA offload the host CPU, it also replaces 64 four-channel digital down-converter ASIC chips, which would not have fit on the PMC.

Complex Local Control Functions

As mezzanine boards acquire higher-level functions by virtue of newly acquired DSP capabilities, the need to control those functions in real time becomes more critical. For example, a scanning communications receiver may need to monitor the airwaves for unknown signal frequencies and tune those signals for acquisition and storage. If the host processor is burdened with this task, reaction time may be compromised by the operating system or execution of other tasks. Therefore, for tough real-time constraints on mezzanine boards it is often necessary to implement the control functions on the mezzanine itself.

Two traditional control solutions afforded by programmable logic are state machines and simple combinatorial logic. These can be highly effective for simpler functions but can be difficult to develop as control algorithm complexity increases.

To address these situations, a completely new type of FPGA resource is now available. One or two PowerPC RISC controllers are embedded within Virtex-II Pro FPGA family devices. Provision for external flash memory allows the controller to boot a control program into that memory and execute using either internal or external RAM. A software tool suite includes libraries, compilers, assemblers and debuggers to simplify development of complex programs written in C.

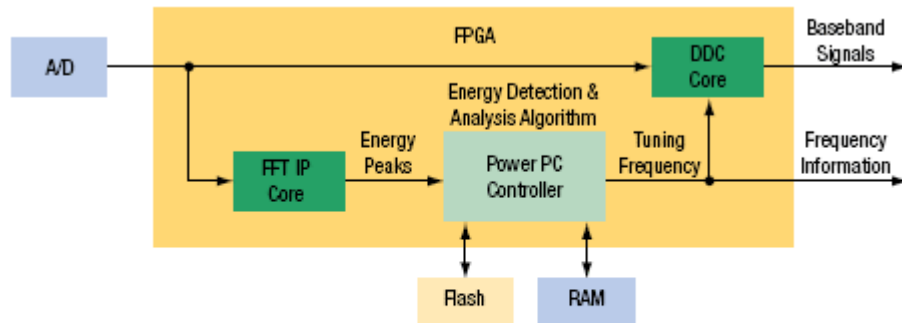


Figure 2 Replacing multiple system boards, a single FPGA-based mezzanine module functions as a tracking receiver that automatically tunes frequency-agile signals.

For example, a complete tracking receiver uses an embedded PowerPC RISC controller (Figure 2). Samples from the A/D converters are processed with an FFT IP core, delivering frequency bin output energy levels to the PowerPC for analysis. The signal frequency deemed worthy of tracking is identified and the appropriate tuning commands are sent to the digital down-converter IP core to down convert that signal. If the frequency of the signal periodically shifts to thwart reception, the detection algorithm adjusts the tuning frequency to implement an adaptive tracking function. The baseband output signal and the latest tuning information are delivered across the mezzanine interface to the host processor.

In this example, a single mezzanine module assumes the role of an entire tracking system that previously might have required several system boards for implementation.

New Gigabit Serial Interfaces

The data rate demands of high-speed networks, advanced RISC and DSP processors, A/D and D/A converters, video devices, storage devices, communication channels and other peripherals have swamped the traditional backplanes and bus architectures that have served embedded systems admirably for more than 30 years. Coming to the rescue are new gigabit serial links and several protocol standards that move data at rates of at least 10 times faster.

Methods of adapting these new links to mezzanine boards for embedded systems are spelled out in the VITA 42 standard, also known as XMC. As an extension to the widely used PMC, XMC defines two new connectors that join the mezzanine board to the host or carrier board. Each connector provides up to 20 differential gigabit signal paths, 10 in each direction. One popular implementation calls for two 4x full-duplex links per connector. With today's serial bit rates of 3.125 GHz, this translates into 2.5 Gbytes/s in each direction for each connector. This is a big increase from the few hundred megabytes per second common for PCI bus transfers.

Once again, FPGAs are the primary enabling technology for these new links. Recent FPGA offerings from Xilinx feature gigabit transceivers called RocketIO, while Altera's counterparts are the Stratix-GX Multi-Gigabit Transceivers (MGTs). Behind these physical interface drivers are channel encoders and decoders that perform serial/parallel conversion so that data and clock are combined in the signaling on each differential pair over the external serial channel. Both receive and transmit circuitry is built into the FPGA and is commonly referred to as serializer/deserializer (SERDES).

A protocol engine within the FPGA interfaces with the SERDES to correctly process packets, header information, control functions, error detection and correction and payload data format. Since each switched serial fabric standard has its own protocols and rules, FPGAs offer excellent flexibility by allowing users to install the appropriate IP core protocol engine. The strategy makes FPGA-based XMC modules truly fabric-agnostic and allows one hardware design to be deployed in several different fabric environments. Various sub-specifications for VITA 42 define the implementation of popular switched fabric standards (Figure 3).

VITA Std	Description	Type	J15 Only Lanes x Clock	Transfer Rate	J15 and J16 Lanes x Clock	Transfer Rate
42.1	Parallel RapidIO	Par	8 x 500 MHz	1 GB/sec	16 x 500 MHz	2.0 GB/sec
42.2	Serial RapidIO	Ser	8 x 3.125 GHz	2.5 GB/sec	16 x 3.125 GHz	5.0 GB/sec
42.3	PCI Express	Ser	8 x 2.5 GHz	2.0 GB/sec	16 x 2.5 GHz	4.0 GB/sec
42.4	HyperTransport	Par	8 x 800 MHz	1.6 GB/sec	16 x 800 MHz	3.2 GB/sec
42.5	Aurora	Ser	8 x 3.125 GHz	2.5 GB/sec	16 x 3.125 GHz	5.0 GB/sec

Figure 3 VITA 42 XMC sub-specifications define specific implementations for widely used fabrics. Popular serial clock rates and the resulting transfer rates in each direction are shown for either one (J15) or two (J15 and J16) XMC connectors.

The Xilinx Aurora protocol, defined for use in XMC as VITA 42.5, is a lightweight link-layer protocol that does not implement the packet routing and switching features of the other more complete protocols. However, it has many advantages: the IP core is much smaller, it is available free from Xilinx, there are no associated runtime licensing fees and the reduced packet overhead makes data payload transmission more efficient. Since many mezzanine applications can be satisfied with this type of dedicated point-to-point connection, Aurora becomes a very attractive option. A similar protocol, called SerialLite, is offered by Altera.

Putting It All Together

Pentek's Model 7140 dual-channel, software radio transceiver XMC mezzanine module illustrates how this new FPGA technology has been deployed (Figure 4). In this mainstream COTS product, a Virtex-II Pro FPGA acts as the interface to all data converter, ASIC, memory and interface resources on the module. With 232 hardware multipliers, this FPGA easily accommodates the 256-channel digital down-converter IP core, for example. The two PowerPC processors with attached SDRAM and flash memories support the tracking receiver application. The RocketIO interface implements the direct connection to the XMC connector for the dual 4x serial fabric ports with a combined data rate capacity of 2.5 Gbytes/s.

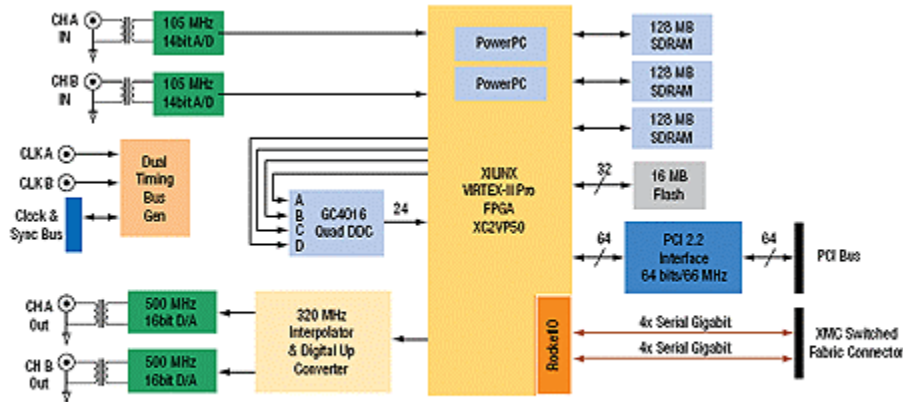


Figure 4 In Pentek's Model 7140 dual-channel software radio transceiver XMC mezzanine module, an FPGA acts as the interface to data converter, ASIC, memory and interface resources.

Since all of these FPGA features are now standard resources found on most later-generation devices, new mezzanine board designs can easily take advantage of them without incurring additional cost. This ensures the rapid adoption of these resources for embedded systems being developed today and also helps establish standards and methodology for future system architectures.

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