The Journal of Military Electronics & Computing

April 17, 2017

JEFF'S PICKS: A-D Processing Board Family Boasts Scalable, Flexible Architecture

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Today's military digital conversation applications rely heavily on analog-to-digital converters (ADCs), digital-to-analogy converters and FPGAs. The evolving trend in recent years is to perform digital conversion as soon along the signal chain as possible. High-bandwidth A/D converters with high sampling rates must connect to extremely fast data transfer paths to store and process data with triggering or gating circuitry to digitize pulse waveforms at precisely the right time. To feed those needs, board vendors continue to push the barriers with solutions with ever faster ADCs and more sophisticated FPGAs. A rich selection of digital receiver products combine ADCs and FPGAs on one VME, VPX, or PCI Express board. Other solutions pair a FPGA processing engine with mezzanine-based ADCs using form-factors like FMC or XMC.

For this month's Jeff's Picks section *COTS Journal* evaluated several ADC and DAC conversion products based on three aspects: technology leadership, design innovation and market relevance. The winning product is the PVP-7xx family of A-D processing boards from Star Communications (Figure 1). This family is scalable from 1 to 4 A/D channels and from 1 to 4 FPGAs (Xilinx high-end Virtex-7 XC7VX485T). According to the company, the product is based on a small, multi-channel A-D component that uses high-speed serial links to route sample data to FPGAs on the board.

Figure 1. *Jeff's Pick is the PVP-7xx family of A-D processing boards from Star Communications. It's scalable from 1 to 4 A/D channels and from 1 to 4 FPGAs (Xilinx high-end Virtex-7 XC7VX485T). Programmable sample rates provide flexibility.*

Each HSSL link consists of a differential pair operating up to 4 Gbits/s, and protected using SONET scrambling and Hamming error correcting codes. Use of HSSL has several PCB design benefits. First, board area is minimized because each differential pair replaces an entire data bus. Second, routing is simplified because careful length matching of large data busses and their clocks is not needed. Finally, the HSSL is directly compatible with Giga-bit transceivers available on Xilinx Virtex-7 FPGAs. This makes it easy to route all sample data is to every FPGA installed on the board.

Flexible, Programable Design

The PVP features a programmable sample rate, based on a clock generator IC manufactured by Analog Devices. Design benefits include small footprint, flexible referencing options, and a low-phase noise sample clock with programmable frequency. Total board area devoted to clock generation is only 22 x 30 cm. An onboard frequency reference is included having ±2.5 ppm stability over time, frequency, and temperature. Alternatively, customers can supply an external reference anywhere from 1 PPS to 250 MHz in a variety of formats. The board automatically recognizes and switches to the external reference if present. Using the selected reference, the sample clock can be programmed anywhere between 100 MHz to 250 MHz in sub-Hertz steps.

The technology and design innovations result in an A-D product that is small yet very flexible. Flexibility allows the product to support a common architecture that can acquire and process data at the edge of multiple systems. This in turn provides the usual benefits of a common

architecture, including scalability, code re-use, common operating procedures, and reduced logistic support. A single board can handle up to four receive channels the intermediate frequency (IF) design allows multiple RF on one board. Front-end bandwidth allows multiple IFs simultaneously—for example 70 and 140 MHz. The board's programmable sample rate allows users to choose their IF frequency. And the sample rate can be chosen so that it relates to one's final application which means less filtering is needed. Sample data is synchronized across all receive channels and FPGAs. And because the architecture is scalable, users can scale from one to four FPGAs to scale processing capability to match what's required.

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…And the Runners Up:

8-Channel A/D XMC Provides Radar Phased-Array Solution

Pentek's Model 71131 is an eight-channel, 250 MHz XMC module featuring 16-bit A/Ds with programmable multiband digital down converters (DDCs) (Figure 2). It's a member of Pentek's Jade family of high-performance data converter XMC modules based on the Xilinx Kintex Ultrascale FPGA. The board is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP. The eight channels make it especially beneficial for multi-channel phased array platforms in defense and weather radar applications where the cost per channel can be substantially reduced.

Figure 2. *The Model 71131 is an eight-channel, 250 MHz XMC module featuring 16-bit A/Ds with programmable multiband digital down converters (DDCs).*

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. The Model 71131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Pentek's Navigator Design Suite was designed from the ground up to work with Pentek's Jade architecture and Xilinx's Vivado Design Suite. The Navigator Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and Navigator BSP (Board Support Package) for creating host applications.

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