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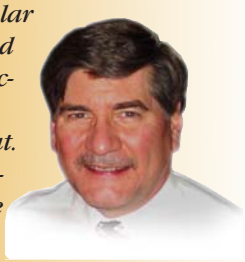
PCI Express: Switched Serial Fabric for the PCI Bus

In This Issue

- A switched serial fabric system connects devices together to support multiple simultaneous data transfers. More in the feature article.

"Pentek's new product line leverages the PCIe technology for our most popular designs and boosts effective data throughput. These high-density PCIe solutions specifically target software radio, radar, telemetry and signal intelligence applications"



Rodger Hosking, Pentek Vice President and Cofounder

- **Product Focus:** Model 7741 Transceiver Click here
- **Product Focus:** Model 7742 Transceiver Click here
- **Product Focus:** Model 7750 200 MHz, 16-bit A/D Click here
- **Product Focus:** Model 7751 256-channel DDC Click here
- **Product Focus:** Model 7752 32-channel DDC Click here

Free Technical Resources

New edition of the *High-Speed Switched Serial Fabrics Handbook:* pentek.com/go/pipeserhb

New edition of the *SDR Handbook:* pentek.com/go/pipesdrhb

New edition of the *FPGAs for Software Radio Systems Handbook:* pentek.com/go/pipefpgahb

New edition of the *High-Speed A/Ds Handbook:* pentek.com/go/pipecrithb

Introduced by Intel in 2004, PCI Express is a bidirectional serial link capable of high-bandwidth data transfers. Designed to replace the more limited PCI expansion bus, PCI Express supports enhanced features such as power management, hot-swappable devices, and has the ability to handle both host-directed and peer-to-peer data transfers. PCI Express can also emulate network environments by sending data between two points without routing it back and forth through the host chip.

Enabling greater bandwidth and performance, PCI Express helps simplify board design and is scalable for future increases in processor speeds and advances in high-performance computing and embedded systems.

Upgraded in 2007, PCI Express 2.0 doubled the data transfer rate over its predecessor for a transfer rate of up to 16 gigabytes per second for a 32X PCIe channel. Providing backwards compatibility with version 1.0, PCI Express 2.0 provides scalable performance, higher bandwidth, lower overhead and lower latency data transfers.

High-Speed Switched Serial Interfaces

A switched serial fabric system connects devices together to support multiple simultaneous data transfers, usually implemented with a crossbar switch. Using differential signaling, data is sent over a pair of wires at a fixed bit rate such as 1.0 GHz, 2.5 GHz, 3.125 GHz, 5.0 GHz, etc.

The clock, data, and data word framing are encoded into the serial stream, usually with 8B10B coding. Ten bits of serial transmission deliver eight bits of data. The extra two bits maintain synchronization, framing, and DC line balance.

The Serializer shown in Figure 1 encodes clock, frame, and eight bits of data into a 10-bit stream. The Deserializer decodes the 10-bit stream into clock, frame, and eight bits of data. These two functions are usually combined into one device for full duplex operation, known as the SERDES (SERializer/DESerializer).

Serial Data Rates

The raw speed of serial fabrics is governed by three factors:

- The serial bit clock frequency
- The inherent 8B10B channel encoding efficiency of 80%
- The number of lanes or parallel bit streams ganged together in the interface.

Since there are 8 bits per byte, the peak rate expressed in MB/sec becomes the serial rate ➤

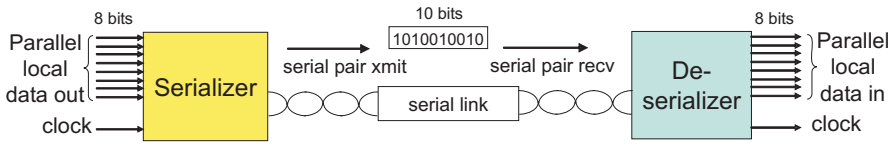


Figure 1. Switched Serial Fabric System

	Peak Rates for Specified Number of Bit Lanes			
Bit Clock	**1X**	**4X**	**8X**	**16X**
1 GHz	100 MB/sec	400 MB/sec	800 MB/sec	1.6 GB/sec
2.5 GHz	250 MB/sec	1.0 GB/sec	2.0 GB/sec	4.0 GB/sec
3.125 GHz	312 MB/sec	1.25 GB/sec	2.5 GB/sec	5.0 GB/sec
5.0 GHz	500 MB/sec	2.0 GB/sec	4.0 GB/sec	8.0 GB/sec

Table 1. Serial Data Rates

PCI Express: Switched Serial Fabric for the PCI Bus

expressed in GHz, times the number of lanes, divided by 10:

Peak Rate (MB/sec)=(Serial Rate•Lanes)÷10

Table 1 on the previous page shows the transfer rates for each link for 1.0, 2.5, 3.125 and 5.0 GHz clocks. The defined clock rates for PCIe 2.0 are 2.5 GHz and 5.0 GHz. With four bit lanes or 4X, the peak transfer rate in each direction with a 2.5 GHz clock is 1.0 GB/sec. With 16X and 5.0 GHz clock, the peak transfer rate reaches 8.0 GB/sec.

The PCI Express Bus

Conceptually, the PCIe bus can be thought of as a 'high-speed serial replacement' of the older parallel PCI/PCI-X bus. At the software level, PCIe preserves compatibility with PCI: a PCIe device can be configured and used in legacy applications and operating systems which have no direct knowledge of PCIe's newer features. In terms of bus protocol, PCIe communication utilizes point-to-point switched serial links.

If you bought a desktop PC with Windows OS in the last couple of years, it most likely came with a PCIe graphics card.

This development led to the rapid acceptance of PCIe at the consumer level, as the only bus that could accommodate increasingly faster graphics speeds. The high-bandwidth PCIe interface and fast dedicated graphics board memory made the better PC graphics possible.

Inside a PCIe PC

Looking inside a desktop PCIe PC we see the familiar motherboard, part of which is shown in Figure 2. At the top of the photo, we see the two familiar PCI connectors where you'd find most of the legacy PCI expansion cards, such as sound or 100BaseT Ethernet.

Next to these PCI connectors are two small 1X PCIe connectors and at the bottom of the photograph we see a PCIe 16X connector. This is where the video card or the Pentek full-length PCIe board shown in Figure 3 plugs in.

A PCIe card will fit into a slot of its physical size or bigger. It will not fit into a smaller PCIe slot. Some slots use open-ended sockets to permit physically longer cards and will negotiate the best available electrical connection. The number of lanes actually connected to a slot may also be less than the number supported by the physical slot size. An example is an 8X slot that actually only runs at 1X; these slots will allow any 1X, 2X, 4X or 8X card to be used, though only running at the 1X speed. The advantage gained is that a larger range of PCIe cards can still be used without requiring the motherboard hardware to support the full transfer rate, thereby keeping design and implementation costs down.

Figure 2. PCIe PC Motherboard

PCIe to PCI bridging

A PCI to PCIe bridge translates PCIe packets back into regular PCI signals, and allows a legacy PCI device to be plugged into a PCIe system. This bridging can happen anywhere, on the motherboard or on the card itself.

Some companies took this approach with their first-generation PCIe cards. There's a PCIe-to-PCI bridge embedded on the card, which means that the card itself is still a "PCI" card even though it fits into a PCIe slot. Other companies have cards that support PCIe natively and therefore don't need the bridge chip.

These bridges do not make any difference as far as PCIe operation is concerned. As a result, they allow the adaptation of legacy cards in PCIe systems at reduced risk and development cost.

Pentek and PCI Express

Three months ago, Pentek entered the PCI Express market by introducing a family of full-length PCIe boards, each offered in single- and dual-resource versions.

Five products are offered as follows:

- Model 7741: SDR Transceiver
- Model 7742: Multichannel Transceiver
- Model 7750: Quad 200 MHz, 16-bit A/D
- Model 7751: 256-channel DDC
- Model 7752: 32-channel DDC

The rest of this issue is dedicated to describing in some detail these new additions to the growing Pentek product line.

Coming soon:

- Model 7753 2/4-channel DDC

Also coming soon:

- A full complement of half-size PCIe cards of these products. Half-size cards support single-resource versions only. ❑

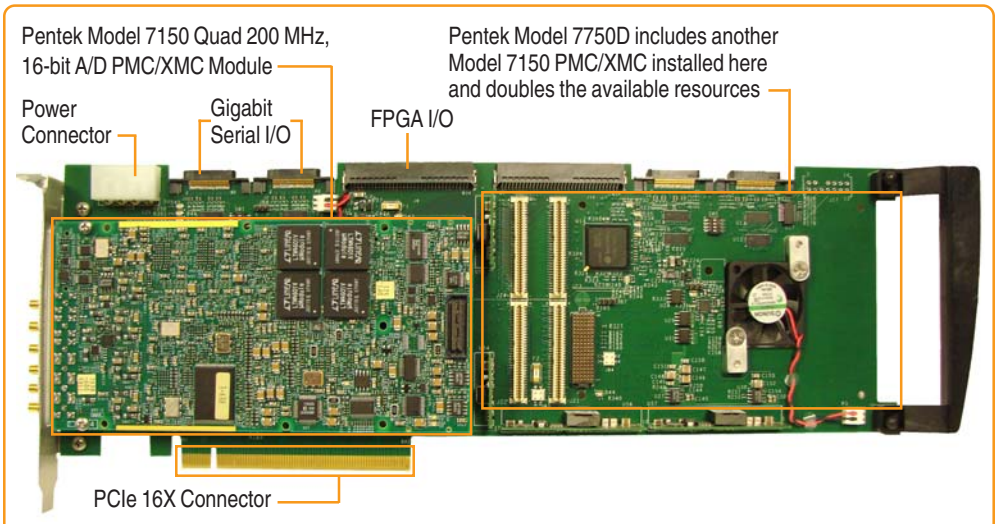


Figure 3. Pentek Model 7750 Full-Length PCI Express Card

Product Focus

Models 7741, 7741D

Dual/Quad Multiband Transceiver with FPGAs - PCIe

Features

- Two or four 125 MHz, 14-bit A/Ds; two or four 500 MHz, 16-bit D/As
- Four or eight DDCs (downconverters) and one or two DUCs (upconverters)
- Up to 1 GB of DDR SDRAM
- One or two Xilinx Virtex-II FPGAs
- Input signal bandwidths to 50 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- Up to 2.56 seconds of delay or data capture at 100 MHz
- Optional factory-installed IP cores available

Model 7741D shown

ReadyFlow Board Support Package GateFlow

General Information

Model 7741 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It is available with either two A/D and two D/A converters (Model 7741) or four A/D and four D/A converters (Model 7741D), and is capable of bandwidths to 50 MHz and above. It attaches directly to motherboards with full length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two or four full-scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into the LTC2255 14-bit 125 MHz A/Ds. The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

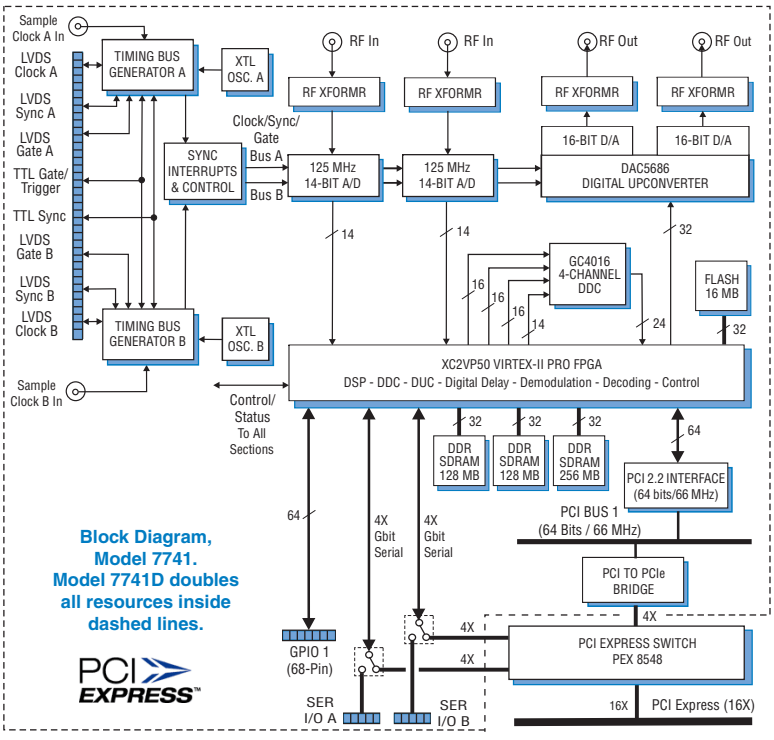
Digital Downconverter

The 7741 features one or two TI/Graychip GC4016 quad DDCs, each accepting either four 14-bit or three 16-bit digital inputs from the FPGA which determines the source of GC4016 input data. These sources include the A/Ds, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Digital Upconverter

A TI DAC5686 digital upconverter and dual D/A is attached to each FPGA, accepting baseband real or complex data streams with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.



Block Diagram, Model 7741. Model 7741D doubles all resources inside dashed lines.

Virtex-II Pro FPGAs

One or two Xilinx XC2VP50 Virtex-II Pro FPGAs serve as control and status engines with data and programming interfaces to each of the on-board resources including the A/D converters, DDCs, DUCs, and D/As.

PCIe Interface

The 7741 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides 16X wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two 4X PCIe connections provided to each FPGA, as well as one 4X connection to each 64-bit PCI interface.

For more information and price quotation on the Models 7741 or 7741D, go to: pentek.com/go/pipe7741. ❑

Product Focus

Models 7742, 7742D

Multichannel Transceiver with Virtex-4 FPGAs - PCIe

Features

- Four or eight 125 MHz, 14-bit A/Ds; one or two 500 MHz, 16-bit D/As
- One or two DUCs (upconverters)
- Up to 1.5 GB of DDR SDRAM
- Two or four Xilinx Virtex-4 FPGAs
- Input signal bandwidths to 50 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- Optional factory-installed IP cores available
- Complete software radio interface solution

Model 7742D shown

ReadyFlow Board Support Package GateFlow

General Information

Model 7742 is a multichannel data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter (Model 7742), or eight A/Ds with two upconverters and D/As (Model 7742D). It attaches to motherboards with full-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF transformer-coupled inputs on front panel MMCX connectors at +10 dBm into 50 ohms into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

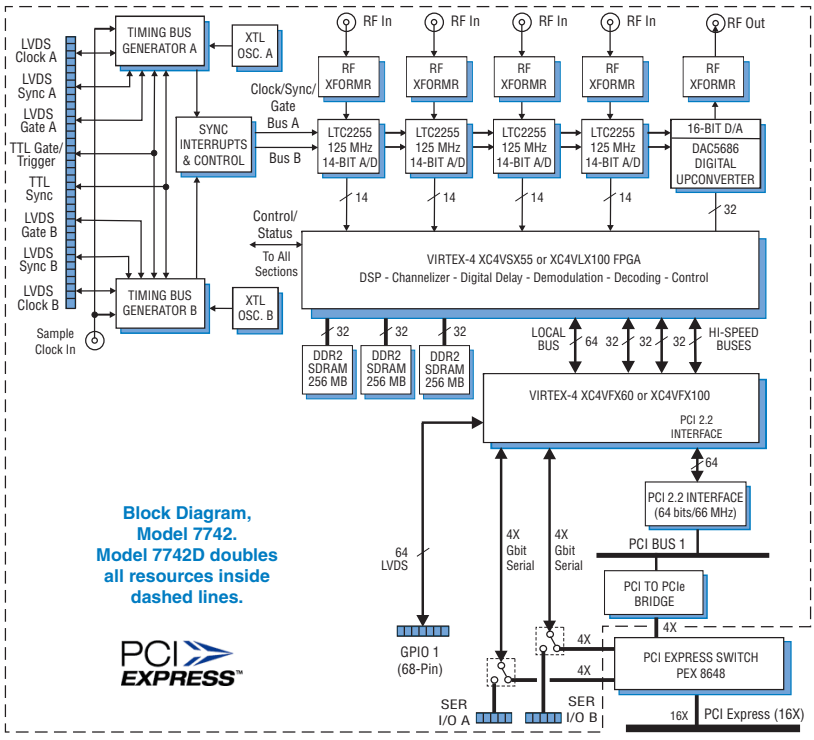
Digital Upconverter and D/A

The 7742 features one or two TI DAC5686 DUCs with D/As. Each accepts a baseband real or complex data stream from its attached FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

The 7742 architecture includes two or four Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.



Block Diagram, Model 7742. Model 7742D doubles all resources inside dashed lines.

PCI EXPRESS™

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to each SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface.

PCI Express Interface

The 7742 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides 16X wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two optional 4X PCIe connections to each SX55/LX100 FPGA, and one 4X connection to each 64-bit PCI interface.

For more information and price quotation on the Models 7742 or 7742D, go to: pentek.com/go/pipe7742. ❑

Product Focus

Models 7750, 7750D

Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCIe

Features

- Four or eight 200 MHz, 16-bit A/Ds
- Two or four Xilinx Virtex-5 FPGAs
- Up to 3 GB of DDR2 SDRAM
- Up to 5.12 seconds of delay or data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- Complete software radio interface solution

Model 7750D shown

ReadyFlow Board Support Package GateFlow

General Information

Model 7750 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features either four 200 MHz, 16-bit A/Ds (Model 7750) or eight A/Ds (Model 7750D). These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7750 attaches to motherboards with full length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

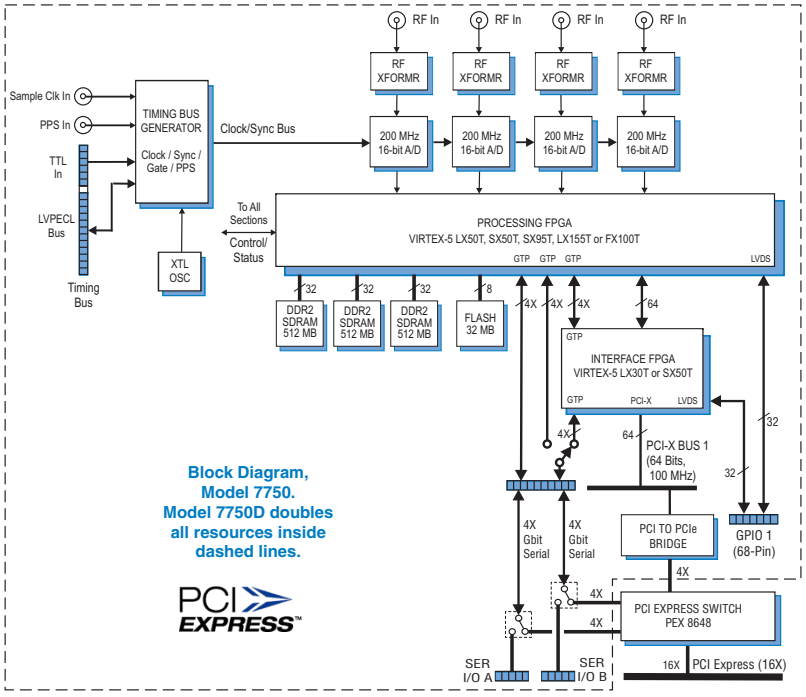
The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7750 architecture includes two (Model 7750) or four (Model 7750D) Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

There are two FPGA types on the 7750: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable I/O and clock, gate and synchronization circuits.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.



Block Diagram, Model 7750. Model 7750D doubles all resources inside dashed lines.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to each processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

PCI Express Interface

The 7750 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides 16X wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two 4X PCIe connections provided to each FPGA, as well as one 4X connection to each 64-bit PCI-X interface.

For more information and price quotation on the Models 7750 or 7750D, go to: pentek.com/go/pipe7750. ❑

Product Focus

Models 7751, 7751D

256- or 512-Channel DDC with Four or Eight 200 MHz, 16-bit A/Ds - PCIe

Features

- 256 or 512 narrowband DDC channels
- Four or eight 200 MHz, 16-bit A/Ds
- Independent tuning for each channel
- DDC Decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters with 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

Model 7751D shown

ReadyFlow Board Support Package

General Information

Model 7751 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features either four 200 MHz 16-bit A/Ds (Model 7751) or eight A/Ds (Model 7751D). Each bank of four A/Ds is supported by a high-performance 256-channel installed DDC IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

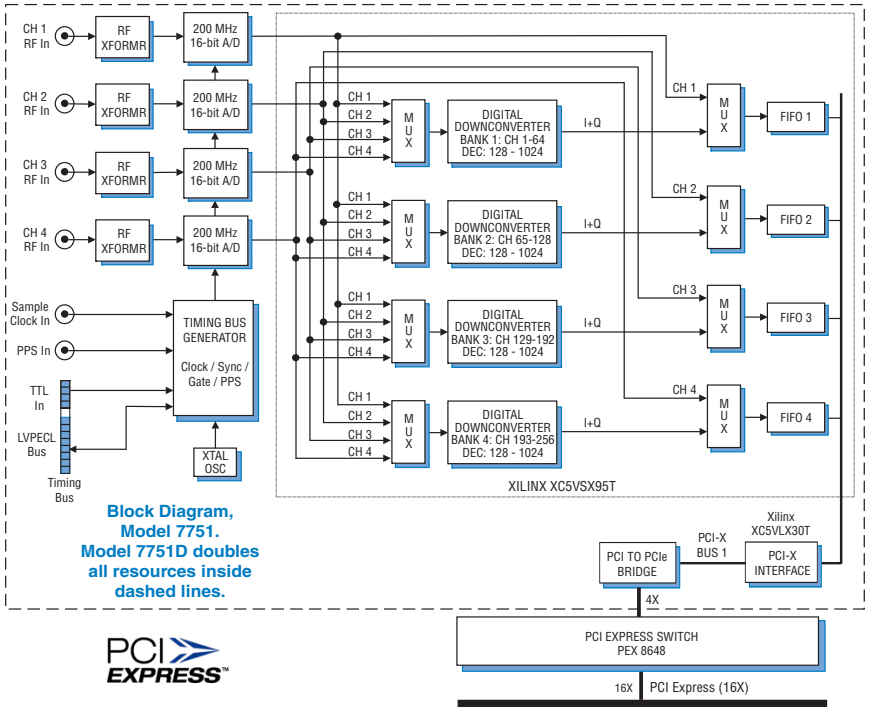
The 7751 attaches to motherboards with full length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/Ds. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

Each of the Model 7751 SX95T FPGAs employs an advanced FPGA-based DDC engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the attached four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.



Block Diagram, Model 7751. Model 7751D doubles all resources inside dashed lines.

PCI EXPRESS

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank selectable from 0 to 64.

Output Multiplexers and FIFOs

Four output MUXs in each SX95T FPGA can be independently switched to deliver either A/D or DDC data into each output FIFO. This allows users to view either wideband A/D data or narrowband DDC data, depending on the application.

For more information and price quotation on the Models 7751 or 7751D, go to: pentek.com/go/pipe7751. ❑

Product Focus

Models 7752, 7752D

64- or 128-Channel DDC with Four or Eight 200 MHz, 16-bit A/Ds - PCIe

Features

- 32 or 64 DDC channels in banks of eight channels
- Independent 32-bit tuning for all channels
- Decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters with 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- Clock/sync bus for multiboard synchronization

Model 7752D shown

ReadyFlow Board Support Package

General Information

Model 7752 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds (Model 7752) or eight A/Ds (Model 7752D). Each group of four A/Ds is supported by a high-performance 32-channel installed DDC IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

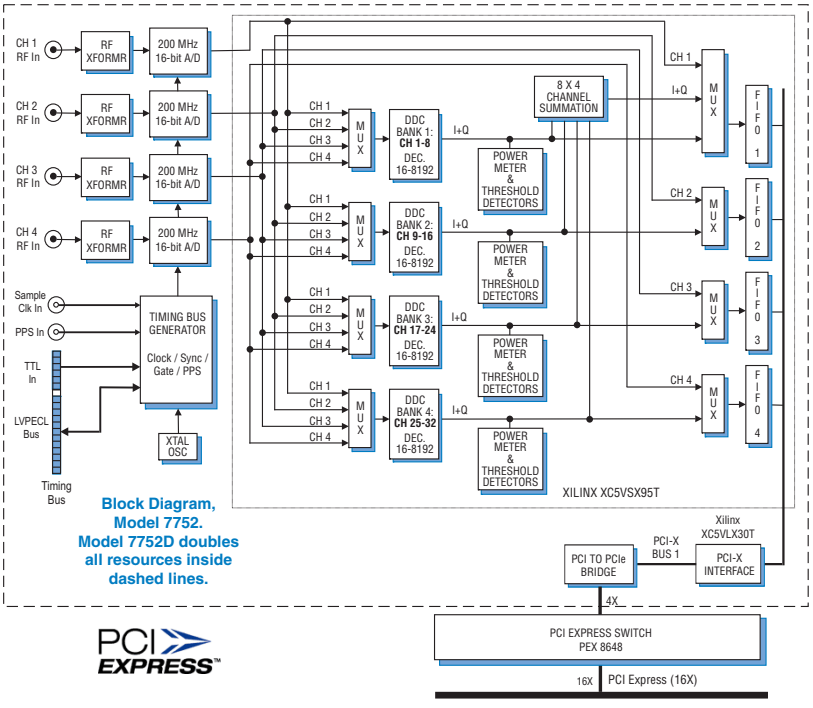
Each of the Model 7752 SX95T FPGAs employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four attached A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Decimation and Filtering

All of the eight channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have a unique decimation setting supporting up to four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. Rejection of adjacent-band components within the 80% bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.



Block Diagram, Model 7752. Model 7752D doubles all resources inside dashed lines.

Power Meters, Threshold Detectors

The 7752 features up to 64 power meters that continuously measure the individual average power output of each DDC channel. The time constant of the averaging interval for each meter is programmable up to 16 kilosamples. In addition, threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

For more information and price quotation on the Models 7752 or 7752D, go to: pentek.com/go/pipe7752. ❑