Model 7651

256-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI

Features

- 256 channels of DDC
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7651 is a high-speed software radio half-length PCI board. It consists of one Model 7151 Quad A/D digitizer with a factory- installed high-performance 256-channel DDC IP Core mounted on a PCI carrier board. The Model 7651 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7651 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 256 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

ReadyFlow Board Support Package

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

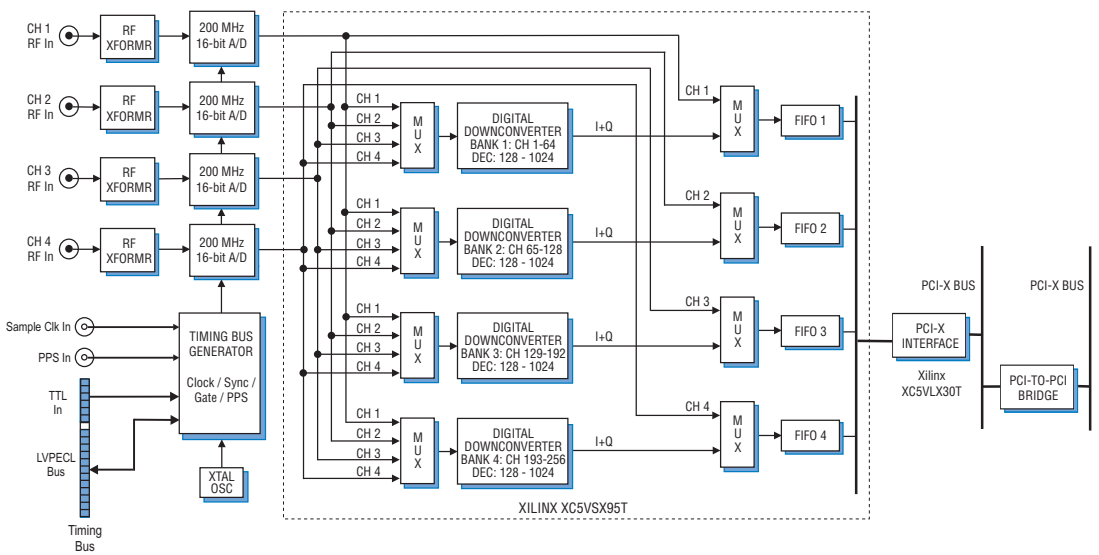
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus. ➤



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➤ Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7651s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7651 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board.

Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array
- **Processing FPGA:** One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T
- **Interface FPGA:** One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface
- **PCI-X Bus:** 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
- **DMA:** 4 channel demand-mode and chaining controller
- **Local Bus:** 64-bit, 66 MHz

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7651	256-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI
Options:	
-732	Two-slot heat sink

Contact Pentek for available options.

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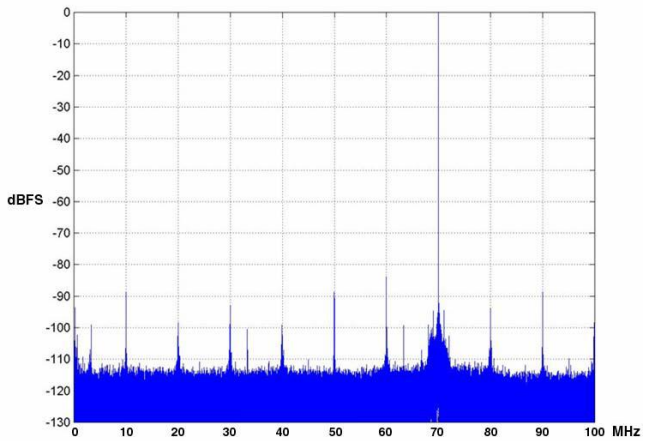
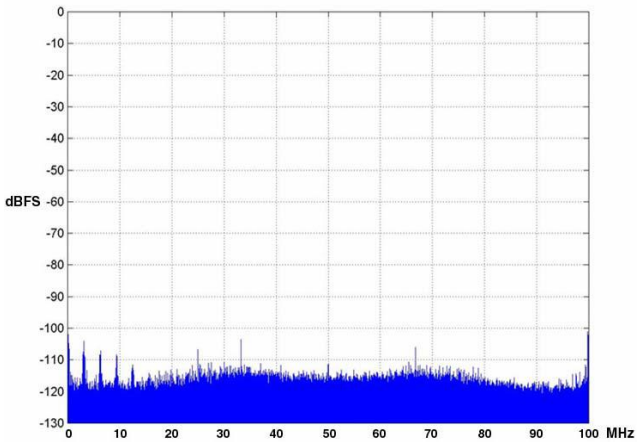
A/D Performance

Spurious-Free Dynamic Range



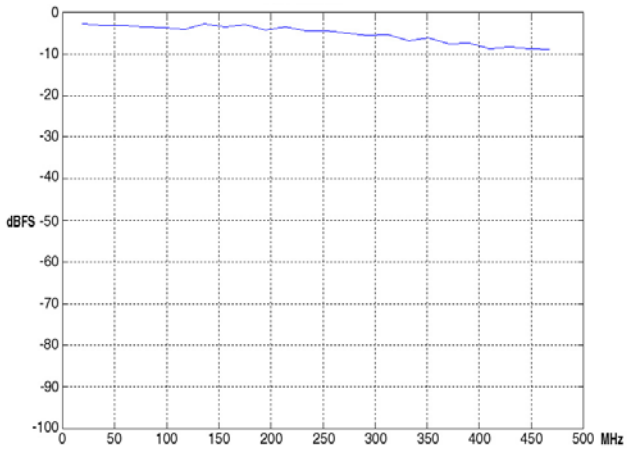
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



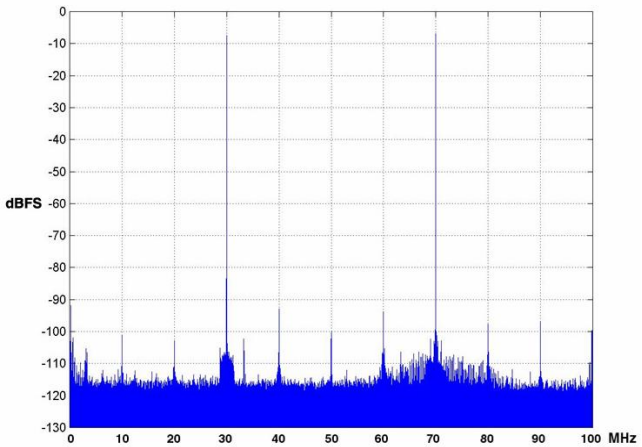
f_s= 200 MHz, Internal Clock

Input Frequency Response



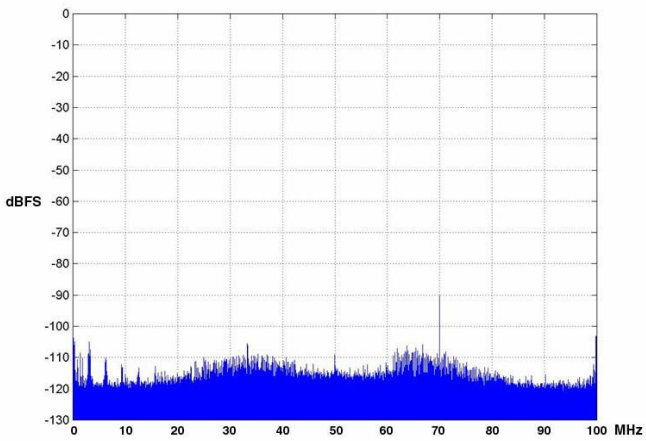
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



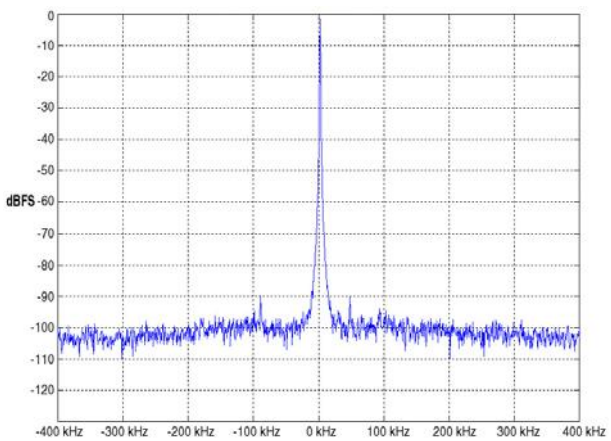
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock