



Model 74751 Model 73751



### Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds

### General Information

Models 72650, 73650 and 74650 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a cPCI carrier board.

Model 72751 is a 6U cPCI board while the Model 73751 is a 3U cPCI board; both are equipped with one Model 71751 XMC. Model 74751 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

### The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC

IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

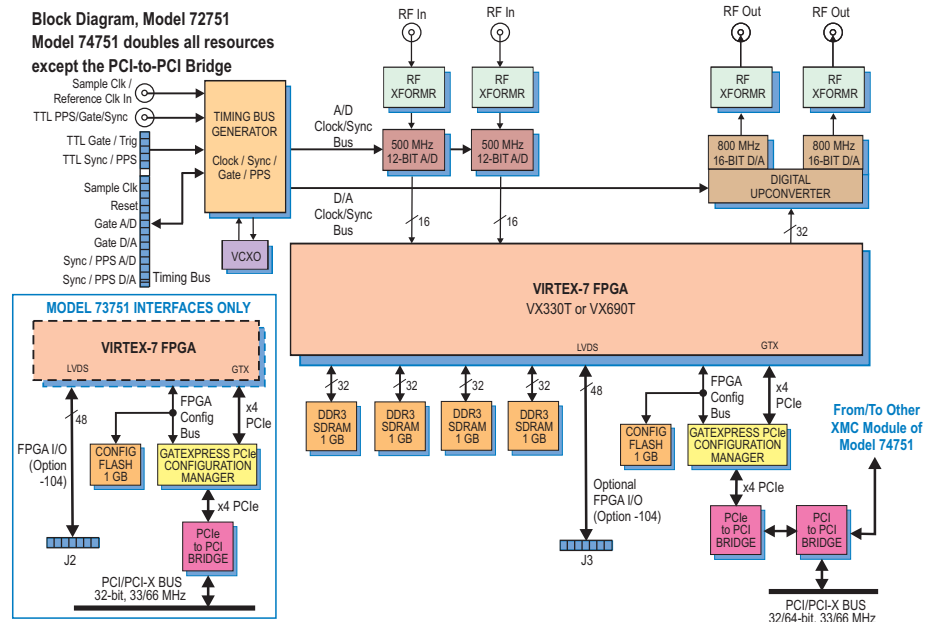
### Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751. ▶



### A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

### DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation set-

ting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

### D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

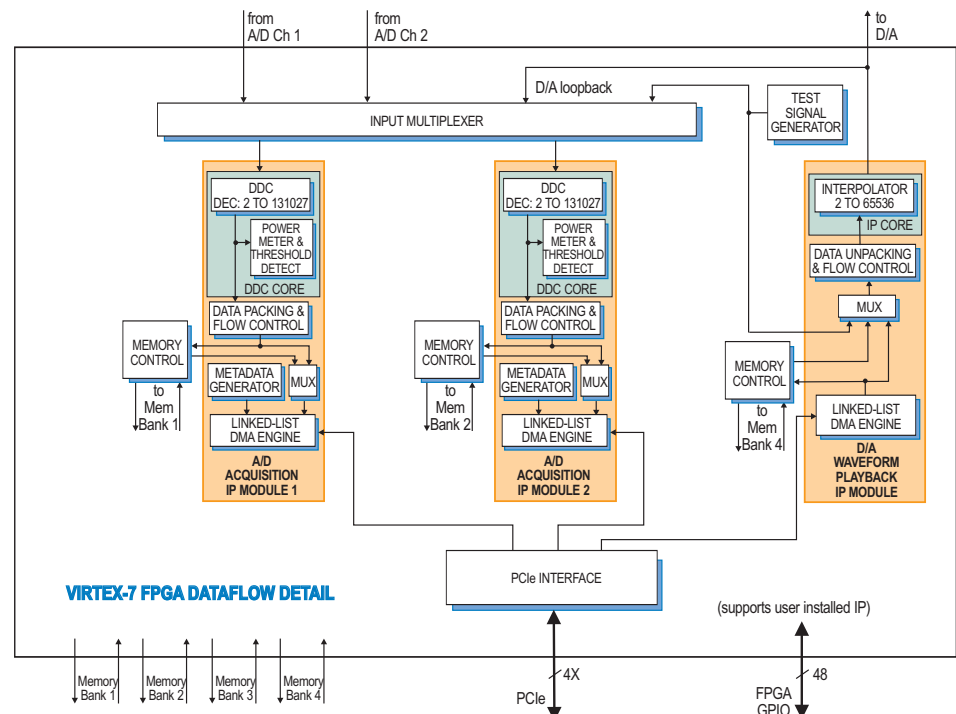
### GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course



► of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

### A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, Texas Instruments ADS5474 400 MHz, 14-bit A/Ds may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

### Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept the baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog outputs are through front-panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

### Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample

clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

### Memory Resources

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

### PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73751: 32 bits only. ►

► **Specifications**

**Model 72751 or Model 73751:** 2 A/Ds,  
2 DDCs, 1 DUC, 2 D/As

**Model 74751:** 4 A/Ds, 4 DDCs, 2 DUCs,  
4 D/As

**Front Panel Analog Signal Inputs (2 or 4)**

**Input Type:** Transformer-coupled, front  
panel female SSMC connectors

**Transformer Type:** Coil Craft  
WBC4-6TLB

**Full Scale Input:** +5 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters (standard) (2 or 4)**

**Type:** Texas Instruments ADS5463

**Sampling Rate:** 20 MHz to 500 MHz

**Resolution:** 12 bits

**A/D Converters (option -014) (2 or 4)**

**Type:** Texas Instruments ADS5474

**Sampling Rate:** 20 MHz to 400 MHz

**Resolution:** 14 bits

**Digital Downconverters (2 or 4)**

**Decimation Range:** 2x to 131,072x in  
two programmable stages of 2x to 256x  
and one fixed 2x stage

**LO Tuning Freq. Resolution:** 32 bits,  
0 to  $f_s$

**LO SFDR:** >120 dB

**Phase Offset Resolution:** 32 bits,  
0 to 360 degrees

**FIR Filter:** 16-bit coefficients, 24-bit output,  
with user programmable coefficients

**Default Filter Set:** 80% bandwidth, <0.3  
dB passband ripple, >100 dB stopband  
attenuation

**D/A Converters (2 or 4)**

**Type:** Texas Instruments DAC5688

**Input Data Rate:** 250 MHz max.

**Output IF:** DC to 400 MHz max.

**Output Signal:** 2-channel real or  
1-channel with frequency translation

**Output Sampling Rate:** 800 MHz max.  
with 2x, 4x or 8x interpolation

**Resolution:** 16 bits

**Digital Interpolators (1 or 2)**

**Interpolation Range:** 2x to 65,536x in  
two stages of 2x to 256x

**Total Interpolation Range (D/A and Digi-  
tal combined):** 2x to 524,288x

**Front Panel Analog Signal Outputs (2 or 4)**

**Output:** Transformer-coupled, front  
panel female SSMC connectors

**Transformer:** Coil Craft WBC4-6TLB

**Full Scale Output:** +4 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources (2 or 4)**

On-board clock synthesizer generates  
two clocks: one A/D clock and one D/A  
clock

**Clock Synthesizers (1 or 2)**

**Clock Source:** Selectable from on-board  
programmable VCXO (10 to 810 MHz),  
front panel external clock or LVPECL  
timing bus

**Synchronization:** VCXO can be locked  
to an external 4 to 180 MHz PLL system  
reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO  
can be divided by 1, 2, 4, 8, or 16, inde-  
pendently for the A/D clock and D/A  
clock

**External Clocks (1 or 2)**

**Type:** Front panel female SSMC connector,  
sine wave, 0 to +10 dBm, AC-coupled,  
50 ohms, accepts 10 to 800 MHz divider  
input clock or PLL system reference

**Timing Bus: (1 or 2)** 26-pin connector

LVPECL bus includes, clock/sync/  
gate/PPS inputs and outputs; TTL sig-  
nal for gate/trigger and sync/PPS  
inputs

**Field Programmable Gate Arrays (1 or 2)**

**Standard:** Xilinx Virtex-7 XC7VX330T-2

**Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**

**Option -104:** Provides 24 LVDS pairs  
between the FPGA and the J2 connector,  
Model 73751; J3 connector, Model 72751;  
J3 and J5 connectors, Model 74751

**Memory (1 or 2)**

**Type:** DDR3 SDRAM

**Size:** Four banks, 1 GB each

**Speed:** 800 MHz (1600 MHz DDR)

**PCI-X Interface**

**PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz  
Model 73751: 32 bits only

**Environmental**

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard 6U or 3U cPCI board

**Ordering Information**

Model	Description
72751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U cPCI
73751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U cPCI
74751	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs - 6U cPCI

**Options:**

-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751