New!

Models 72663, 73663 and 74663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

Model 74663 *Model 73663*

Features

- Complete GSM channelizer with analog IF interface
- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 72663, 73663 and 74663 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a cPCI carrier board.

Model 72663 is a 6U cPCI board while the Model 73663 is a 3U cPCI board; both are equipped with one Model 71663 XMC. Model 74663 is a 6U cPCI board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

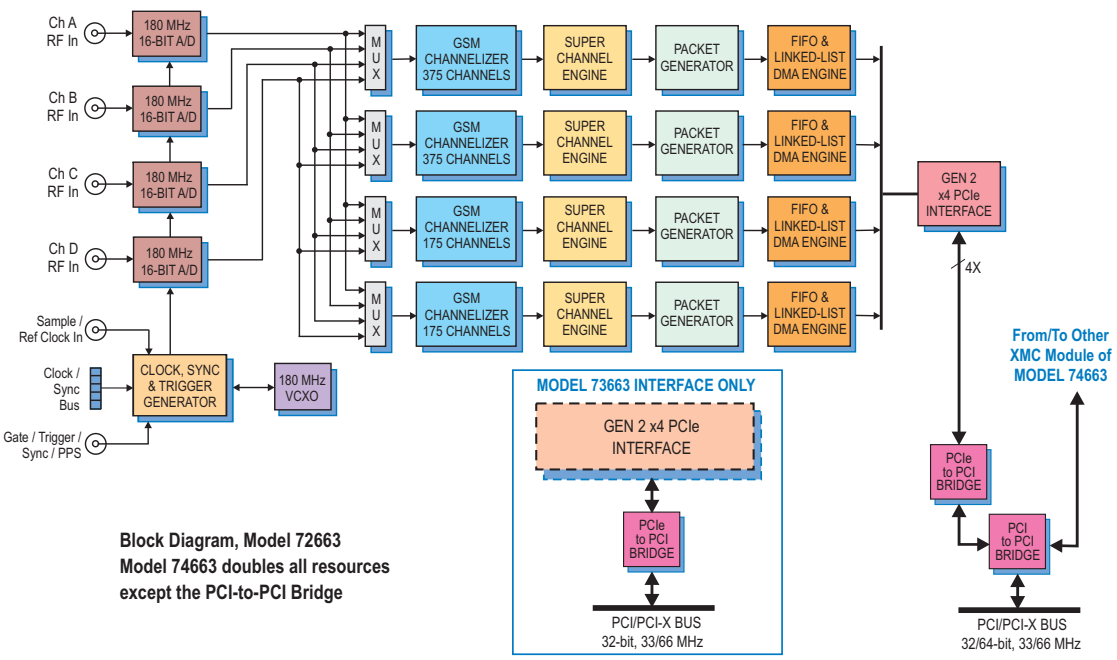
The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤



Block Diagram, Model 72663
Model 74663 doubles all resources except the PCI-to-PCI Bridge

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➤ GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digtitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once compete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73663: 32 bits only.

The PCI-X interface is also used as the programming interface for all status and control between these models and host. ➤

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Specifications

Model 72663 or Model 73663: 4 A/Ds
Model 74663: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
GSM Channel Banks (1 or 2)
DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz
DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 KHz
> 96 dB attenuation at > ±3 MHz
DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
DDC Data Output Format:
24 bits I + 24 bits Q
Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
Frequency Offsets for each DDC:
First: $-f_s/4$ (-270.8333 kHz)
Second: 0 Hz
Third: $+f_s/4$ (+270.8333 kHz)
Fourth: $+f_s/2$ (+541.666 kHz)
Superchannel Sample Rate: f_s
Superchannel Output Format:
26 bits I + 26 bits Q
Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94
Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73663: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72663	1100-Channel GSM Channelizer with Quad A/D - 6U cPCI
73663	1100-Channel GSM Channelizer with Quad A/D - 3U cPCI
74663	2200-Channel GSM Channelizer with Octal A/D - 6U cPCI

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