



Model 7342-428

Model 7242D-428



Features

- Complete software radio transceiver solution
- GateFlow IP Core 428, with four or eight high-performance multiband DDCs and one or two Interpolation Filters, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Models 7242-428 and 7342-428 are cPCI Transceivers with four or eight Multiband DDCs and one or two Interpolation Filters. They consist of one Model 7142-428 transceiver mounted on a cPCI carrier board. Model 7242-428 is a 6U cPCI board, while the Model 7342-428 is a 3U cPCI board. Model 7242D-428 is the same as the Model 7242-428, except it contains two 7142-428's rather than one.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The

DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

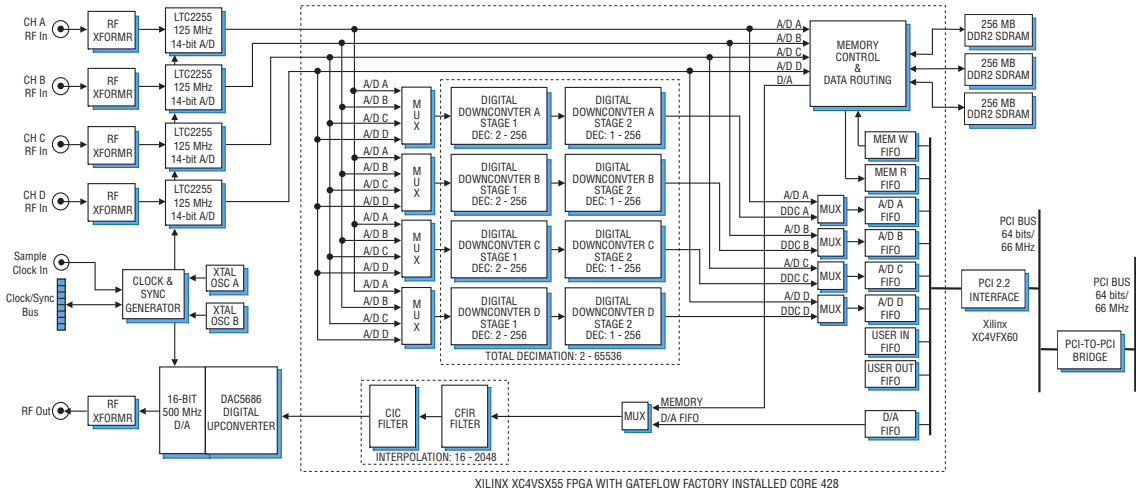
The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ▶

Model 7242-428 and 7342-428 Block Diagram Model 7242-428D doubles all resources except the PCI Bridge



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7242-428's or 7342-428's, or four 7242D-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7242-428 or 7342-428 boards, or forty 7242D-428 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7242-428: Dual Configuration; 7242D-428: Quad Configuration; 7342-428: Dual Configuration
7242D-428 shown in the Specifications

Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters (4)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (4)

Type: Two Xilinx Virtex-4 XC4VXS55 and two Xilinx Virtex-4 XC4VFX60

Memory

DDR SDRAM: 1 GB in six banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7242-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation Filter factory-installed - 6U cPCI
7242D-428	GateFlow Transceiver with eight Multiband DDCs and two Interpolation Filters factory-installed - 6U cPCI
7342-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation 3U cPCI

Contact Pentek for available options