New!

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

Model 58131

JADE

NAVIGATOR
Design Suite

Features

- Ideal radar and software radio interface solution
- Supports one or two Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 multiband DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57131 and 58131 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71131 XMC modules mounted on a VPX carrier board. Model 57131 is a 6U board with one Model 71131 module while the Model 58131 is a 6U board with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating,

triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the ➤
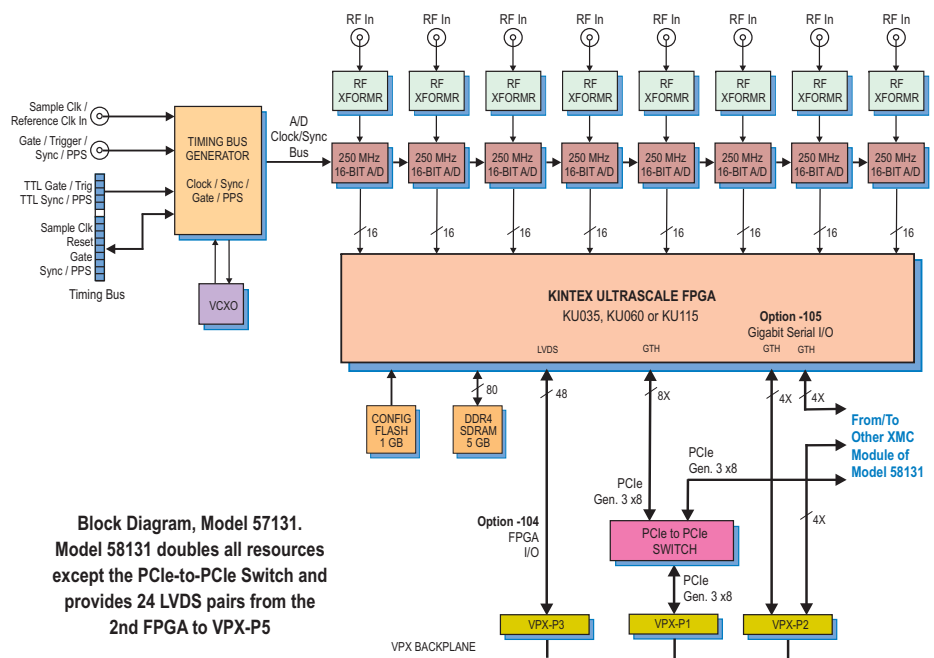
**Block Diagram, Model 57131.
Model 58131 doubles all resources
except the PCIe-to-PCIe Switch and
provides 24 LVDS pairs from the
2nd FPGA to VPX-P5**

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A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients.

The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts eight or 16 analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight or four.

Memory Resources

The architecture supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 ➤

KINTEX ULTRASCALE FPGA DATAFLOW DETAIL
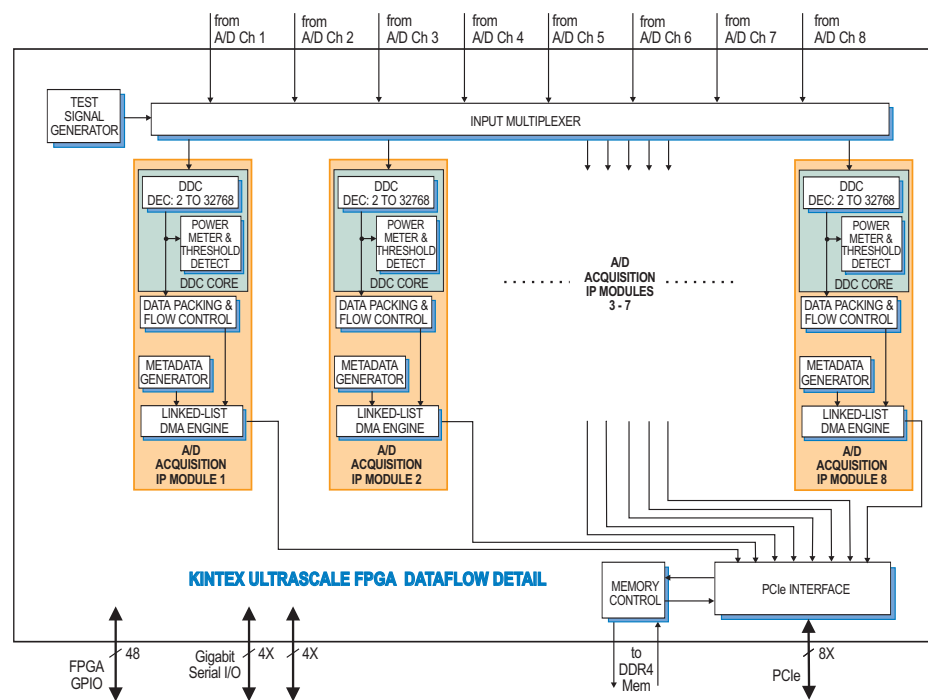
Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK
Development Systems

Ordering Information

Model	Description
57131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
58131	16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57131: 8 A/Ds;

Model 58131: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
 Input Type: Transformer-coupled, front panel female MMCX connectors
 Transformer Type: Coil Craft WBC4-6TLB
 Full Scale Input: +4 dBm into 50 ohms
 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8 or 16)
 Type: Texas Instruments ADS42LB69
 Sampling Rate: 10 MHz to 250 MHz
 Resolution: 16 bits

Digital Downconverters (8 or 16)
 Decimation Range: 2x to 32,768x in three stages of 2x to 32x
 LO Tuning Freq. Resolution: 32 bits, 0 to f_s
 LO SFDR: >108 dB
 Phase Offset Resolution: 32 bits, 0 to 360 degrees
 FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
 Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
 On-board clock synthesizers

Clock Synthesizer (1 or 2)
 Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
 Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
 Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
 Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
 Type: Front panel female MMCX connector, LVTTL
 Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
 Standard: Xilinx Kintex UltraScale XCKU035-2
 Option -084: Xilinx Kintex UltraScale XCKU060-2
 Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
 Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57131; and P5 connector, Model 58131 for custom I/O
 Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
 Type: DDR4 SDRAM
 Size: 5 GB Model 57131; 10 GB Model 58131
 Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
 PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
 Standard: L0 (air cooled)
  Operating Temp: 0° to 50° C
  Storage Temp: –20° to 90° C
  Relative Humidity: 0 to 95%, non-condensing
 Option -702: L2 (air cooled)
  Operating Temp: –20° to 65° C
  Storage Temp: –40° to 100° C
  Relative Humidity: 0 to 95%, non-condensing
 Option -713: L3 (conduction cooled)
  Operating Temp: –40° to 70° C
  Storage Temp: –50° to 100° C
  Relative Humidity: 0 to 95%, non-condensing

Size: 9.187 in. x 6.717 in. (233.35 mm x 170.60 mm)