PENTEK

Onyx Virtex-7 & Cobalt Virtex-6

Product Catalog

Onyx

Cobalt

Last Updated: May 2014

Contents

Cobalt/Onyx Selection Chart

Cobalt	Onyx	A/D Converters Qty	A/D Converters Rate	A/D Converters Bits	D/A Converters Qty	D/A Converters Rate	D/A Converters Bits	Other Features
71620	71720	3	200 MHz	16	2	800 MHz	16	
71621		3	200 MHz	16	2	800 MHz	16	3 DDCs, Sum, Int
71660	71760	4	200 MHz	16				
71661		4	200 MHz	16				4 DDCs, Sum
71662		4	200 MHz	16				32 DDCs, Sum
71663		4	200 MHz	16				1100 DDCs
71690	71790	2	200 MHz	16				L-Band Tuner
71650		2	400 MHz	14	2	800 MHz	16	
71651	71751	2	400 MHz	14	2	800 MHz	16	2 DDCs, Int
71650		2	500 MHz	12	2	800 MHz	16	
71651	71751	2	500 MHz	12	2	800 MHz	16	2 DDCs, Int
71630	71730	1	1 GHz	12	1	1 GHz	12	
71640		1/2	3.6/1.8 GHz	12				
71641	71741	1/2	3.6/1.8 GHz	12				1/2 DDCs,
71670					4	1.25 GHz	16	
71671	71771				4	1.25 GHz	16	Extended Int
71610								LVDS I/O
71611								Quad sFPDP

Rate = Maximum Sampling Frequency
DDC = Digital Downconverter
Int = Interpolation Filter
sFPDP = Serial FPDP – VITA 17.1
Sum = Beamforming Summation Block & Aurora Chaining Interface

The Latest Generations of Virtex FPGAs

With each new generation of FPGA devices, Xilinx continues to push the performance envelope to match the ever increasing requirements of target applications.

The announcement of the Virtex-6 and Virtex-7 were no exception. More processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements, are all part of these new devices.

While it might be easy to assume that faster, bigger, more powerful is better, it's important to understand how the latest FPGA innovations actually deliver this higher performance to best match the device to the specific requirements of the application.

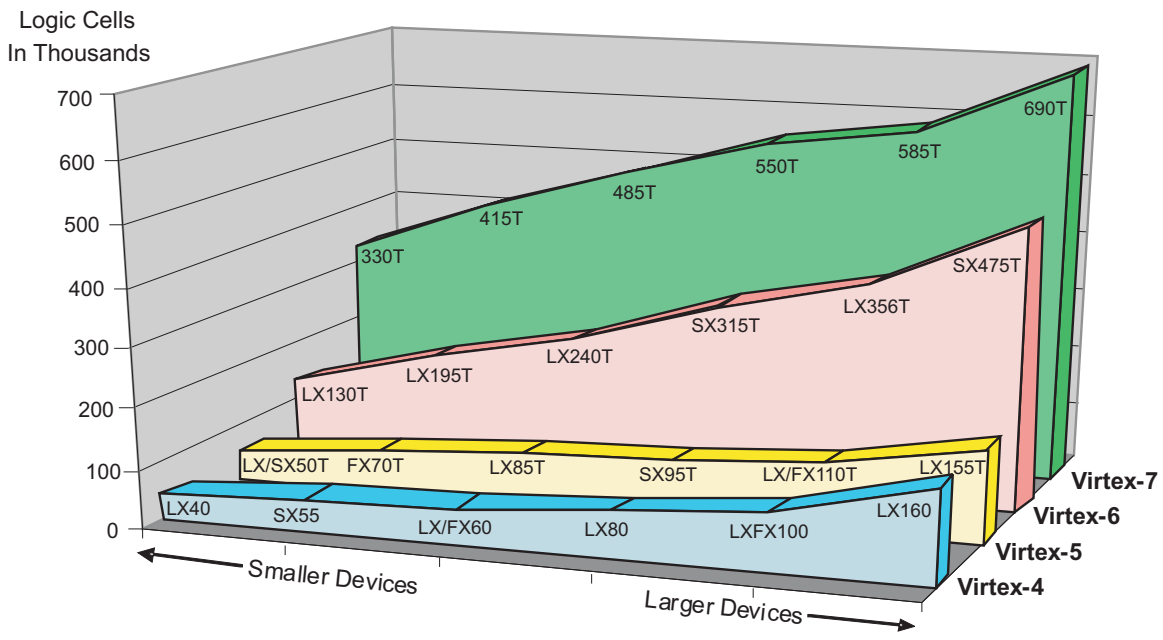
One of the standard metrics for FPGAs is the number of logic cells. This figure shows the steady improvement in the last four generations of Xilinx FPGAs starting with the Virtex-4 and continuing to the Virtex-7. The graph displays the number of logic cells contained in a range of different density devices offered in a 35 mm x 35 mm BGA (Ball-Grid Array) package. This clearly shows the dramatic increase in resource density, bounded by the constraints of the size and power dissipation capacity of a given package.

Since Virtex-4 CLBs (Configurable Logic Blocks) comprise eight logic cells, while Virtex-5 and Virtex-6 CLBs comprise 12, the increase in logic cells between Virtex-4 and Virtex-5 actually translates to a decrease in CLBs because each CLB in the Virtex-5 requires more logic cells. While the Virtex-5 CLBs are more powerful than their Virtex-4 counterparts, there are still fewer of them to use. What is also clear from this graph is that the Virtex-6 represents a significant increase in density from the Virtex-5 family.

The Virtex-7 offers the highest performance thus far with twice the performance and twice the resources of the Virtex-6.

The Virtex-7 devices feature low-power 28 nm process technology to implement up to 3.1 Tbits/sec of I/O and up to 2 million logic cells. They provide up to 6.7 TMACs of DSP resources, especially important for software radio applications. Because of new process technologies and other power management schemes, they consume half the power of Virtex-6 for a given function.

This combination of lower power and higher performance for each of the key resources benefits software radio, opens up new product markets, and extends the capabilities of existing applications.



Logic Cell Density Comparison, Virtex-4, Virtex-5, Virtex-6, and Virtex-7 FPGAs Used in Pentek Products

The Cobalt & Onyx Architecture

Features and Implementation

Cobalt & Onyx Architectural Features

- Cobalt®: Xilinx Virtex-6 FPGA
- Onyx®: Xilinx Virtex-7 FPGA
- Configurable memory resources—depending on model
- On-board clocking and synchronization
- Modular I/O design to support a wide range of signal types

Cobalt & Onyx Performance Features

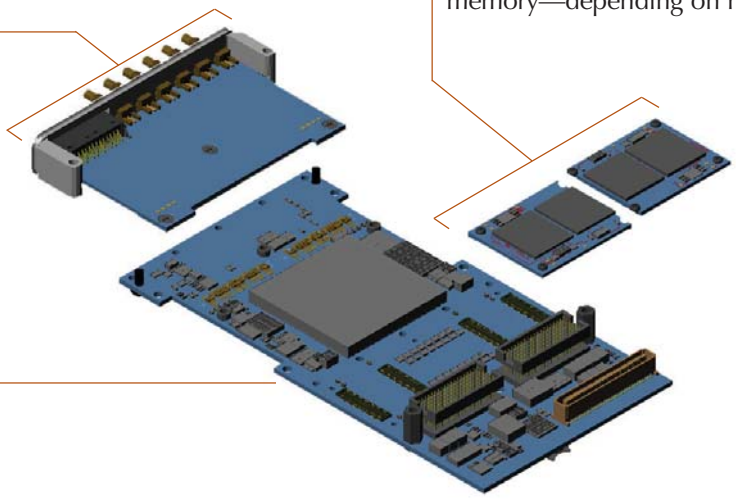
- A/D sampling rates from 10 MHz to 3.6 GHz
- D/A sampling rates up to 1.25 GHz
- Powerful linked-list DMA engines
- PCI Express as the primary control and data transfer interface
- Secondary serial gigabit interface
- All models available in XMC, PCI Express, OpenVPX and CompactPCI formats
- Available in commercial and in several ruggedization levels up to and including conduction cooling

Memory Resources

These two smaller boards are used for the memory resources allowing for customization of two types of memory—depending on model.

I/O Module

The I/O module is a separate printed-circuit board that caries all of the analog interface circuitry providing excellent isolation from noise. Typical front panel signals include analog in and out, clocking, sync, and triggering.



Main Board

The main board serves as the foundation of all Cobalt and Onyx products. It houses the FPGA, FLASH memory, XMC interfaces, user programmable FPGA interfaces and hosts the memory and I/O modules.

Flexible Architecture

The modularity of this assembly offers an unprecedented degree of flexibility for creating Cobalt or Onyx modules with completely different features by just incorporating different I/O modules.

As shown in the diagram, the front panel allows for a maximum of six SSMC signal connectors. The external clocking, trigger and synchronization connector is a front-panel multipin flat cable connector and is the same on all models, except those designed to operate at frequencies higher than 1.0 GHz.

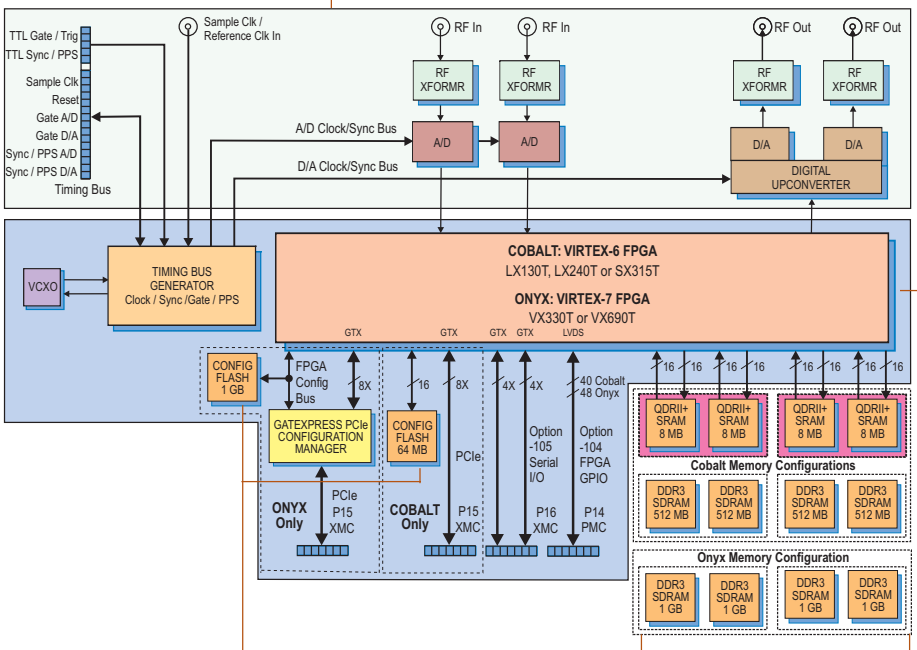
Components and Circuitry

Cobalt or Onyx I/O Module

Shown here is a typical Cobalt or Onyx I/O module. The input analog ports are transformer-coupled to two high-speed A/D converters. The digital outputs are delivered into the Virtex-6 or Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Besides the two A/Ds, the typical module could include one DUC (Digital Upconverter), and two D/As which are transformer-coupled to the output analog ports.

In addition to the input and output ports, the module includes a multiport connector for clocking and synchronization. All connectors are on the front panel.



Xilinx Virtex-6 or Virtex-7 FPGA

The Cobalt Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T.

The Onyx Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are: VX330T or VX690T.

The SX315T features 1344 DSP48E slices, while the VX690T features 3600 DSP48E1 slices. These devices are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

FLASH Memory

Cobalt: The 16-bit wide 64 MB FLASH provides non-volatile memory for factory boot code, self-test, and user parameters

Onyx: The 16-bit wide 1024 MB FLASH provides non-volatile memory for factory boot code, self-test, user parameters, and FPGA images for dynamically reconfiguring the FPGA.

Memory Resources

Cobalt: Up to four independent memory banks can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each memory type.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep.

Onyx: Four independent DDR3 SDRAM memory banks are available. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

More on next page ➤

The Cobalt & Onyx Architecture

Components and Circuitry

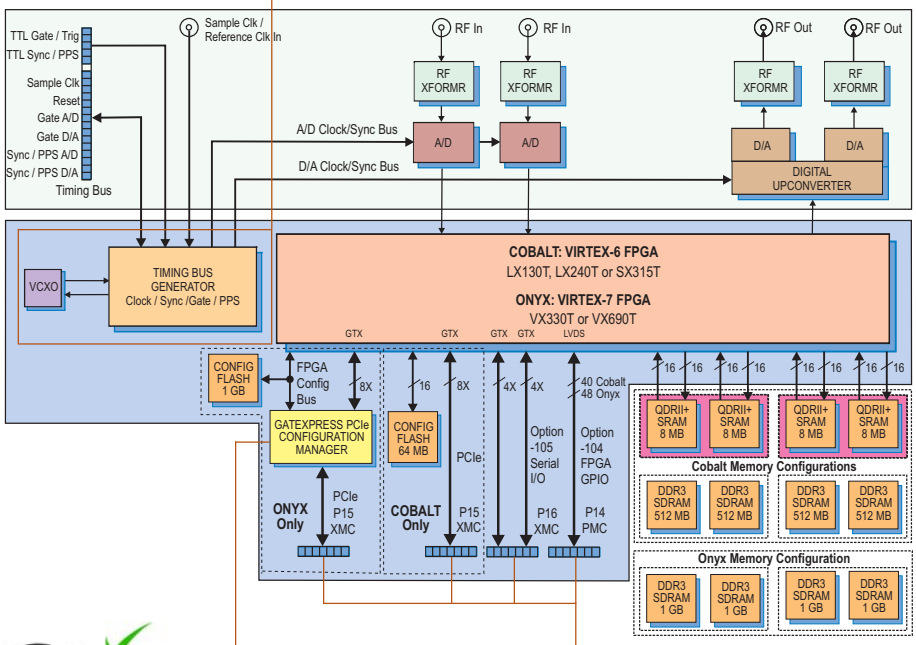
Clocking and Synchronization

The internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

The timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock which can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the synthesizer locks the VCXO to an external system reference, typically 10 MHz.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.



GateXpress

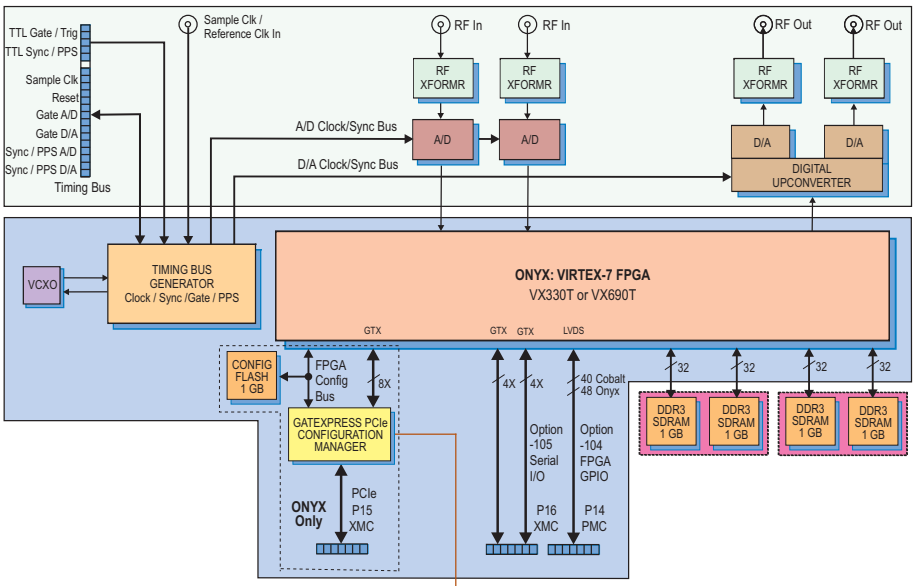
Available only in the **Onyx** series, the GateXpress™ is a sophisticated FPGA PCIe configuration manager for loading and reloading the FPGA. At powerup, GateXpress presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window.

The board's configuration FLASH can hold up to four FPGA images for dynamically reconfiguring the FPGA.

Board Interfaces

The FPGA is also used to implement the primary board interfaces. The basic XMC module shown here is also available in different formats, such as PCI Express, OpenVPX, and CompactPCI.

More information about formats and interfaces starts on page 9.



GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH.

This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

The Cobalt & Onyx Architecture

FPGA Dataflow

All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering, and memory control. The Cobalt & Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt/Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. Depending on model, the factory-installed functions may include A/D acquisition and D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ (Cobalt only) memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the board to operate as a complete turn-key solution without the need to develop any FPGA IP.

For applications that require specialized functions, users can install custom IP for data processing. Pentek GateFlow® FPGA Design Kits (described later in this catalog) include all of the factory installed modules as documented source code. Developers can integrate their IP with the Pentek factory-installed functions or use the GateFlow to completely replace the Pentek IP with theirs.

A/D Acquisition IP Modules

This typical Cobalt/Onyx module includes two A/D Acquisition IP modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

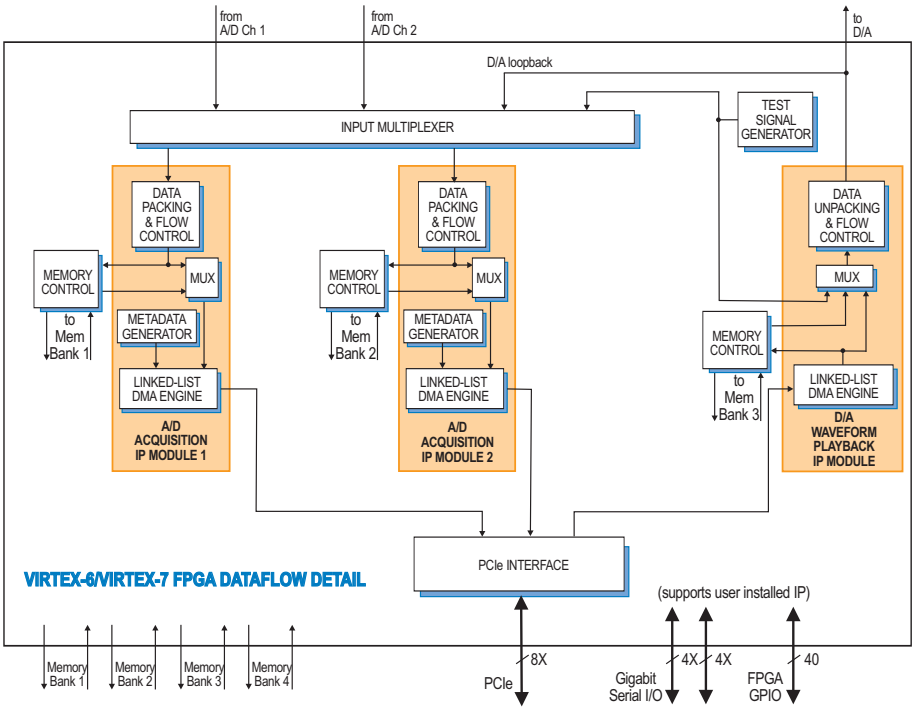
For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

Factory-installed functions for this typical Cobalt/Onyx module include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

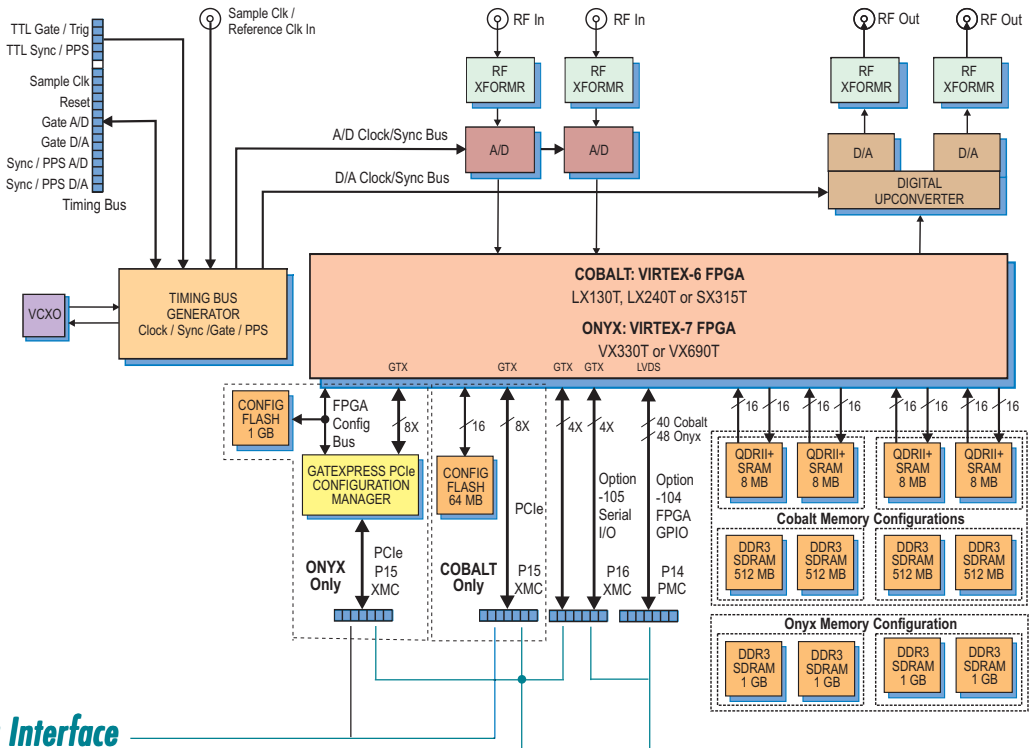


XMC Format

Here is a photograph of the typical board reviewed in detail in the previous section. In its XMC configuration, each Cobalt or Onyx module complies with the VITA 42.0 XMC specification and is suitable for mounting on motherboards with PMC/XMC connectors.

All XMC modules are available in commercial and in several ruggedization levels up to and including conduction cooling.

The XMC format applies to the Model 71xxx product family.



PCI Express Interface

The **Cobalt** XMC includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Gen. 2 provides 4 GB/sec peak data transfer rate.

The **Onyx** XMC includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen. 3 provides 8 GB/sec peak transfer rate.

The x8 interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

Both **Cobalt** and **Onyx** XMC products comply with the VITA 42.0 XMC specification. Each of the two connectors provides dual 4X links or a single 8X link.

With dual XMC connectors, the XMC products support both x4 and x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Optional Interfaces

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections (Cobalt) or 24 pairs (Onyx) to the FPGA for custom I/O.

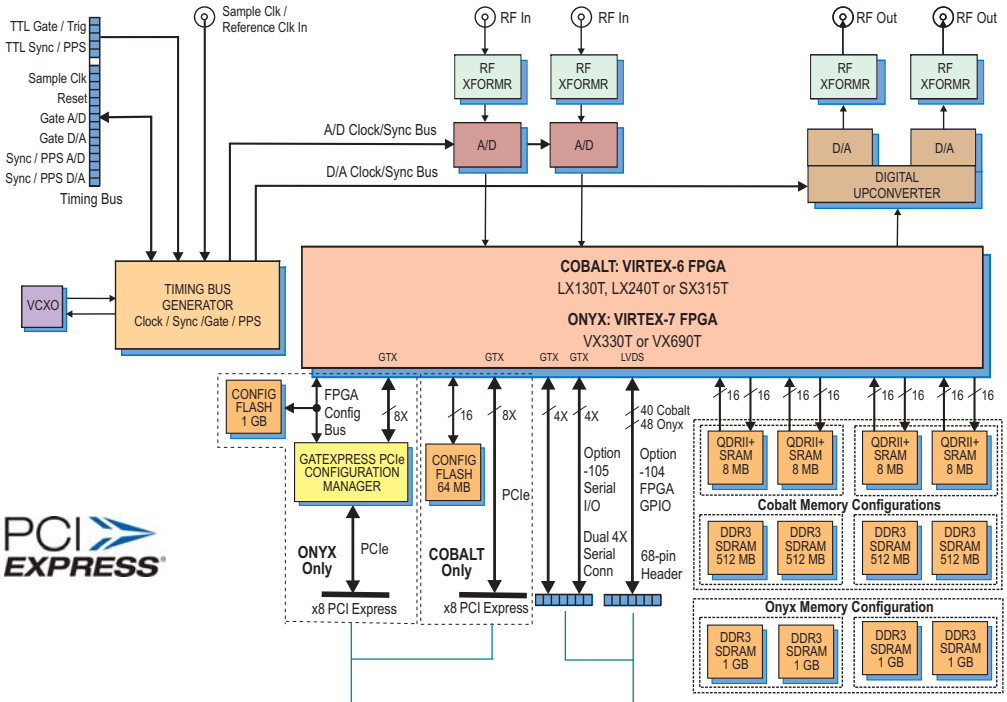
Option -105 installs the P16 XMC connector with a single 8X or dual 4X gigabit links to the FPGA to support serial protocols.

Cobalt & Onyx Formats & Interfaces

PCI Express Format

The PCI Express format shown here is suitable for mounting in PCs with PCIe connectors and interfaces. Physically, the XMC module reviewed in the previous page is mounted on a PCI Express "carrier" board with x8 PCIe motherboard connectors. Other connectors provide additional interfaces as described below.

The unique design of the PCIe carrier includes an integrated fan that keeps the module cool even in demanding situations while still requiring a single PCIe slot.



PCI Express Interface

The **Cobalt** PCIe board includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Gen. 2 provides 4 GB/sec peak data transfer rate.

The **Onyx** PCIe board includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen. 3 provides 8 GB/sec peak transfer rate.

The x8 interface includes multiple DMA controllers for efficient transfers to and from the module.

Optional Interfaces

Option -104 connects 20 pairs of LVDS connections (Cobalt) or 24 pairs (Onyx) from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

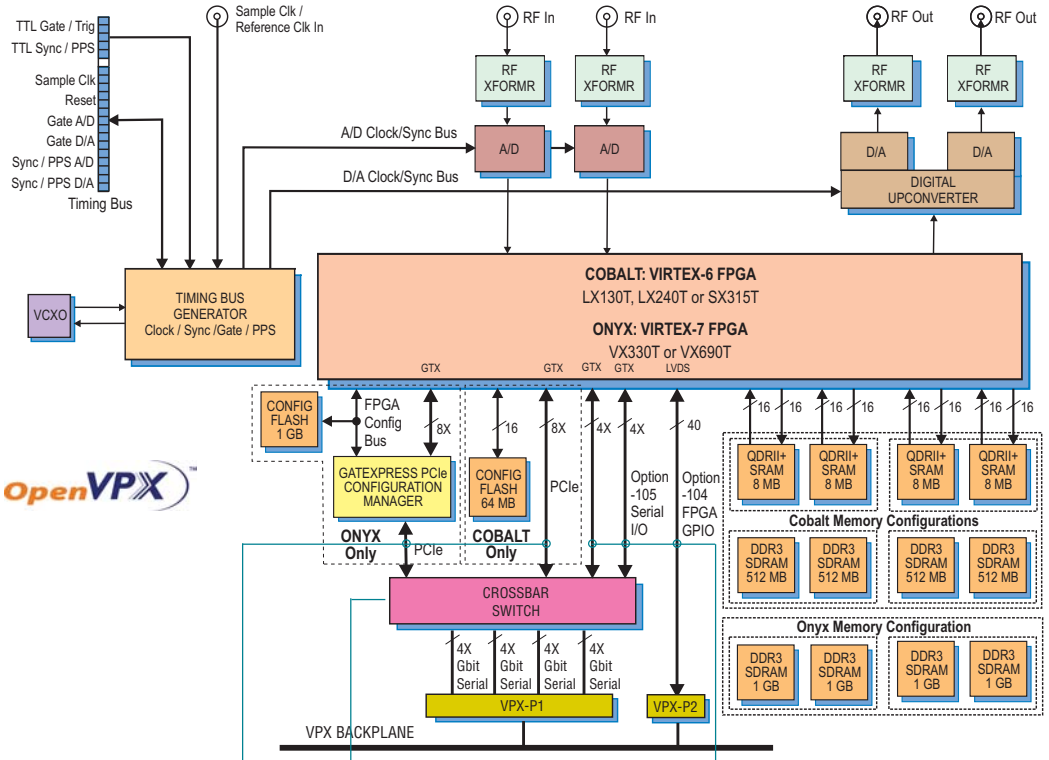
3U OpenVPX Format 1

The OpenVPX Format 1 is compatible with several VITA standards including:

VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)

Shown here is the 3U OpenVPX COTS version (left) and the rugged version which is available in several ruggedization levels up to and including conduction cooling.

Another OpenVPX format is described in the next page.



PCI Express Interface

The **Cobalt** 3U OpenVPX board includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Gen. 2 provides 4 GB/sec peak data transfer rate.

The **Onyx** 3U OpenVPX board includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen. 3 provides 8 GB/sec peak transfer rate.

The x8 interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 3U OpenVPX Cobalt or Onyx board features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X) for routing over to the VPX-P1 connector.

Optional Interfaces

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX-P2 connector for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to the crossbar switch for routing to VPX-P1.

Cobalt & Onyx Formats & Interfaces

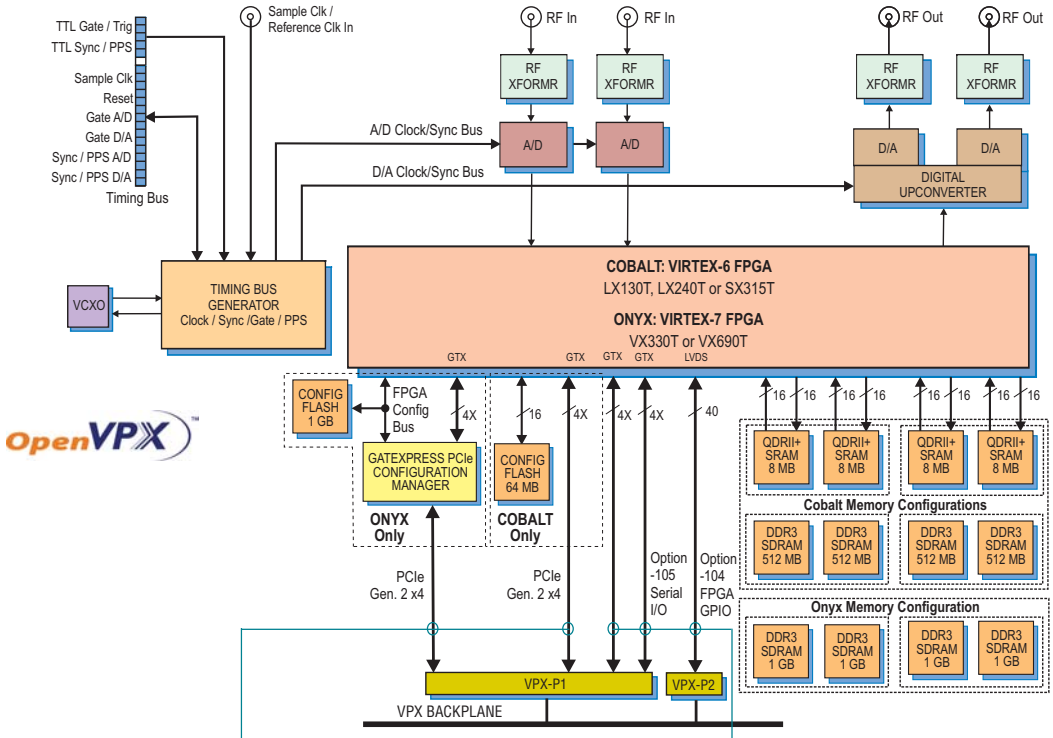
3U OpenVPX Format 2

The OpenVPX Format 2 is compatible with several VITA standards including:

VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)

Shown here is the 3U OpenVPX COTS version (left) and the rugged version which is available in several ruggedization levels up to and including conduction cooling.

A comparison of the two OpenVPX formats is given in the table below.



PCI Express Interface

Both **Cobalt** and **Onyx** boards include an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications.

The x4 PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

Optional Interfaces

Option -104 installs 20 pairs of LVDS connections (**Cobalt**) or 24 pairs (**Onyx**) between the FPGA and VPX-P2 for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA to VPX-P1 to support serial protocols.

OpenVPX Families

By omitting the Format 1 Crossbar switch, Format 2 products achieve significant reductions in power and price. These and other differences are shown in the comparison table.

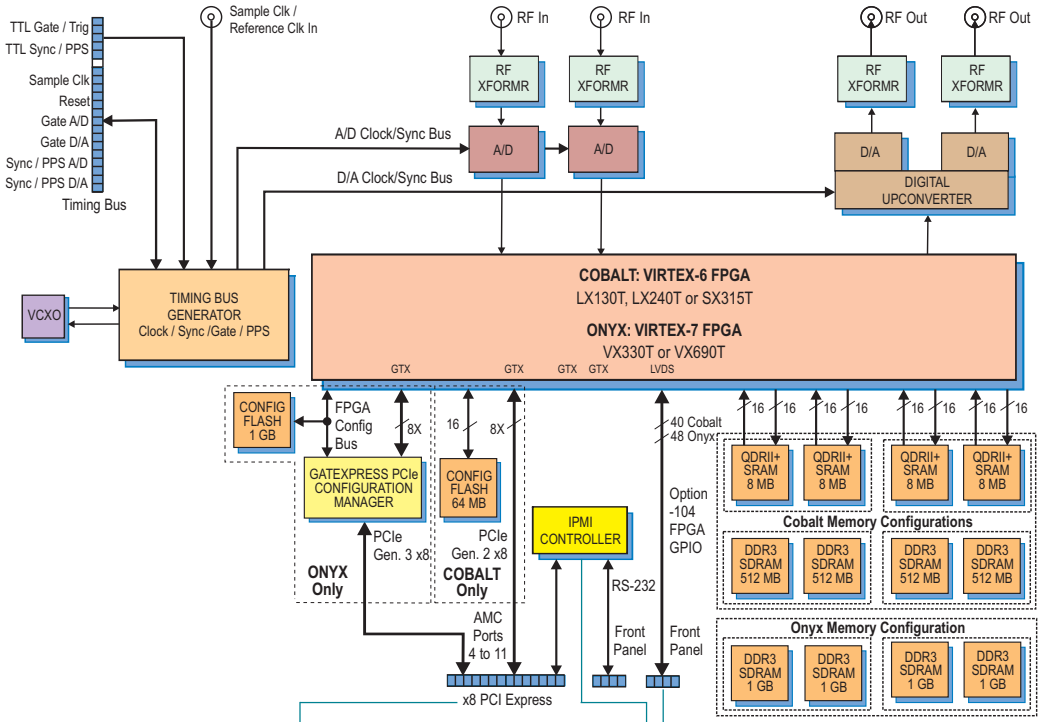
OpenVPX Family Comparison

	Format 2	Format 1
Form Factor	3U OpenVPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

AMC Format

Module Management

The AMC format complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).



PCI Express Interface

The **Cobalt** AMC module includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications.

The x8 PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

The **Onyx** AMC module includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications.

The x8 PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

Module Management

The Module Management Controller complies with the IPMI 2.0 MMC specification.

Optional Interface

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

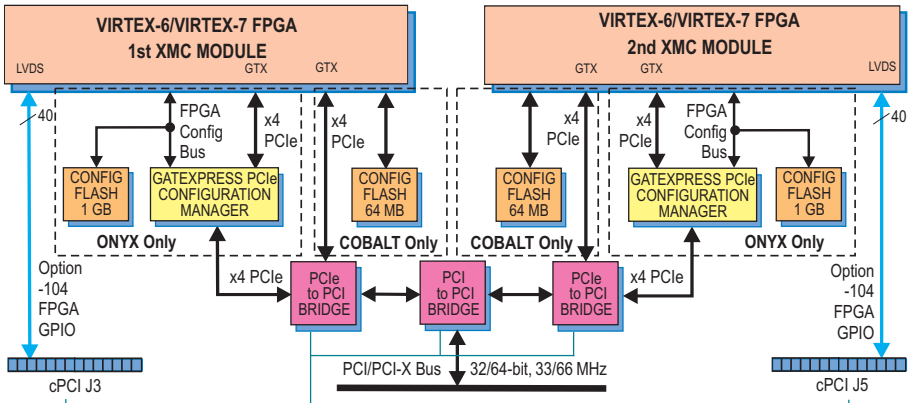
Cobalt & Onyx Formats & Interfaces

CompactPCI Formats

As shown here, the CompactPCI format is available in three configurations:

- 6U cPCI with double density; this configuration mounts two XMC modules on a 6U carrier board.
- 6U cPCI with single density; this configuration mounts only one XMC module on a 6U carrier board.
- 3U cPCI mounts one XMC module on a 3U carrier board

In order to describe these three configurations in more detail, we have omitted the components and circuitry shown in the previous three formats; we just show the Virtex-6/Virtex-7 FPGAs with the external connections that define the standard and optional interfaces.



6U cPCI Double Density

Two PCIe-to-PCI bridges connect the x4 PCIe interfaces from each XMC module to a PCI-to-PCI bridge. This bridge connects both modules to the 32- or 64-bit, 33/66 MHz PCI/PCI-X bus.

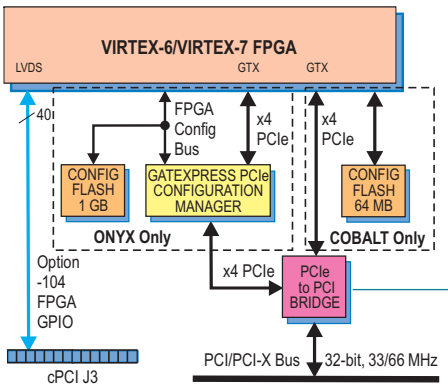
6U cPCI Optional Interface

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 connector for custom I/O.

The J5 connector supports Option -104 for the 2nd XMC module.

6U cPCI Single Density

The 2nd XMC module, its associated PCIe-to-PCI bridge, and the optional interface connection to J5 are not present.



3U cPCI Single Density

A PCIe-to-PCI bridge connects the x4 PCIe interface from the XMC module to the 32-bit, 33/66 MHz PCI/PCI-X bus.

3U cPCI Optional Interface

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 connector for custom I/O.

Pentek ReadyFlow Board Support Package

Users of high-performance data acquisition and signal processing boards often find themselves frustrated by the fact that when their new devices are delivered, they are unable to put them to immediate use.

To address this issue, Pentek has developed the **ReadyFlow**® BSPs (Board Support Packages) for all of its board-level products.

The package contains C-language examples that demonstrate the capabilities of Pentek products. The examples included provide the answers to most of the questions that occur with first-time users of these products.

ReadyFlow BSPs are designed to reduce development time during the initial stages and when new hardware is added to the system. All packages are built with a consistent style and function-naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware.

Command Line Interface

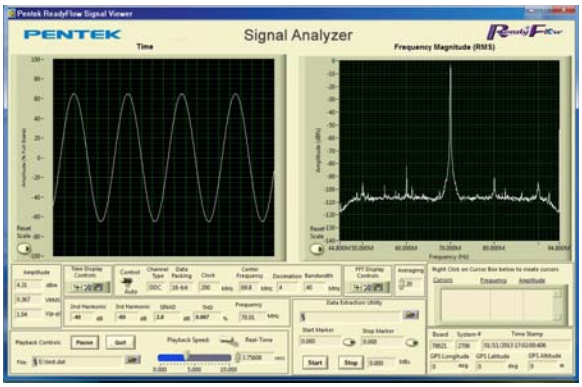
The Command Line Interface is a pre-compiled executable that runs the hardware right out of the box, without the need to write any code.

Specific to the hardware features of the supported board, it allows operating arguments to be entered on the command line for controlling board parameters.

For command line functions that control data acquisition, the captured data can be saved in a host file or routed to the Signal Analyzer.

Signal Analyzer

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



ReadyFlow Board Support Package

Pentek GateFlow FPGA Design Kit

Using the FPGA Design Kit

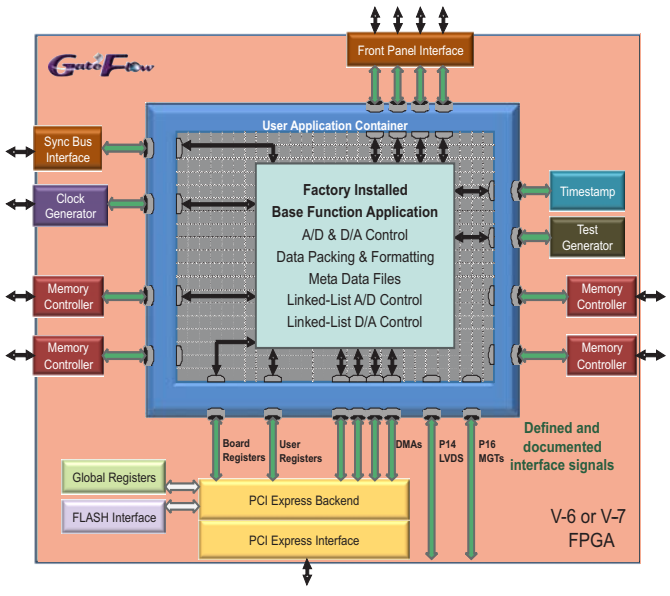
The **GateFlow**® FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt or Onyx architecture configures the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

The User Application Container

Shown here is the FPGA block diagram of a typical Cobalt/Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the following pages.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



Models 71620 & 71720: Transceiver with Three A/Ds, DUC, Two D/As - XMC

Model 71620

Model 71720

Model 71620 is a member of the **Cobalt** family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. Model 71720 is a member of the **Onyx** family of high-performance modules based on the Virtex-7 FPGA.

These multichannel, high-speed data converters, are suitable for connection to HF or IF ports of a communications or radar system. Their built-in data capture and playback features offer an ideal turnkey solution.

Each model includes three A/Ds, one DUC, two D/As and four banks of memory. In addition to supporting PCI Express as a native interface, these models include general-purpose and gigabit serial connectors for application-specific I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT or Virtex-7 VXT FPGAs
- Model 71720: GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Model 71620: Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM; Model 71720: 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Model 71620: PCI Express (Gen. 1 & 2) interface up to x8; Model 71720: PCI Express (Gen. 1, 2, and 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converters

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

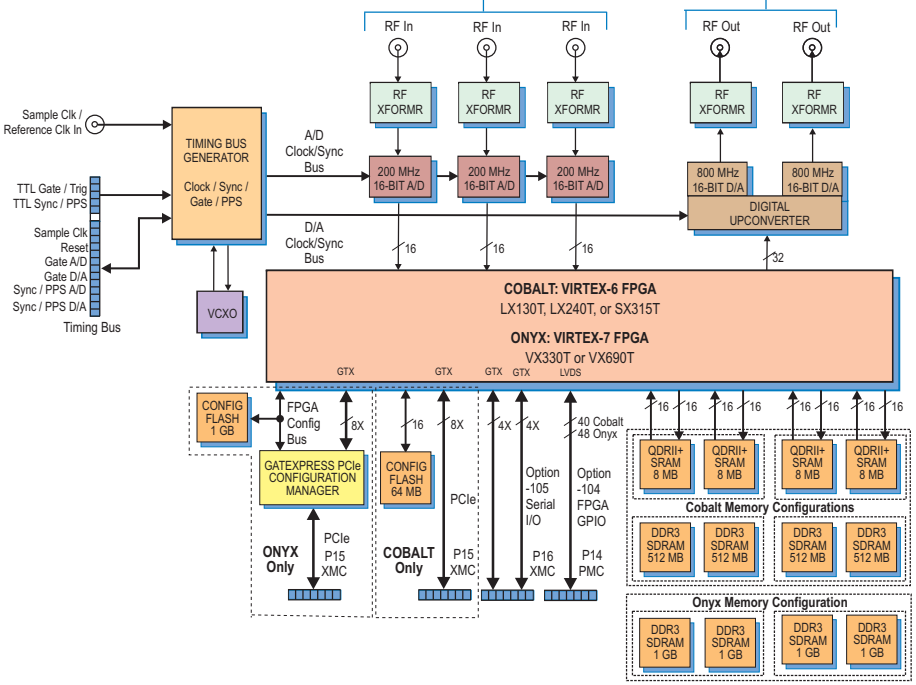
The digital outputs are delivered into the Virtex-6 or Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/As

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA which is optionally interpolated, upconverted and then delivered to the two D/As.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) digital outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.



Models 71620 & 71720: Transceiver with Three A/Ds, DUC, Two D/As - XMC

Installed IP Modules

The factory-installed functions in both models include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

A/D Acquisition IP Modules

Both models feature three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

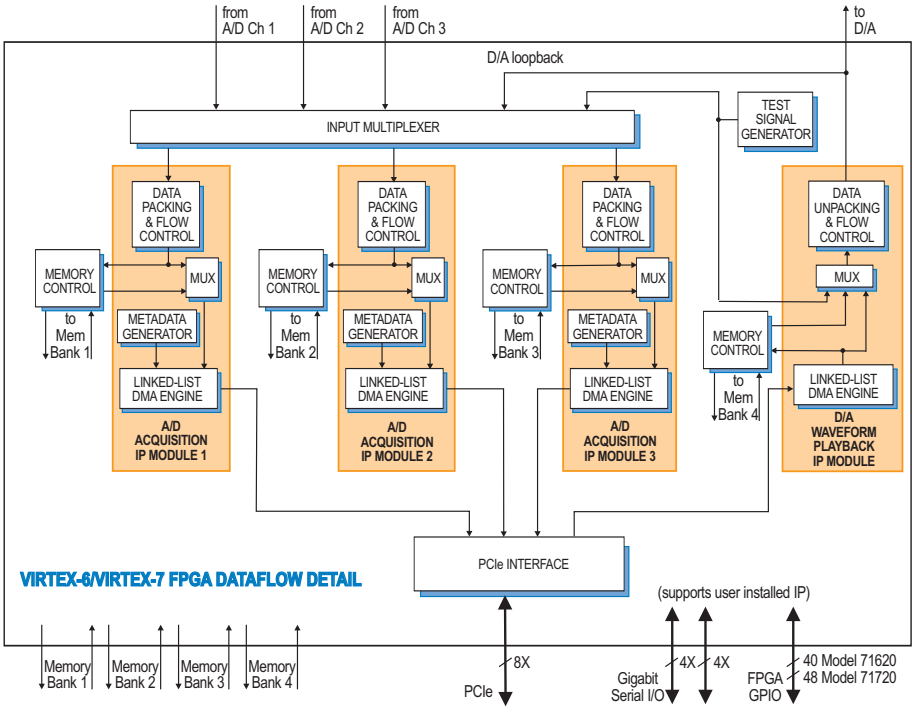
For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The factory-installed functions in both models include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.



Models 71620 & 71720: Transceiver with Three A/Ds, DUC, Two D/As - XMC

Also Available

Model	Format
78620	x8 PCI Express
53620	3U OpenVPX - Format 1
52620	3U OpenVPX - Format 2
56620	AMC
73620	3U cPCI - Single Density
72620	6U cPCI - Single Density
74620	6U cPCI - Double Density

Model	Format
78720	x8 PCI Express
53720	3U OpenVPX - Format 1
52720	3U OpenVPX - Format 2
56720	AMC
73720	3U cPCI - Single Density
72720	6U cPCI - Single Density
74720	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Model 71620 Xilinx Virtex-6 FPGA
- **Standard:** CXC6VLX130T
- **Optional:** XC6VLX240T, or XC6VSX315T

Model 71720 Xilinx Virtex-7 FPGA
- **Standard:** XC7VX330T-2
- **Optional:** XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs (Model 71620) or 24 pairs (Model 71720) to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Model 71620**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
- **Model 71720**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each

PCI-Express Interface
- **Model 71620**
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4
- **Model 71720**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71621: Transceiver with Three A/Ds, DDCs, DUC, Two D/As - XMC

The model 71621 consists of a Model 71620 as described previously, but with the addition of three multiband DDCs, one interpolator and one beamformer IP Cores installed in the Virtex-6 FPGA. These IP Cores are in addition to the factory-installed IP Modules described in the Model 71620.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Interpolator IP Core

The DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x.

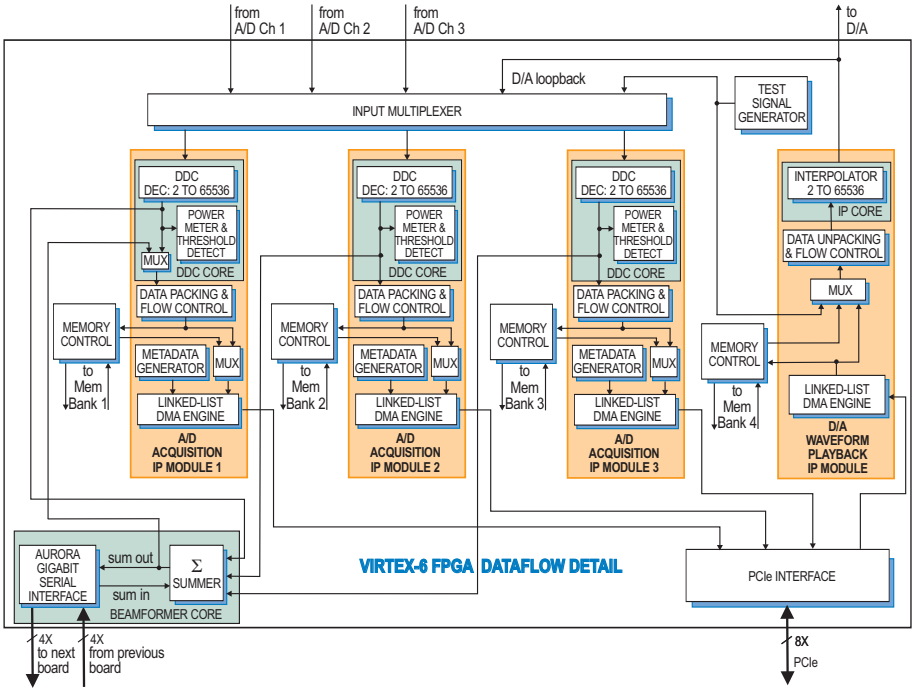
The two interpolators can be combined to crate a total range from 2x to 524,288x.

Beamformer IP Core

In addition to the DDCs, the 71621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.



Model 71621: Transceiver with Three A/Ds, DDCs, DUC, Two D/As - XMC

Also Available

Model	Format
78621	x8 PCI Express
53621	3U OpenVPX - Format 1
52621	3U OpenVPX - Format 2
56621	AMC
73621	3U cPCI - Single Density
72621	6U cPCI - Single Density
74621	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Models 71630 & 71730: 1 GHz A/D, 1 GHz D/A - XMC

Model 71630

Model 71630 is a member of the **Cobalt** family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. Model 71730 is a member of the **Onyx** family of high-performance modules based on the Virtex-7 PGA.

These high-speed data converters are suitable for connection to HF or IF ports of a communications or radar system. Their built-in data capture and playback features offer an ideal turnkey solution.

Each model includes a 1 GHz A/D and a 1 GHz D/A converter and four banks of memory. In addition to supporting PCI Express as a native interface, these models include optional general purpose and gigabit serial connectors for application-specific I/O.

Model 71730

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT or Virtex-7 FPGAs
- Model 71730: GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Model 71630: Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM; Model 71730: 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL sync bus for multimodule synchronization
- Dual-µSync clock/sync bus for multimodule synchronization
- Model 71630: PCI Express (Gen. 1 & 2) interface up to x8; Model 71730: PCI Express (Gen. 1, 2 and 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions

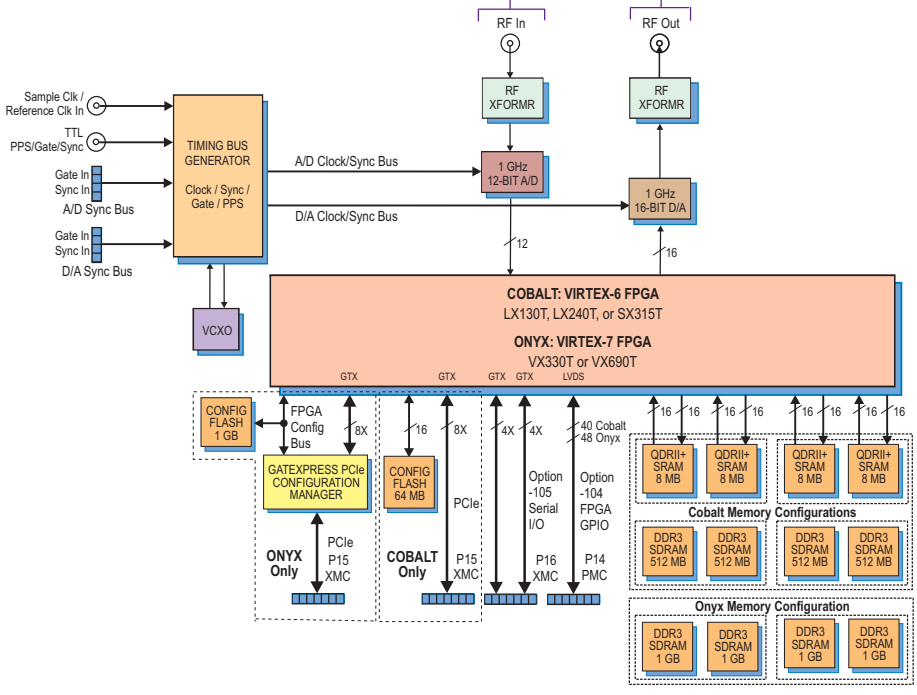
A/D Converter

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 or -7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter

Both models feature a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is transformer-coupled to a front panel SSMC connector.



Models 71630 & 71730: 1 GHz A/D, 1 GHz D/A - XMC

Installed IP Modules

The factory-installed functions in both models include an A/D acquisition and a D/A waveform playback IP module.

In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

A/D Acquisition IP Module

Both models feature an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

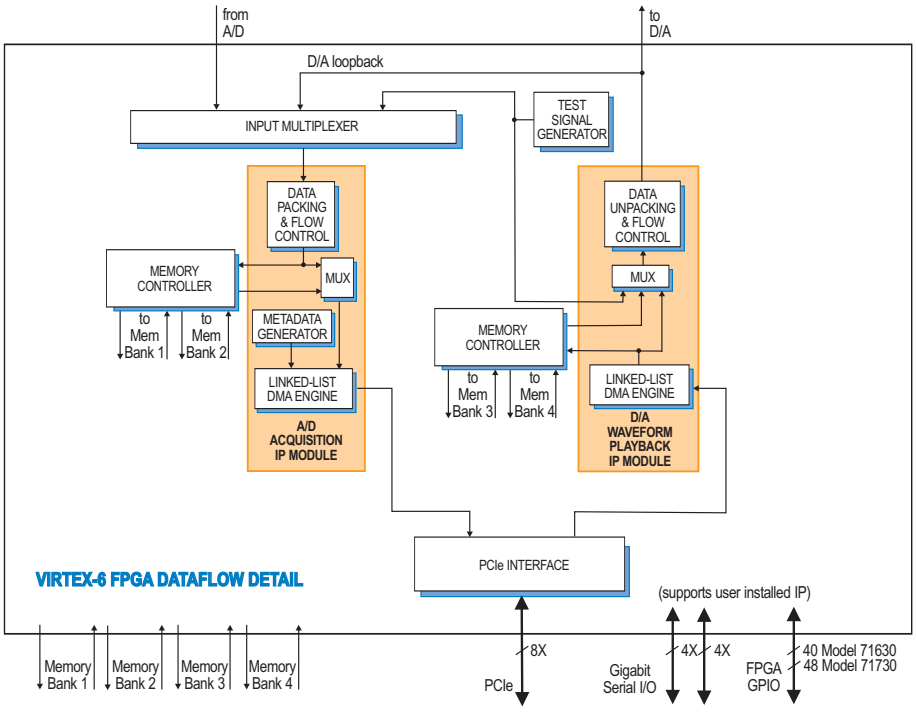
For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The factory-installed functions in these models include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.



Also Available

Cobalt

Model	Format
78630	x8 PCI Express
53630	3U OpenVPX - Format 1
52630	3U OpenVPX - Format 2
56630	AMC
73630	3U cPCI - Single Density
72630	6U cPCI - Single Density
74630	6U cPCI - Double Density

Onyx

Model	Format
78730	x8 PCI Express
53730	3U OpenVPX - Format 1
52730	3U OpenVPX - Format 2
56730	AMC
73730	3U cPCI - Single Density
72730	6U cPCI - Single Density
74730	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector, includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Model 71630 Xilinx Virtex-6 FPGA
- **Standard:** CXC6VLX130T
- **Optional:** XC6VLX240T, or XC6VSX315T

Model 71730 Xilinx Virtex-7 FPGA
- **Standard:** XC7VX330T-2
- **Optional:** XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs (Model 71630) or 24 pairs (Model 71730) to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Model 71630**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
- **Model 71730**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each, 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **Model 71630**
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4
- **Model 71730**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71640: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D - XMC

Model 71640 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71640 includes optional general purpose and gigabit serial connectors for application-specific I/O.

A/D Converter

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

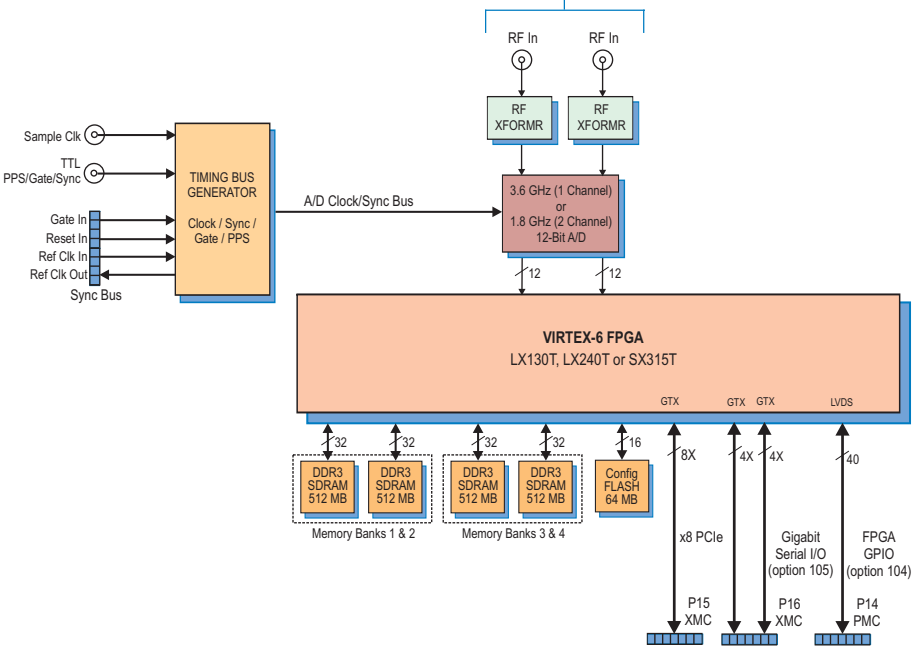
The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multimodule synchronization
- PCI Express Gen. 2 interface x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions



Installed IP Modules

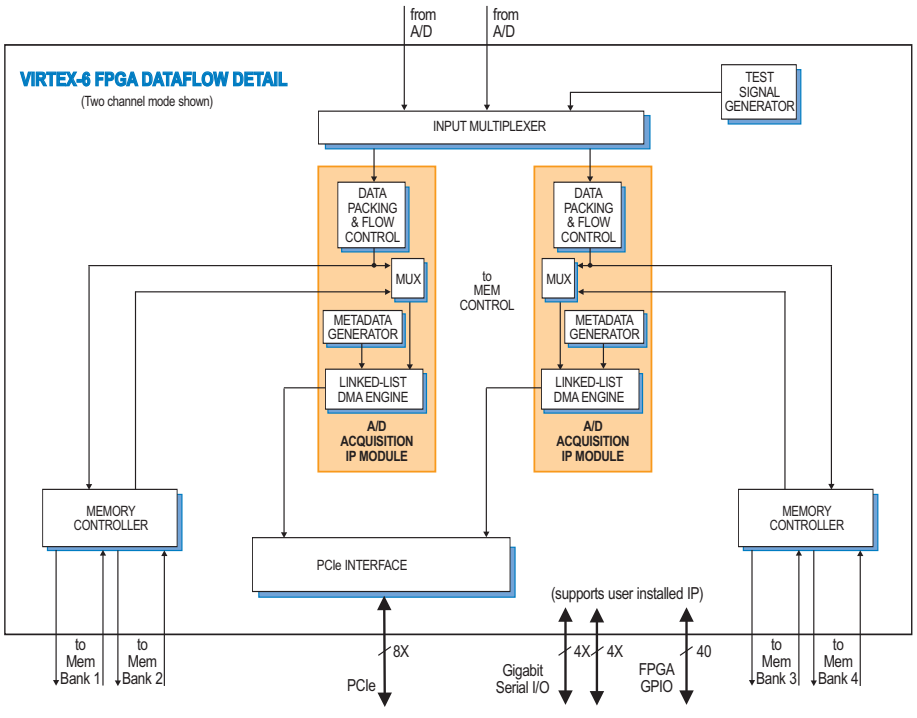
The 71640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

A/D Acquisition IP Module

The 71640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Model 71640: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D - XMC

Also Available

Model	Format
78640	x8 PCI Express
53640	3U OpenVPX - Format 1
52640	3U OpenVPX - Format 2
56640	AMC
73640	3U cPCI - Single Density
72640	6U cPCI - Single Density
74640	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71641: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, w/ DDC- XMC

The model 71641 consists of a Model 71640 as described previously, but with the addition of two wideband DDC IP Cores installed in the Virtex-6 FPGA.

These IP Cores are in addition to the factory-installed IP Modules described in the Model 71640.

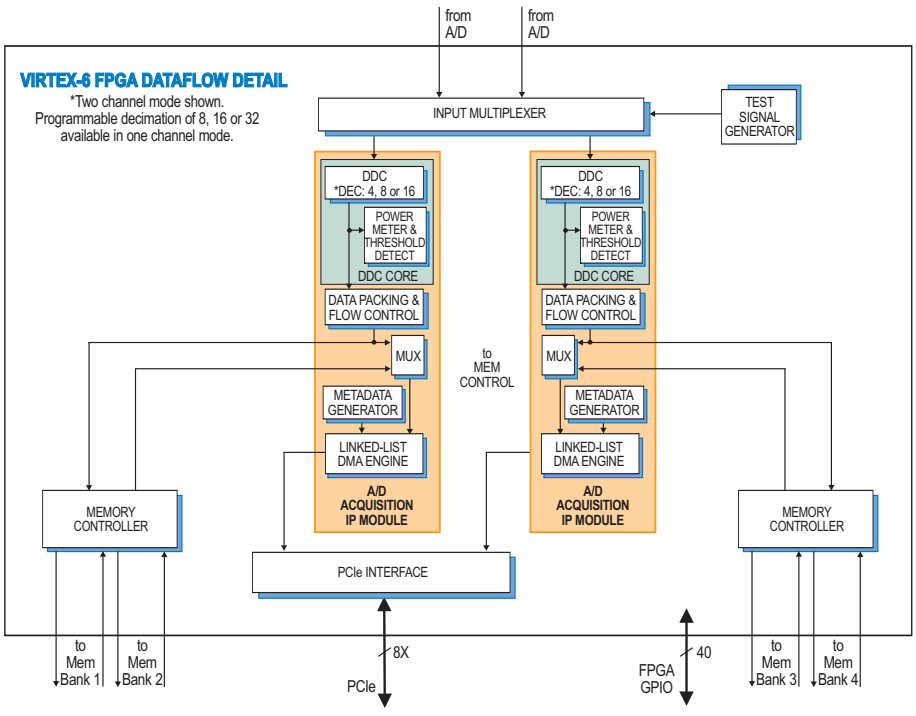
DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.



Model 71641: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, w/ DDC- XMC

Also Available

Model	Format
78641	x8 PCI Express
53641	3U OpenVPX - Format 1
52641	3U OpenVPX - Format 2
56641	AMC
73641	3U cPCI - Single Density
72641	6U cPCI - Single Density
74641	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin front panel connector, includes gate, reset, and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include trigger and gate

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71741: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, w/ DDC - XMC

Model 71741 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The model 71741 includes two wideband DDC IP cores factory-installed in the Virtex-7 FPGA.

A/D Converter

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

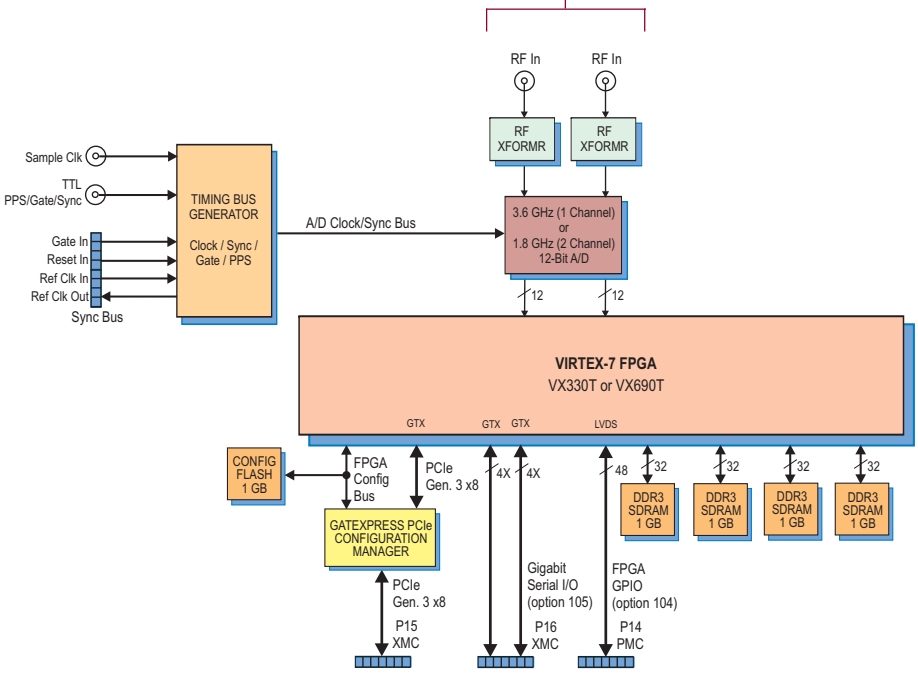
The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two- channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions



Model 71741: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, w/ DDC - XMC

Installed IP Modules

The 71741 factory-installed functions include an A/D acquisition IP module and a programmable DDC (digital downconverter). In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

A/D Acquisition IP Module

The 71741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

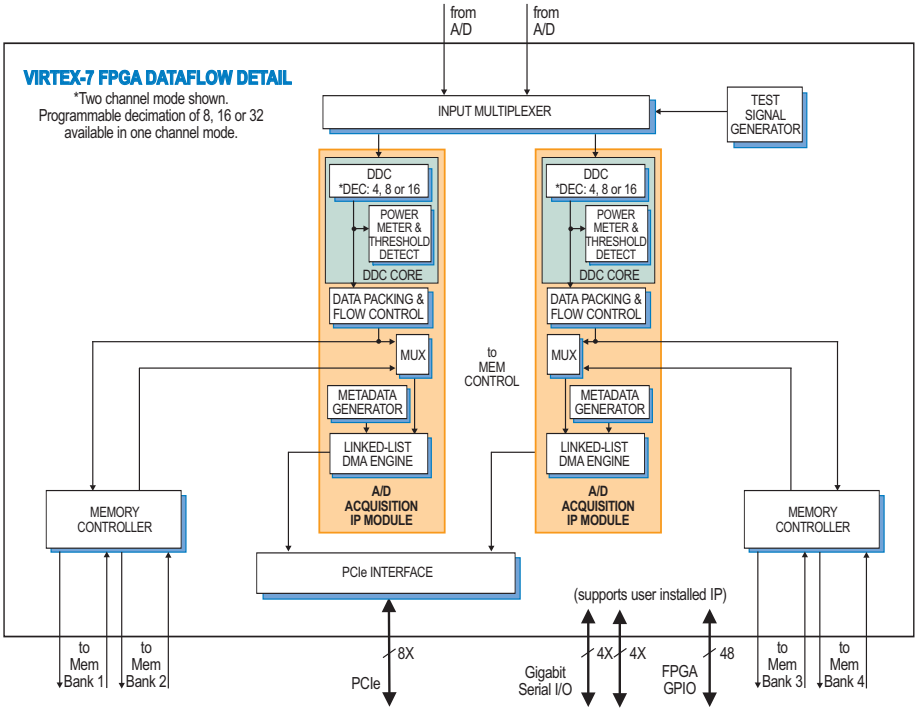
DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.



Model 71741: 1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, w/ DDC - XMC

Also Available

Model	Format
78741	x8 PCI Express
53741	3U OpenVPX - Format 1
52741	3U OpenVPX - Format 2
56741	AMC
73741	3U cPCI - Single Density
72741	6U cPCI - Single Density
74741	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71650: Transceiver with Two A/Ds, DUC, Two D/As - XMC

Model 71650 is a member of the Cobalt family of high performance XMC mod--ules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC, two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71650 includes optional general-purpose and gigabit serial card connectors for application-specific I/O.

A/D Converter

The front end accepts two full-scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/As

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA which is optionally interpolated, upconverted and then delivered to the two D/As.

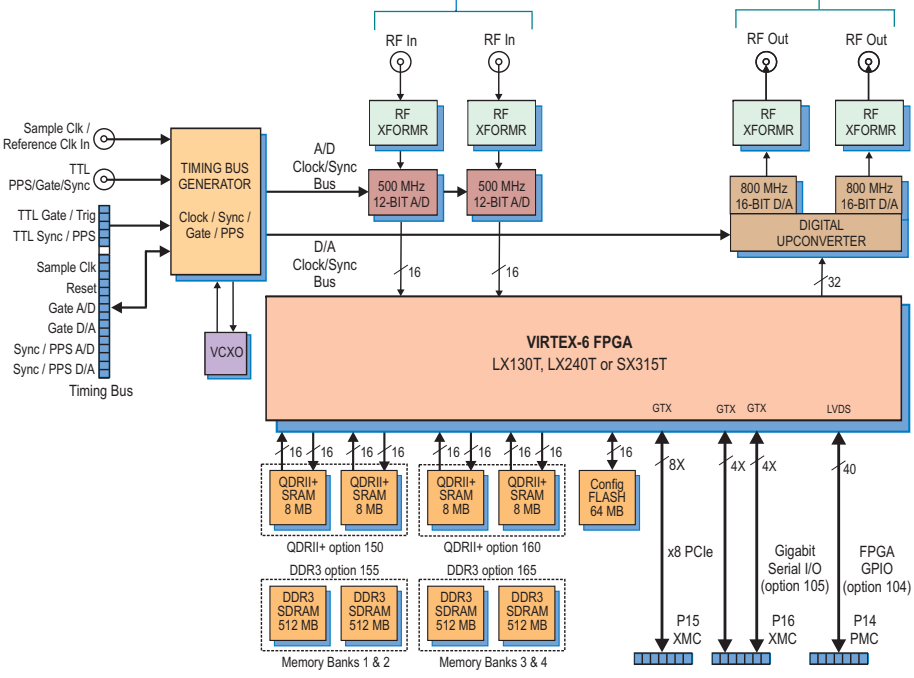
When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) digital outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A converter with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions



Installed IP Modules

The 71650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

A/D Acquisition IP Modules

The 71650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

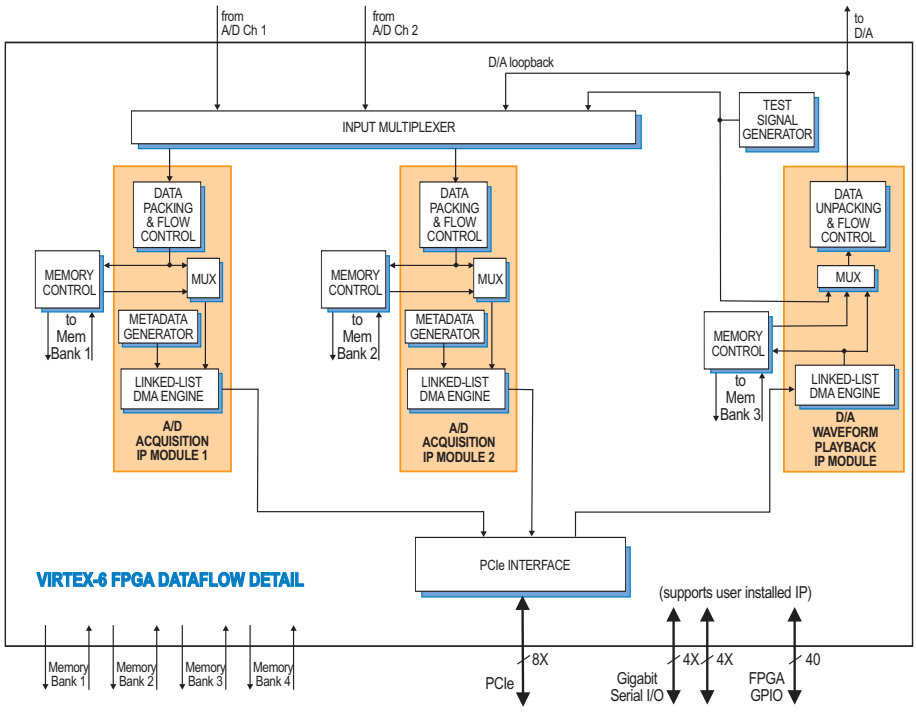
These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.



Model 71650: Transceiver with Two A/Ds, DUC, Two D/As - XMC

Also Available

Model	Format
78650	x8 PCI Express
53650	3U OpenVPX - Format 1
52650	3U OpenVPX - Format 2
56650	AMC
73650	3U cPCI - Single Density
72650	6U cPCI - Single Density
74650	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen.1 or Gen.2, x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71651: Transceiver with Two A/Ds, DDC, DUC, Two D/As - XMC

The model 71651 consists of a Model 71650 as described previously, but with the addition of two powerful DDCs and a beamformer IP Cores installed in the Virtex-6 FPGA. These IP Cores are in addition to the factory-installed IP modules described in the Model 71650.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

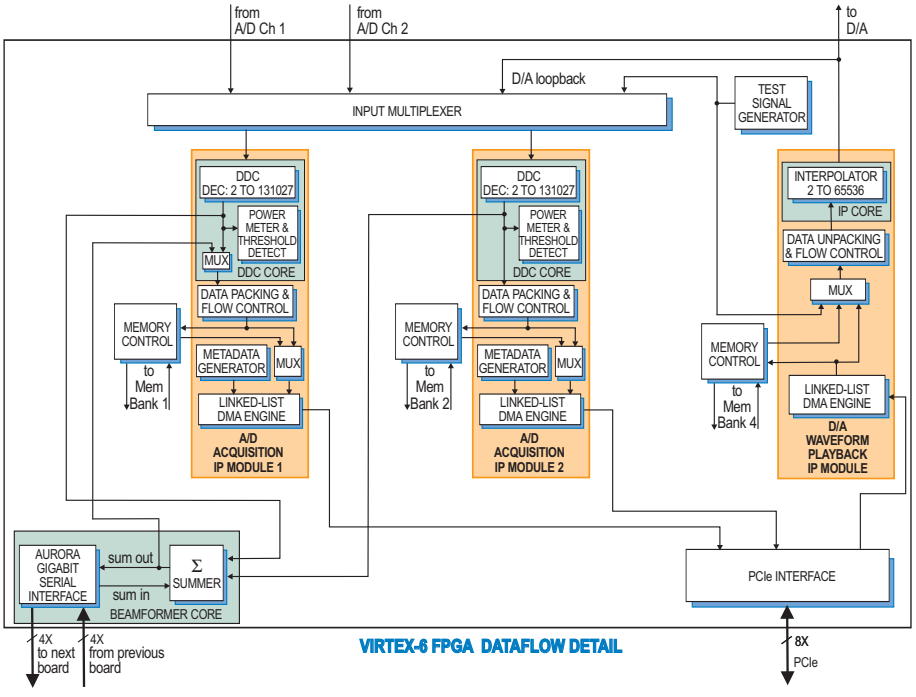
In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71651's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.



VIRTEX-6 FPGA DATAFLOW DETAIL

Model 71651: Transceiver with Two A/Ds, DDC, DUC, Two D/As - XMC

Also Available

Model	Format
78651	x8 PCI Express
53651	3U OpenVPX - Format 1
52651	3U OpenVPX - Format 2
56651	AMC
73651	3U cPCI - Single Density
72651	6U cPCI - Single Density
74651	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC, 2.91 in. x 5.87 in.

Model 71751: Transceiver with Two A/Ds, DDC, DUC, Two D/As - XMC

Model 71751 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turn-key solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71751 includes a general-purpose connector for application-specific I/O.

A/D Converters

The front end accepts two full-scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer-coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

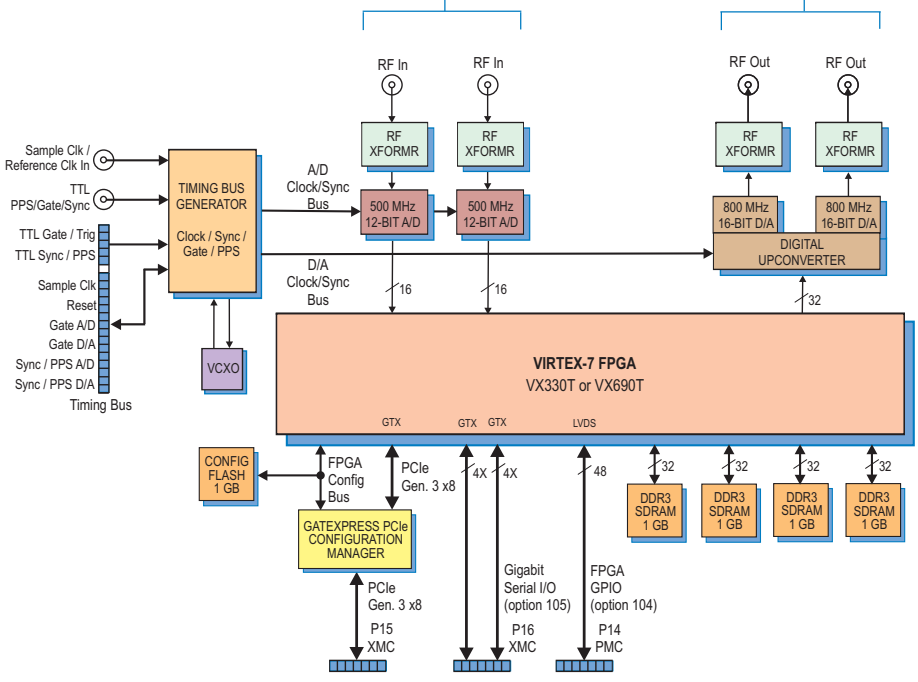
The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/As

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA which is optionally interpolated, upconverted and then delivered to the two D/As.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) digital outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A converter with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. An FPGA-based interpolator provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds

Contact Pentek for availability of rugged and conduction-cooled versions

Model 71751: Transceiver with Two A/Ds, DDC, DUC, Two D/As - XMC

Installed IP Modules

The 71751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

A/D Acquisition IP Modules

The 71751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Core

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

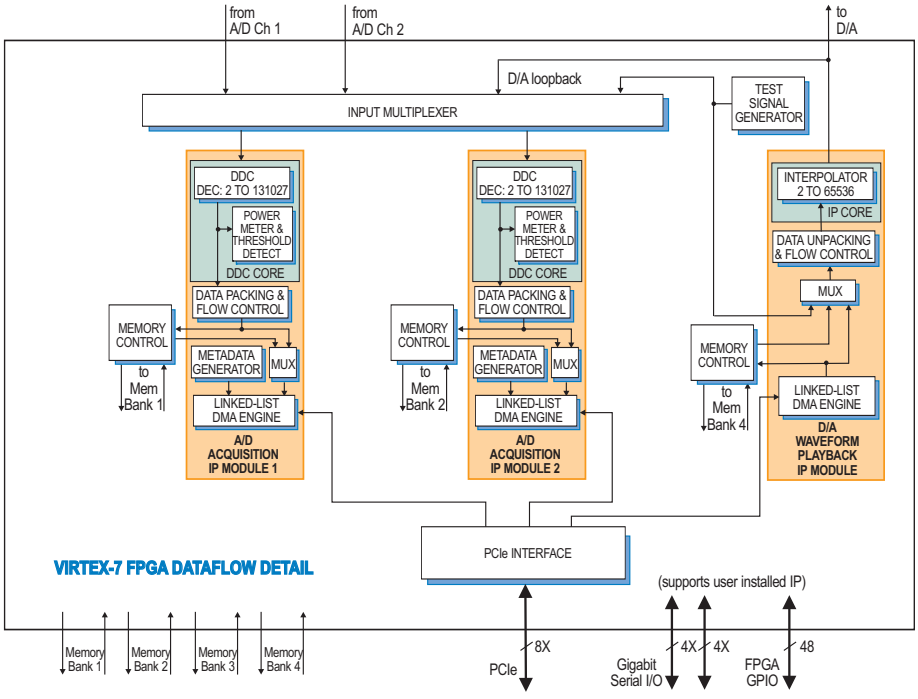
The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 71751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.



Model 71751: Transceiver with Two A/Ds, DDC, DUC, Two D/As - XMC

Also Available

Model	Format
78751	x8 PCI Express
53751	3U OpenVPX - Format 1
52751	3U OpenVPX - Format 2
56751	AMC
73751	3U cPCI - Single Density
72751	6U cPCI - Single Density
74751	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front-panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (optional)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front-panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front-panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Models 71660 & 71760: 4-Channel 200 MHz A/D - XMC

Model 71660

Model 71760

Model 71660 is a member of the **Cobalt** family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. Model 71760 is a member of the **Onyx** family of high-performance modules based on the Virtex-7 FPGA.

These multichannel, high-speed data converters, are suitable for connection to HF or IF ports of a communications or radar system. Their built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

Each model includes four A/Ds and four banks of memory. In addition to supporting PCI Express as a native interface, these models include general-purpose and gigabit serial connectors for application-specific I/O .

Features

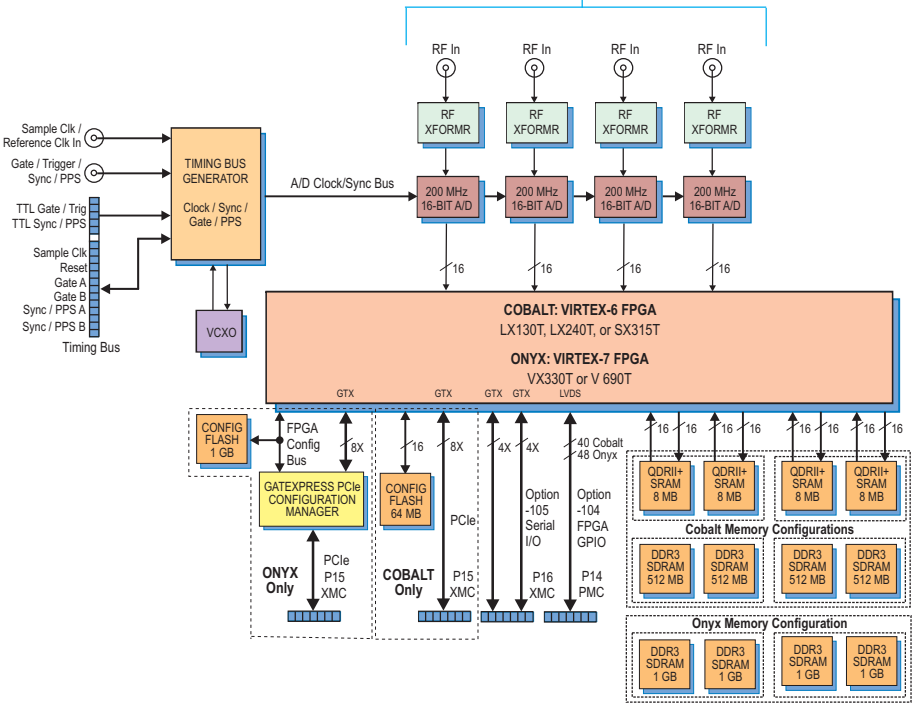
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT or Virtex-7 VXT FPGAs
- Model 71720: GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Model 71660: Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM; Model 71760: 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Model 71660: PCI Express (Gen. 1 & 2) interface up to x8; Model 71760: PCI Express (Gen. 1, 2, and 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converters

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the FPGA for signal processing, data capture or for routing to other module resources.



Installed IP Modules

The factory-installed functions in both models include four A/D acquisition IP modules.

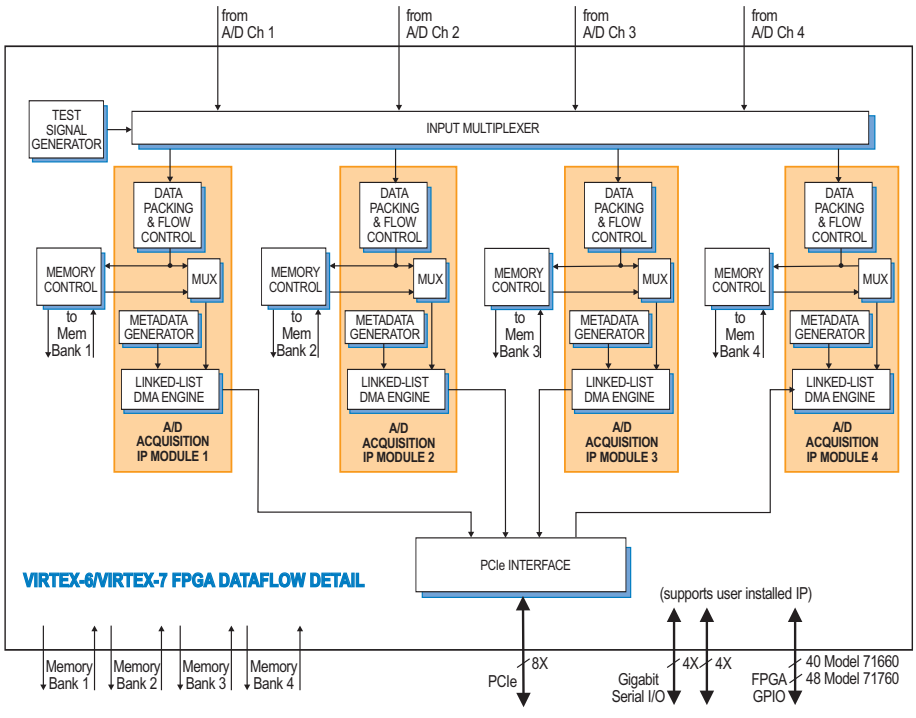
IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions without the need to develop any FPGA IP.

A/D Acquisition IP Modules

Both models feature four A/D Acquisition IP modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Models 71660 & 71760: 4-Channel 200 MHz A/D - XMC

Also Available

Model	Format
78660	x8 PCI Express
53660	3U OpenVPX - Format 1
52660	3U OpenVPX - Format 2
56660	AMC
73660	3U cPCI - Single Density
72660	6U cPCI - Single Density
74660	6U cPCI - Double Density

Model	Format
78760	x8 PCI Express
53760	3U OpenVPX - Format 1
52760	3U OpenVPX - Format 2
56760	AMC
73760	3U cPCI - Single Density
72760	6U cPCI - Single Density
74760	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Model 71660 Xilinx Virtex-6 FPGA
- **Standard:** XC6VLX130T
- **Optional:** XC6VLX240T or XC6VSX315T

Model 71760 Xilinx Virtex-7 FPGA
- **Standard:** XC7VX330T-2
- **Optional:** XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs (Model 71660) or 24 pairs (Model 71760) to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Model 71660**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
- **Model 71760**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each

PCI-Express Interface
- **Model 71660**
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4
- **Model 71760**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71661: 4-Channel 200 MHz A/D with DDCs and Beamformer - XMC

The model 71661 consists of a Model 71660 as described previously, but with the addition of four multiband DDCs, and one beamformer IP Cores installed in the Virtex-6 FPGA. These IP Cores are in addition to the factory-installed IP Modules described in the Model 71660.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

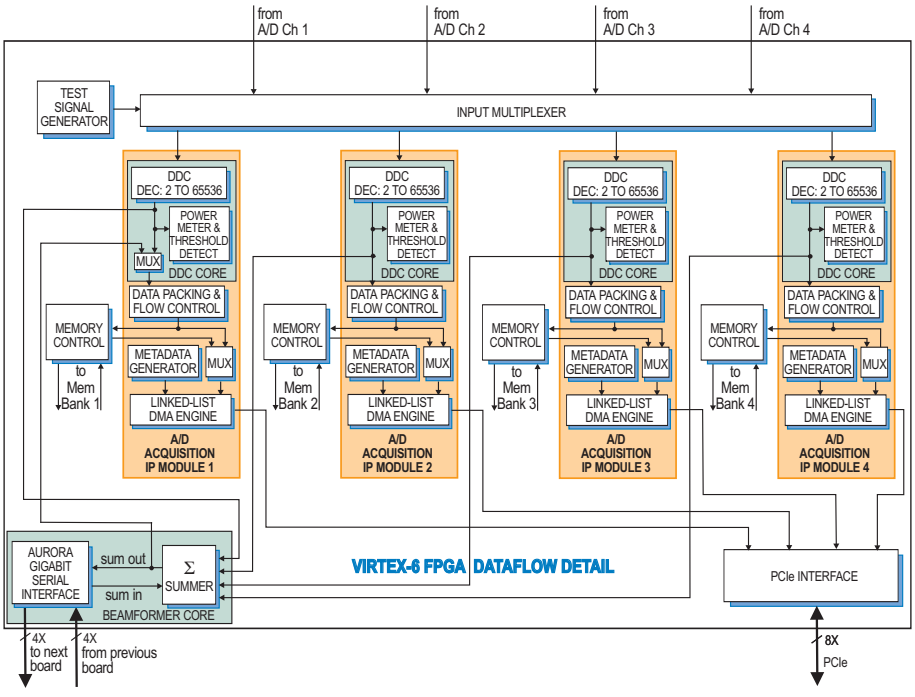
The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.



Model 71661: 4-Channel 200 MHz A/D with DDCs and Beamformer - XMC

Also Available

Model	Format
78661	x8 PCI Express
53661	3U OpenVPX - Format 1
52661	3U OpenVPX - Format 2
56661	AMC
73661	3U cPCI - Single Density
72661	6U cPCI - Single Density
74661	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71662: 4-Channel 200 MHz A/D with 32-Channel DDC - XMC

The Model 71662 consists of a Model 71660 as described previously, but with the addition of four 8-Channel DDC IP Cores installed in the Virtex-6 FPGA.

These IP Cores are in addition to the factory-installed IP Modules described in the Model 71660.

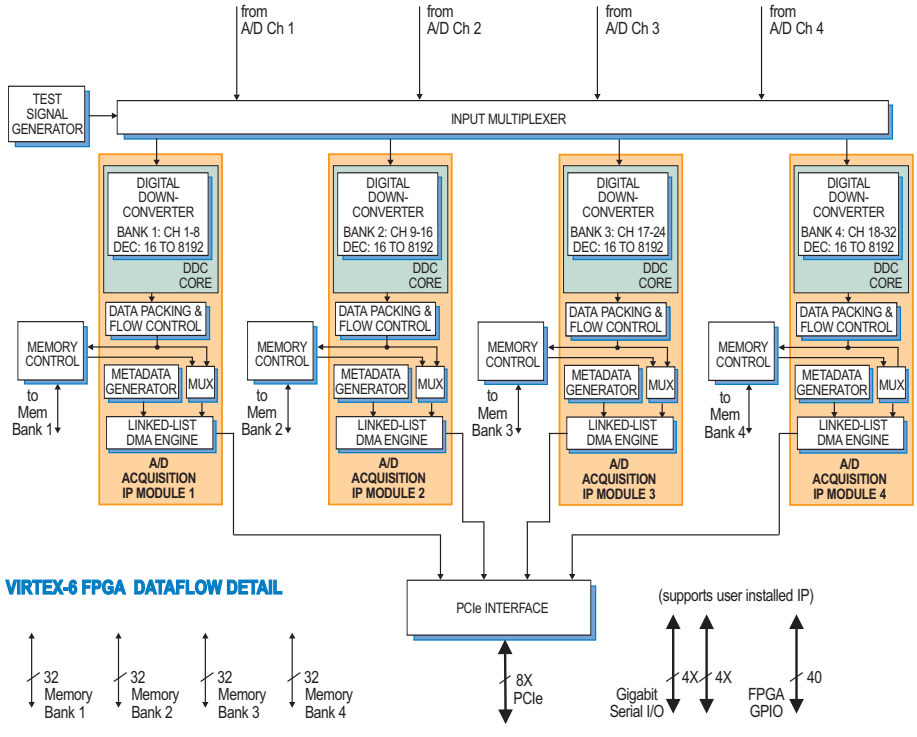
DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.



Model 71662: 4-Channel 200 MHz A/D with 32-Channel DDC - XMC

Also Available

Model	Format
78662	x8 PCI Express
53662	3U OpenVPX - Format 1
52662	3U OpenVPX - Format 2
56662	AMC
73662	3U cPCI - Single Density
72662	6U cPCI - Single Density
74662	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71663: 1100 GSM Channelizer with Quad A/D - XMC

The Model 71663 consists of a Model 71660 as described previously, but with the addition of 1100 GSM channelizer cores installed in the Virtex-6 FPGA.

These IP Cores are in addition to the factory-installed IP Modules described in the Model 71660.

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

GSM Channelizers

The 71663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Before connection to the 71663, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45, 135, or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 71663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively.

Super Channel Engines

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, exceeding the 4 GB/sec peak rate of PCIe Gen. 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "super channel". This results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen. 2 x8 interface.

Super Channel Packets and Headers

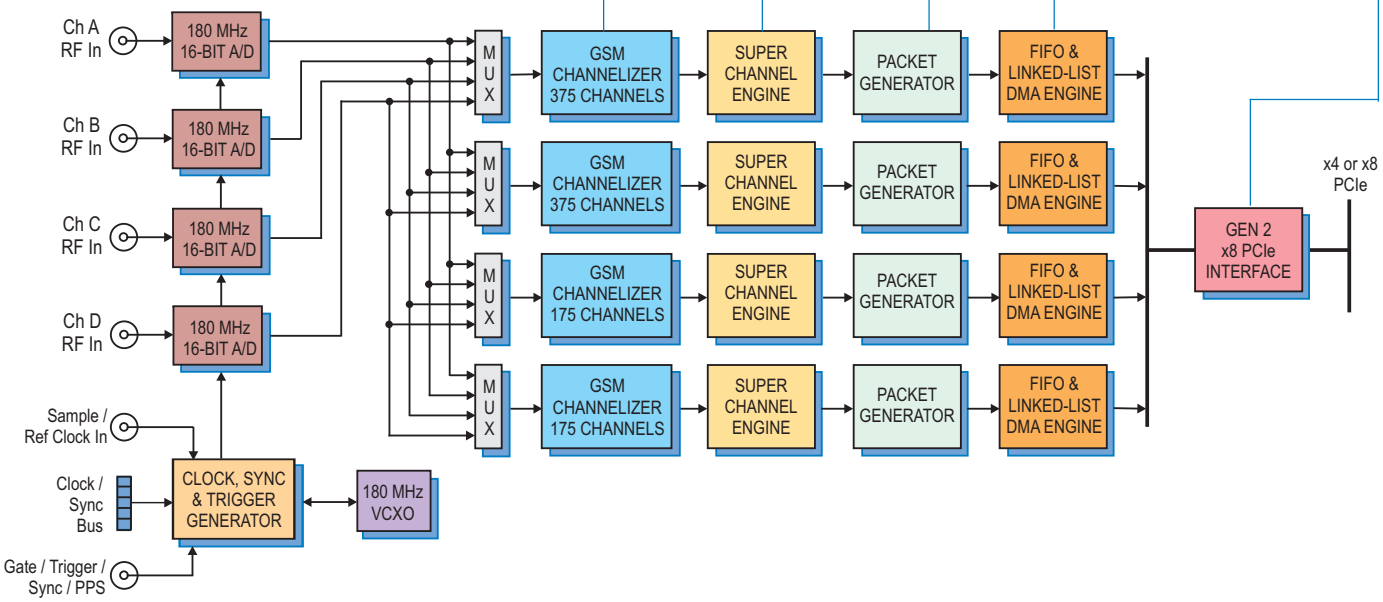
Super channel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining data "payload" samples can be identified and recovered by the host.

PCI Express Interface

The Model 71663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 71663 and host.



Model 71663: 1100 GSM Channelizer with Quad A/D - XMC

Also Available

Model	Format
78663	x8 PCI Express
53663	3U OpenVPX - Format 1
52663	3U OpenVPX - Format 2
56663	AMC
73663	3U cPCI - Single Density
72663	6U cPCI - Single Density
74663	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front-panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- and 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Frequencies:** IF Freq ± k ∗ 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s**: Resampled to 180 MHz∗13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Super Channels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: $-f_s/4$ (-270.8333 kHz)
  - Second: 0 Hz
  - Third: $+f_s/4$ (+270.8333 kHz)
  - Fourth: $+f_s/2$ (+541.666 kHz)

Superchannel Sample Rate: f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71670: 4-Channel 1.25 GHz D/A with DUC - XMC

Model 71670 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

The 71670 includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O.

Digital Upconverter and D/A

Two Texas Instruments DAC3484s provide four DUC (Digital Upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

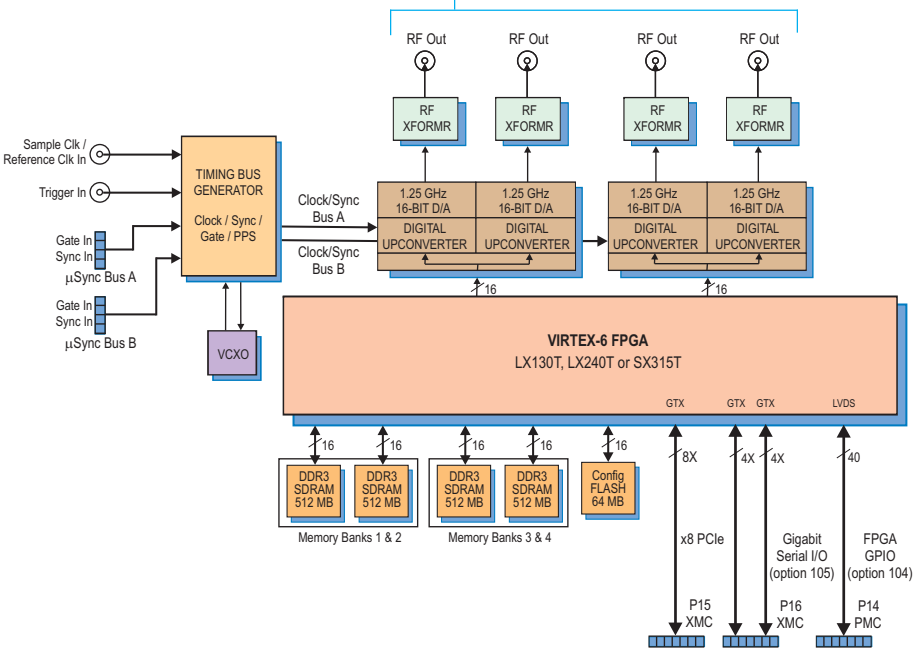
When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Transformer-coupled analog output is through four front panel SSMC connectors.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions



Model 71670: 4-Channel 1.25 GHz D/A with DUC - XMC

Installed IP Modules

The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

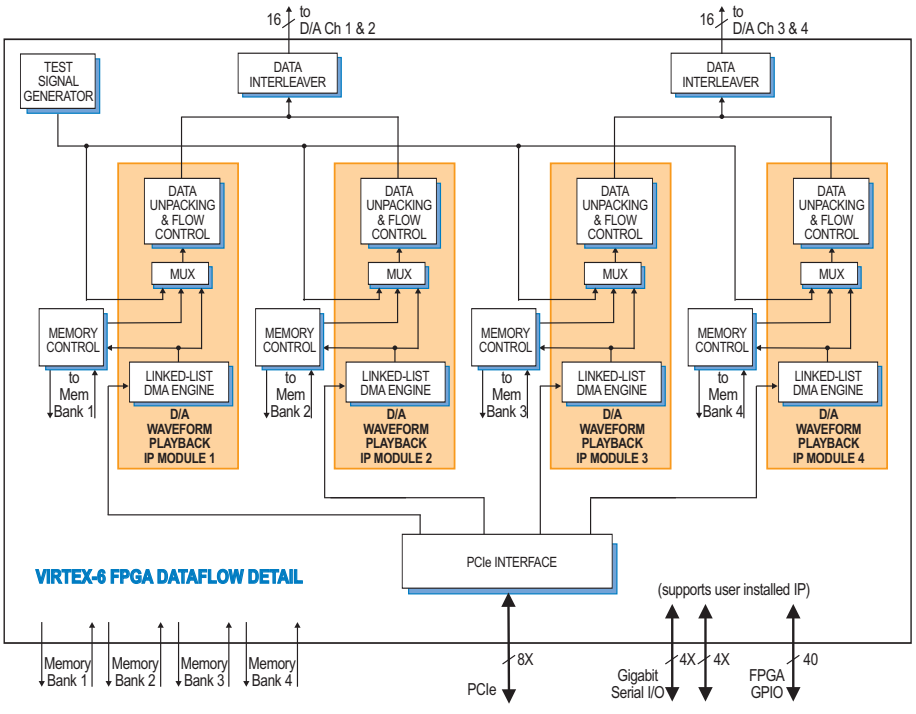
D/A Waveform Playback IP Module

The Model 71670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



Model 71670: 4-Channel 1.25 GHz D/A with DUC - XMC

Also Available

Model	Format
78670	x8 PCI Express
53670	3U OpenVPX - Format 1
52670	3U OpenVPX - Format 2
56670	AMC
73670	3U cPCI - Single Density
72670	6U cPCI - Single Density
74670	6U cPCI - Double Density

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, sync and gate/trigger inputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

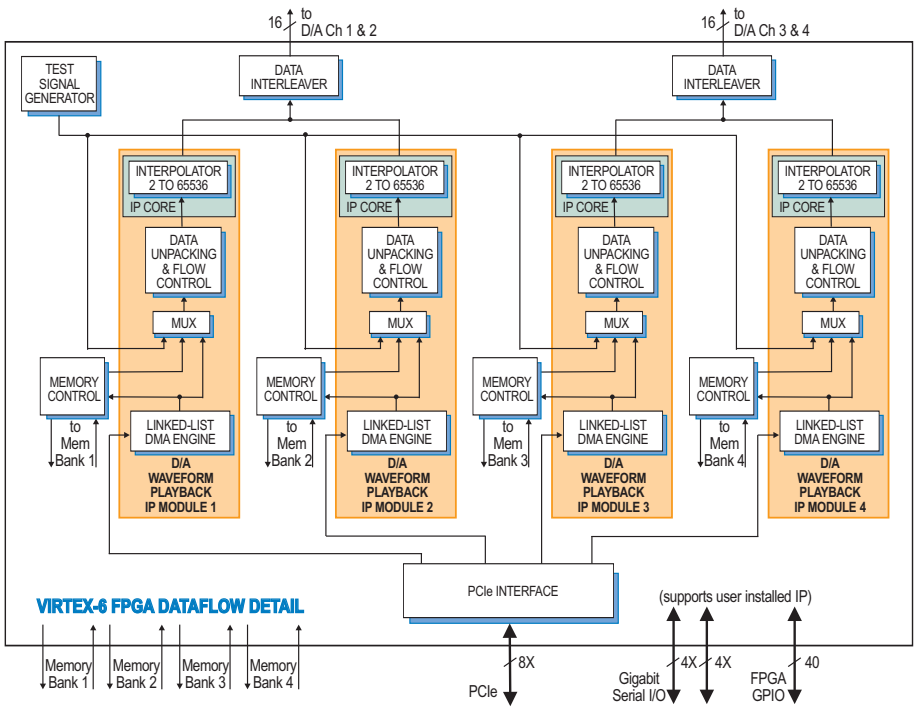
Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71671: 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation - XMC

The model 71671 consists of a Model 71670 as described previously, but with the addition of four wide-range programmable interpolation IP Cores installed in the Virtex-6 FPGA. Installed in each of the four channels, these IP Cores are in addition to the factory-installed IP modules described in the Model 71670.

Interpolator IP Core

In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems.



Model 71671: 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation - XMC

Also Available

Model	Format
78671	x8 PCI Express
53671	3U OpenVPX - Format 1
52671	3U OpenVPX - Format 2
56671	AMC
73671	3U cPCI - Single Density
72671	6U cPCI - Single Density
74671	6U cPCI - Double Density

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, sync and gate/trigger inputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71771: 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation - XMC

Model 71771 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71771 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

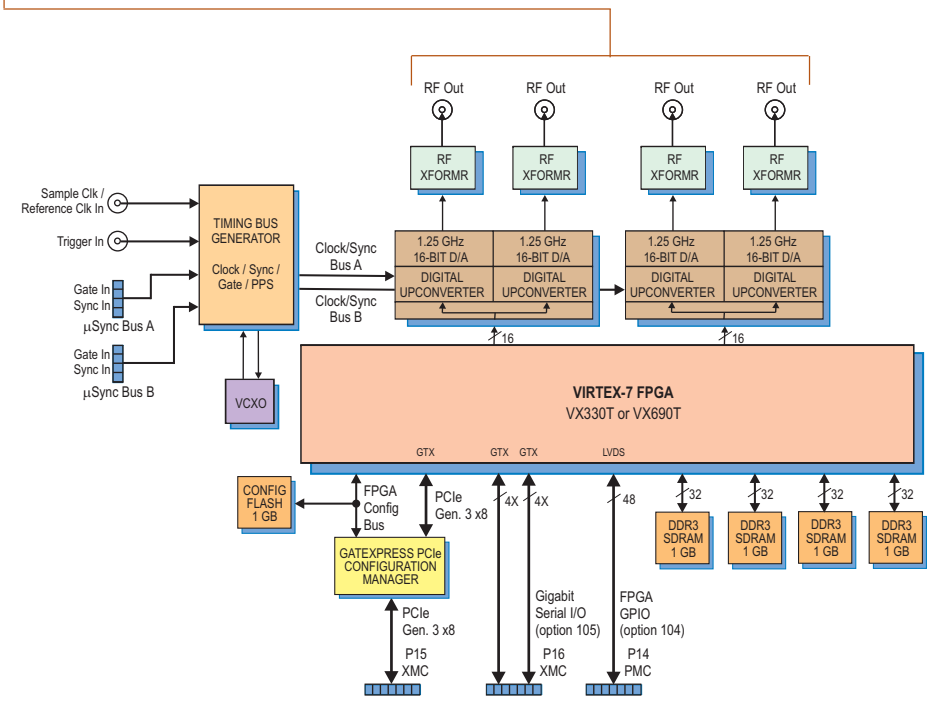
Contact Pentek for availability of rugged and conduction-cooled versions

Digital Upconverter and D/A

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Transformer-coupled analog outputs are through four front panel SSMC connectors.



Model 71771: 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation - XMC

Installed IP Modules

The 71771 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters.

IP modules for an interpolation engine, DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71771 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Waveform Playback IP Module

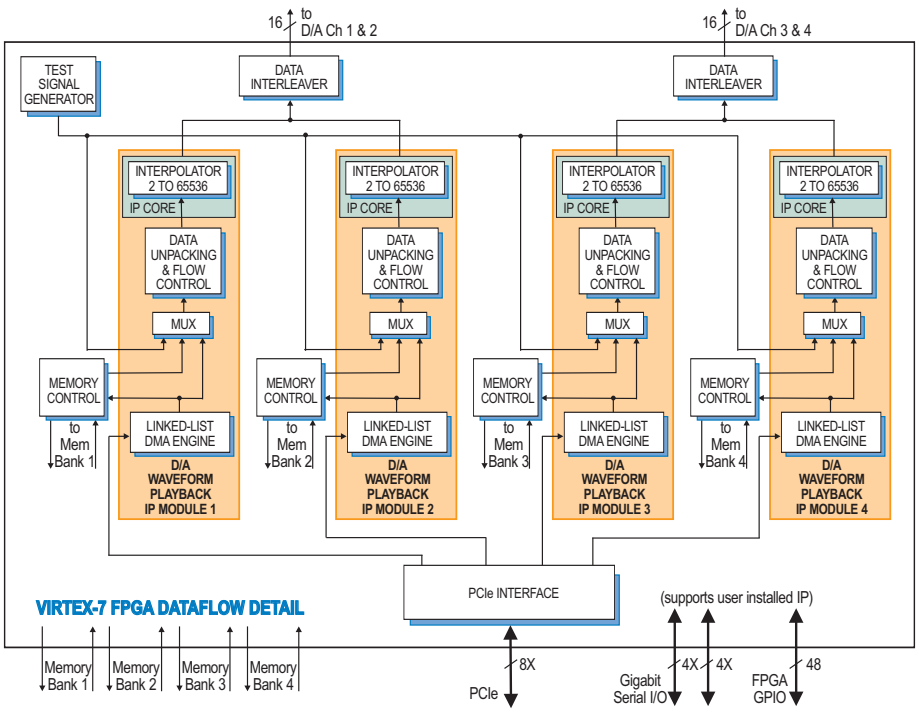
The Model 71771 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

Interpolator IP Core

In addition to the DAC3484, the 71771 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems.



Model 71771: 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation - XMC

Also Available

Model	Format
78771	x8 PCI Express
53771	3U OpenVPX - Format 1
52771	3U OpenVPX - Format 2
56771	AMC
73771	3U cPCI - Single Density
72771	6U cPCI - Single Density
74771	6U cPCI - Double Density

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO, front panel external clock or µSync timing buses
- **Synchronization:** Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX485T-2, or XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71690: L-Band RF Tuner with 2-Channel 200 MHz A/D - XMC

Model 71690 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71690 includes general purpose and gigabit serial connectors for application-specific I/O.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 80 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multimodule synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions

RF Tuner

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

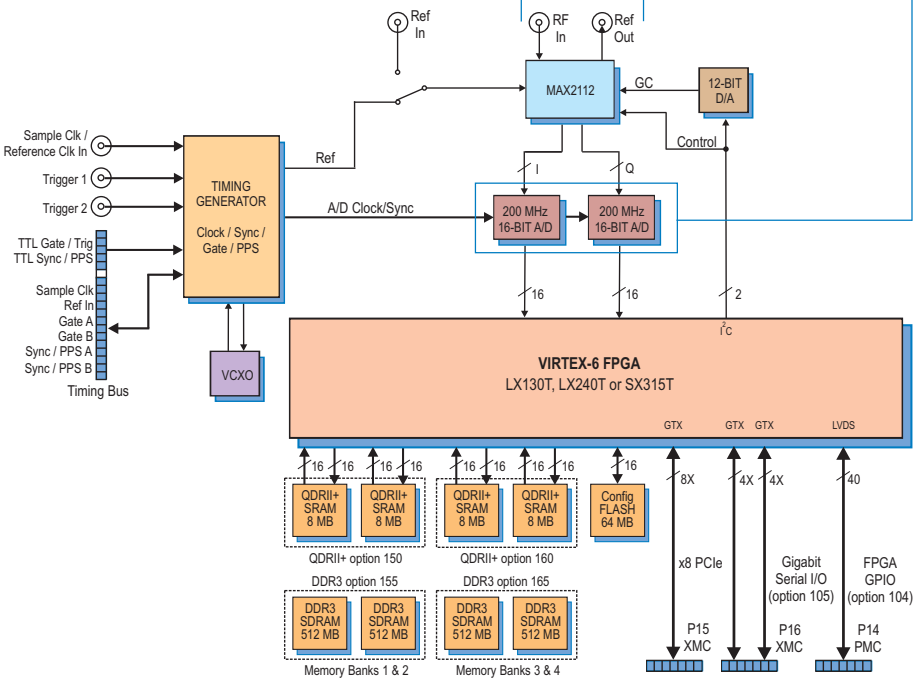
The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase- locked loop) synthesized local oscillator, quadrature (I + Q) down-converting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to an on-board crystal, the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable-gain range of more than 80 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converters

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.



Model 71690: L-Band RF Tuner with 2-Channel 200 MHz A/D - XMC

Installed IP Modules

The 71690 factory-installed functions include two A/D acquisition IP modules.

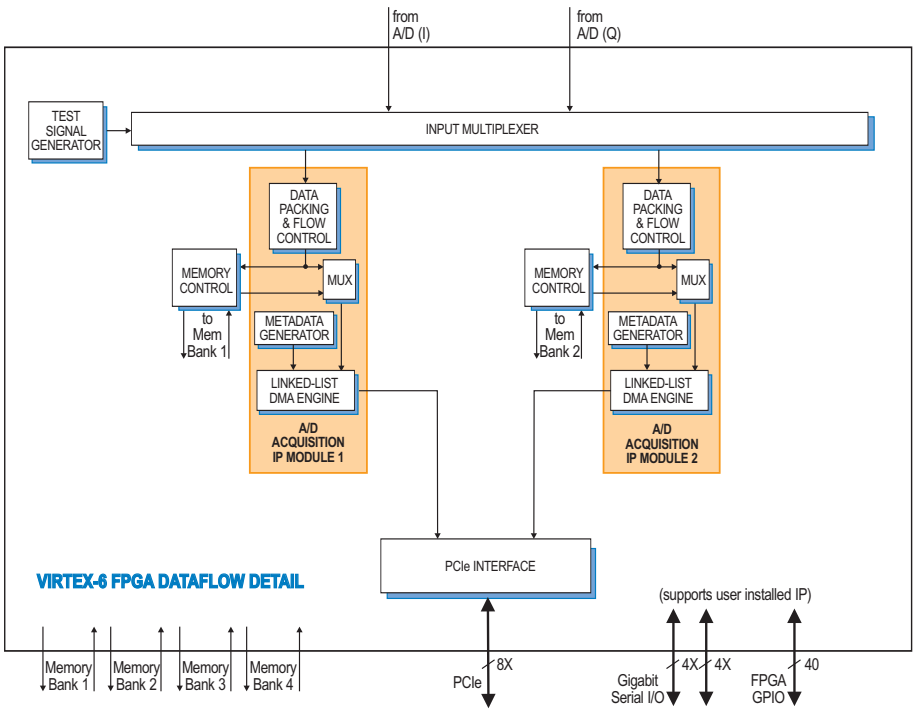
IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

A/D Acquisition IP Modules

The 71690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Model 71690: L-Band RF Tuner with 2-Channel 200 MHz A/D - XMC

Also Available

Model	Format
78690	x8 PCI Express
53690	3U OpenVPX - Format 1
52690	3U OpenVPX - Format 2
56690	AMC
73690	3U cPCI - Single Density
72690	6U cPCI - Single Density
74690	6U cPCI - Double Density

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
- **Dynamic Range:** -75 dBm to 0 dBm

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

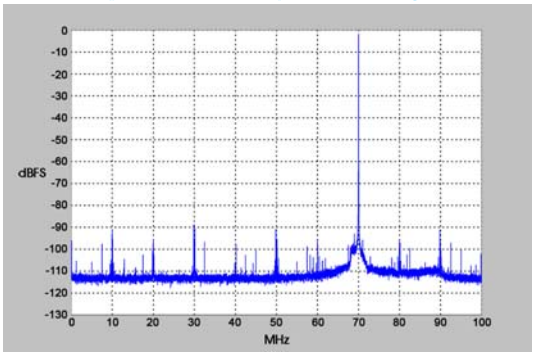
Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Performance Graphs

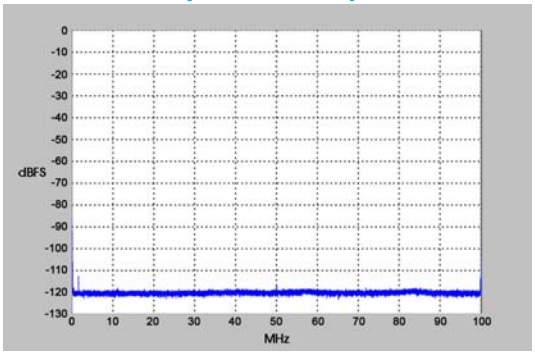
A/D Performance: Models 71620, 71720, 71621, 71660, 71760, 71661, 71761, 71662, 71762

Spurious Free Dynamic Range



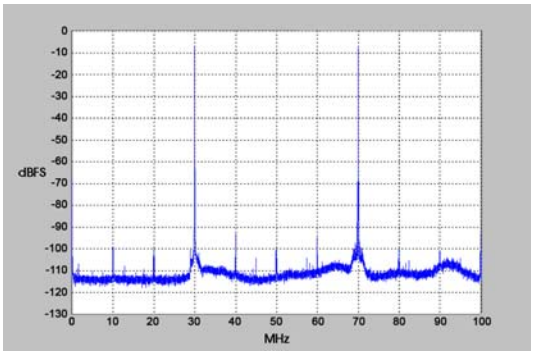
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



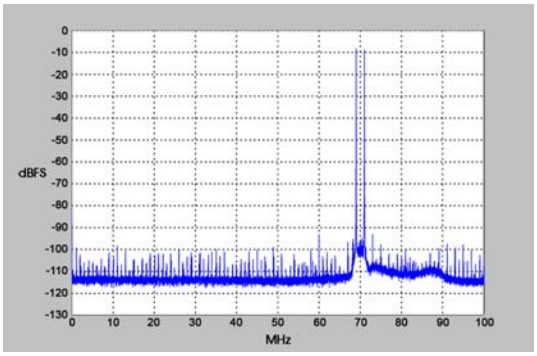
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



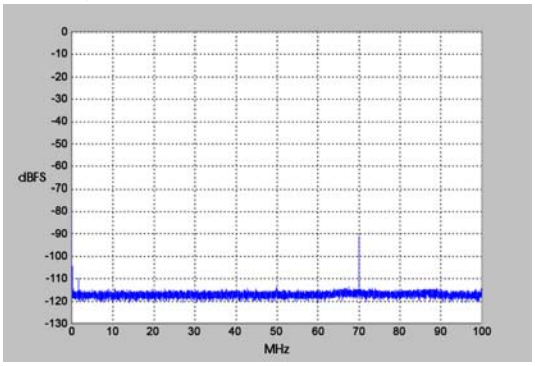
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



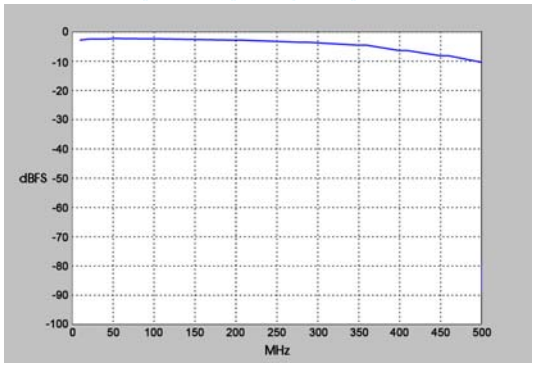
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk Crosstalk



$f_{in\ Ch2}$ = 70 MHz, f_s = 200 MHz, Ch 1 shown

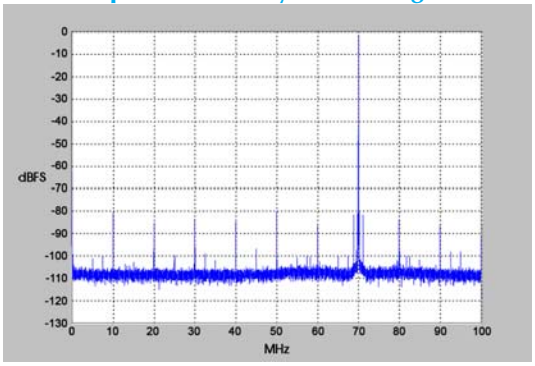
Input Frequency Response



f_s = 200 MHz, Internal Clock

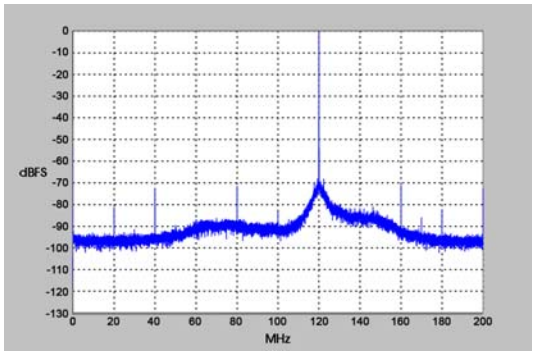
D/A Performance: Models 71620, 71621, 71720

Spurious Free Dynamic Range



f_{out} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Free Dynamic Range



f_{out} = 120 MHz, f_s = 400 MHz, External Clock

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Model 71610: LVDS Digital I/O with Virtex-6 FPGA - XMC

Model 71610 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector.

Its built-in data capture and data generation feature offers an ideal turn-key solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board

Contact Pentek for availability of rugged and conduction-cooled versions

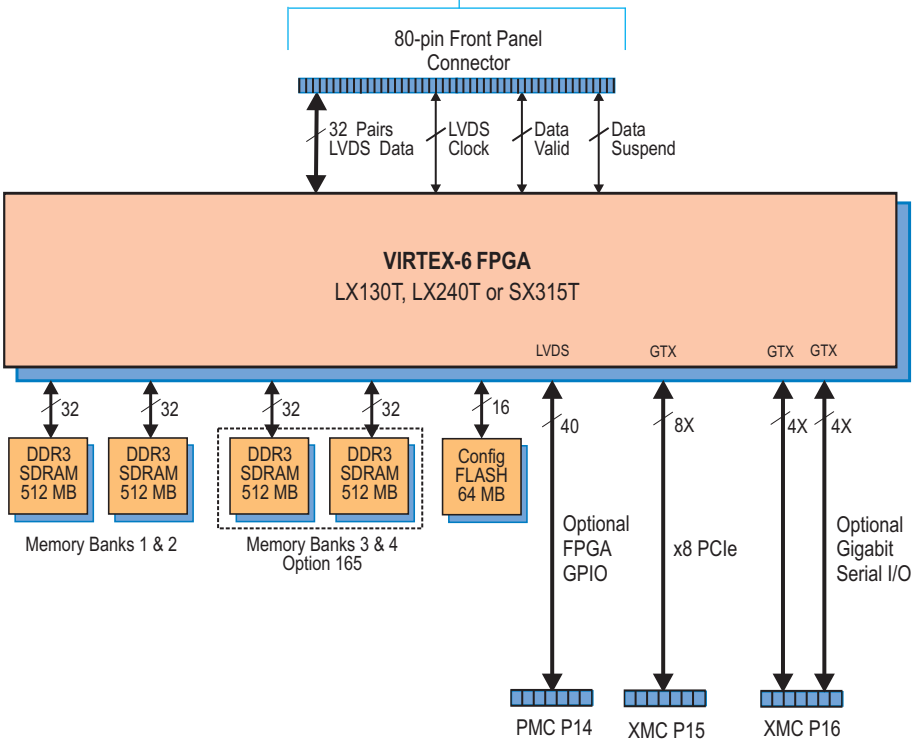
Acquisition IP Module

The module can be configured for digital input mode by setting a jumper on the board. In this case, the module accepts input data Clock and input Data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The module can optionally generate a Data Suspend output signal indicating that the 71610 is no longer capable of accepting data. The module accepts 32 bits from the front panel connector or from an on-board test signal generator.

Generation IP Module

The module can be configured for digital output mode by setting a jumper on the board. In this case, the module generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The module can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory.



Model 71610: LVDS Digital I/O with Virtex-6 FPGA - XMC

Also Available

Model	Format
78610	x8 PCI Express
53610	3U OpenVPX - Format 1
52610	3U OpenVPX - Format 2
56610	AMC
73610	3U cPCI - Single Density
72610	6U cPCI - Single Density
74610	6U cPCI - Double Density

Installed IP Modules

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

XMC Interface

The Model 71610 complies with the VITA 42.0 XMC specification. Each of two connectors provides multilane gigabit serial interfaces with up to a 6 GHz bit clock. With dual XMC connectors, the 71610 supports x4 or x8 PCIe on the primary P15 XMC connector. The secondary P16 XMC connector is used for dual 4X or single 8X user-installed gigabit serial interfaces, such as Aurora, PCIe, and serial RapidIO.

PCI Express Interface

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Memory Resources

The 71610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

Specifications

Front Panel Input/Output

Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
Clock: One LVDS differential pair, 2.5 V compliant
Data Valid: One LVDS differential pair, 2.5 V compliant
Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71611: Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

Model 71611 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, gigabit serial interface, it is ideal for interfacing to serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general-purpose connector for application-specific I/O.

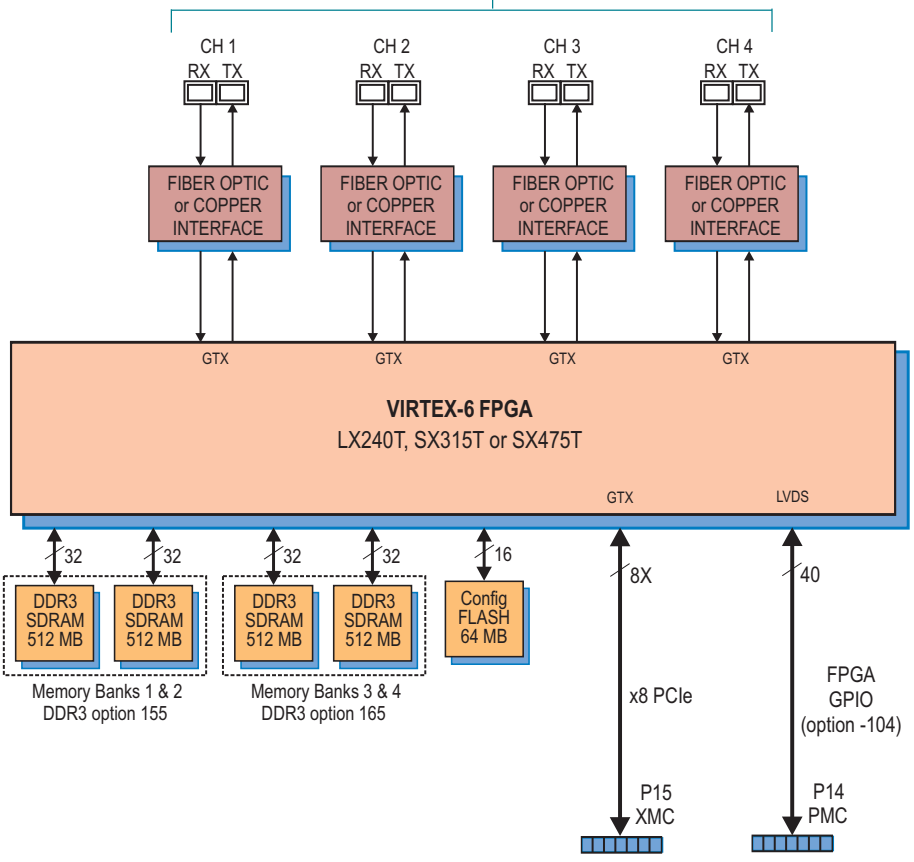
Serial FPDP Interface

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Features

- Complete serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O

Contact Pentek for availability of rugged and conduction-cooled versions



Model 71611: Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

Also Available

Model	Format
78611	x8 PCI Express
53611	3U OpenVPX - Format 1
52611	3U OpenVPX - Format 2
56611	AMC
73611	3U cPCI - Single Density
72611	6U cPCI - Single Density
74611	6U cPCI - Double Density

Installed IP Modules

Four identical serial FPDP interfaces are installed in the FPGA. The interfaces are fully compatible with the VITA 17.1 serial FPDP specification.

Each interface includes a serial FPDP TX and a serial FPDP RX engine. These are enhanced with DMA engines for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- **Fiber Optic Connector Type:** LC
- **Laser:** 850 nm (standard, other options available)
- **Copper Connector Type:** Micro Twinax
- **Fiber Optic or Copper Link Rates:** 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- **Fiber Optic or Copper Data Transfer Rates:** 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

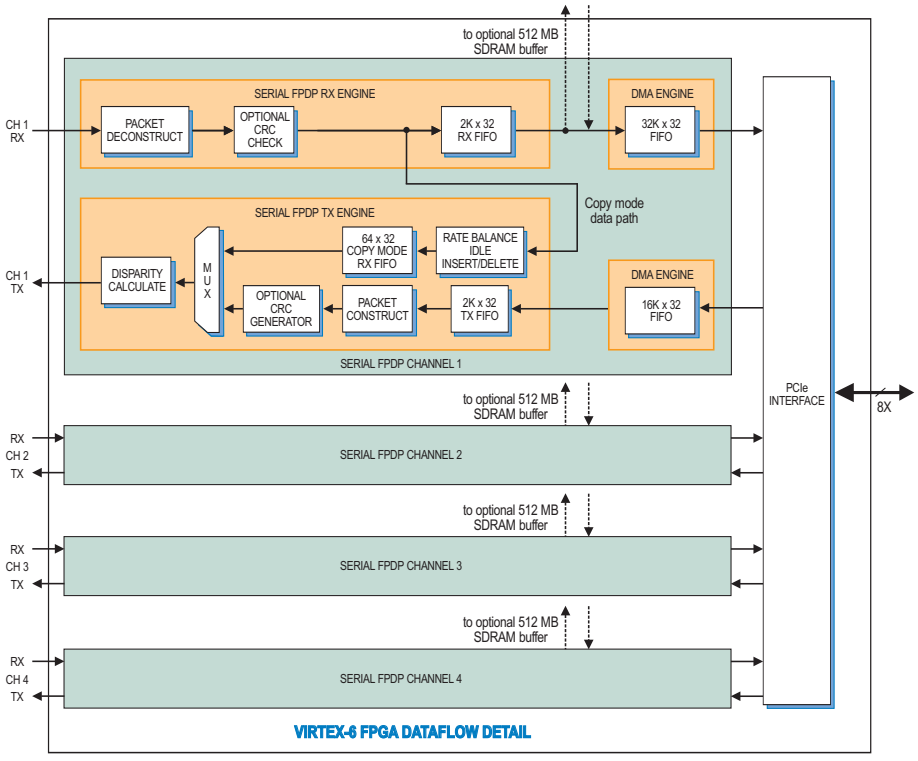
Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Std XMC module, 2.91 in. x 5.87 in.



VIRTEX-6 FPGA DATAFLOW DETAIL

Complementary Products

Model 7192: High-Speed Synchronizer and Distribution Board - PMC/XMC

ReadyFlow Board Support Package

Features

- Synchronizes up to four separate high-speed Cobalt or Onyx I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt and Onyx modules

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

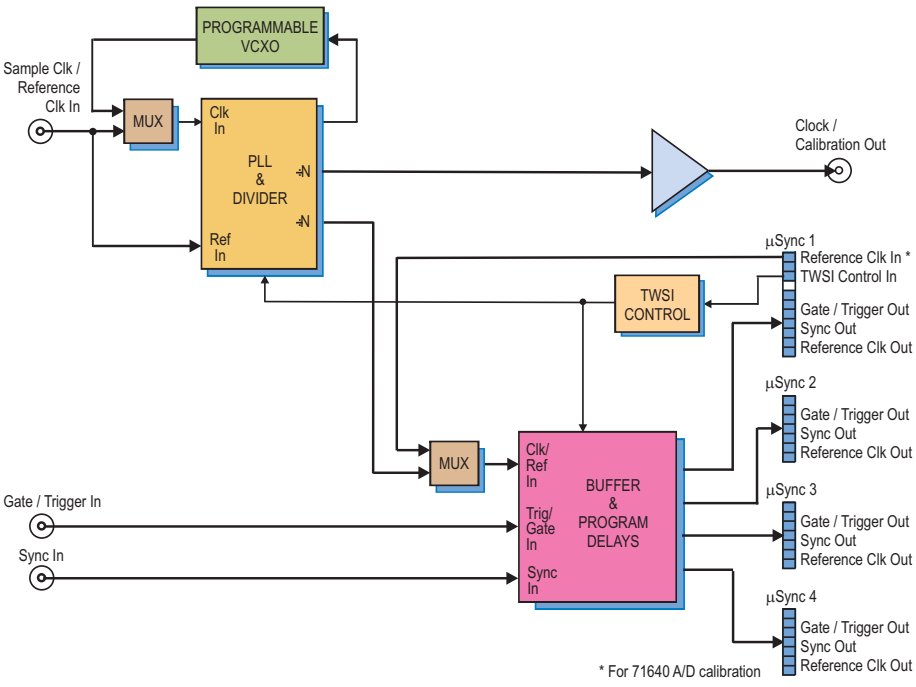
Output Signals

The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals

The 7192 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 7192 can use its on-board VCXO (programmable voltage-controlled crystal oscillator) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or onboard clock can operate at full rate or be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected modules. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.



Model 7192: High-Speed Synchronizer and Distribution Board - PMC/XMC

Also Available

Model	Format
7892	x8 PCI Express
5292	3U OpenVPX - Format 2
5692	AMC
7392	3U cPCI - Single Density
7292	6U cPCI - Single Density
7492	6U cPCI - Double Density

Gate and Synchronization Signals

The 7192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.

Calibration

The 7192 features a calibration output specifically designed to work with the Models 71640 or 71740 3.6 GHz A/D modules and provide a signal reference for phase adjustment across multiple D/As.

Programming

The 7192 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 7192 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** MMCX
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
- **Connector Type:** MMCX
- **Input Level:** LVTTL

Front Panel µSync Inputs/Outputs
- **Quantity:** 4
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2–4):** Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
- **Connector Type:** MMCX
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

PMC/XMC Interface: Power only on PMC P1 or XMC P15

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Complementary Products

Model 9192: Rackmount High-Speed System Synchronizer Unit

Features

- Synchronizes up to twelve separate high-speed Cobalt or Onyx I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Rear panel SMA connectors for input signals
- Rear panel µSync connectors compatible with a range of Pentek Cobalt and Onyx modules

The Model 9192 Rackmount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to twelve boards can be synchronized using the 9192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

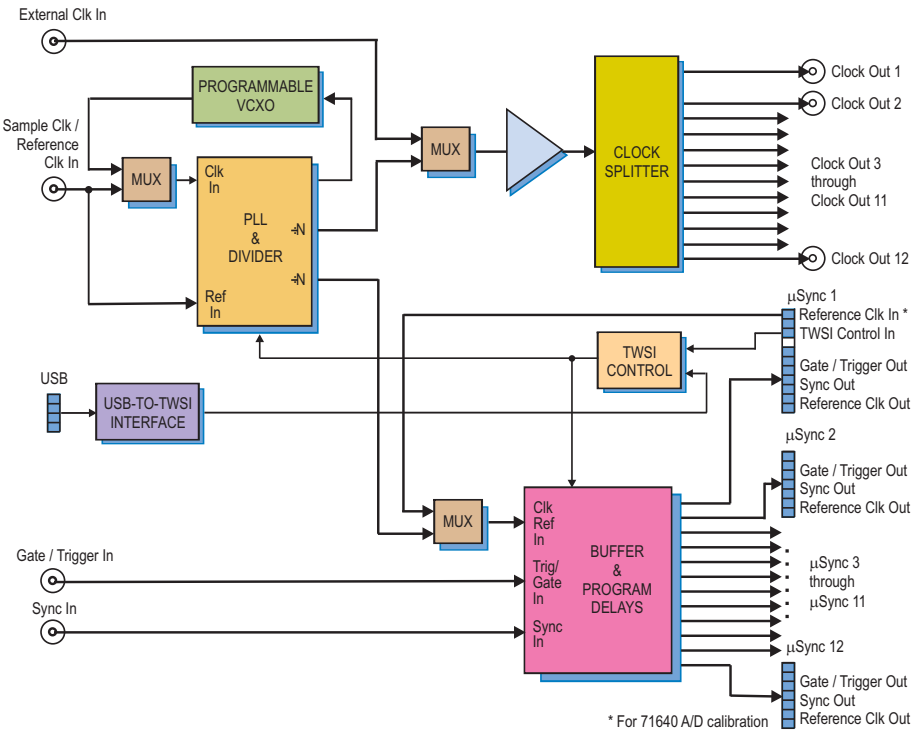
Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals

The 9192 can accept a user supplied external clock on its rear panel SMA connector. As an alternative to the external clock, the 9192 can use its onboard VCXO (programmable voltage controlled crystal oscillator) as the clock source. The VCXO can operate



Model 9192: Rackmount High-Speed System Synchronizer Unit

alone or be locked to a system reference clock signal delivered to the rear panel reference clock input.

The on-board or external clock can operate at full rate or can be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at twelve Clock Out SMAs as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 9192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.

Calibration

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D board and provide a signal reference for phase adjustment across multiple D/As.

Programming

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 is programmed via a rear panel USB connector or a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** SMA
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Rear Panel Gate/Trigger & Sync Inputs
- **Connector Type:** SMA
- **Input Level:** LVTTL

Rear Panel µSync Inputs/Outputs
- **Quantity:** 12
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2-12):** Reference Clock Out, Gate/Trigger Out, Sync Out

Rear Panel Clock / Calibration Outputs
- **Quantity:** 12
- **Connector Type:** SMA
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal at 1400 MHz, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

Power: 120VAC

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 1U Rack-mount, 19 in. x 1.75 in.

Complementary Products

Model 7893: System Synchronizer and Distribution Board - PCIe

ReadyFlow Board Support Package

Features

- Synchronizes up to eight separate Cobalt or Onyx boards
- Up to eight 7893s can be linked together to synchronize up to 64 boards
- Synchronizes sampling, data acquisition and playback for multi-channel systems
- Synchronizes gating and triggering functions
- Onboard programmable sample clock generator
- Output clock rates up to 800 MHz
- Front panel SMA connectors for TTL input signals and clock outputs
- Single-slot PCIe format

Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions.

For larger systems, up to eight 7893's can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

Input Signals

The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an onboard VCXO sample clock source.

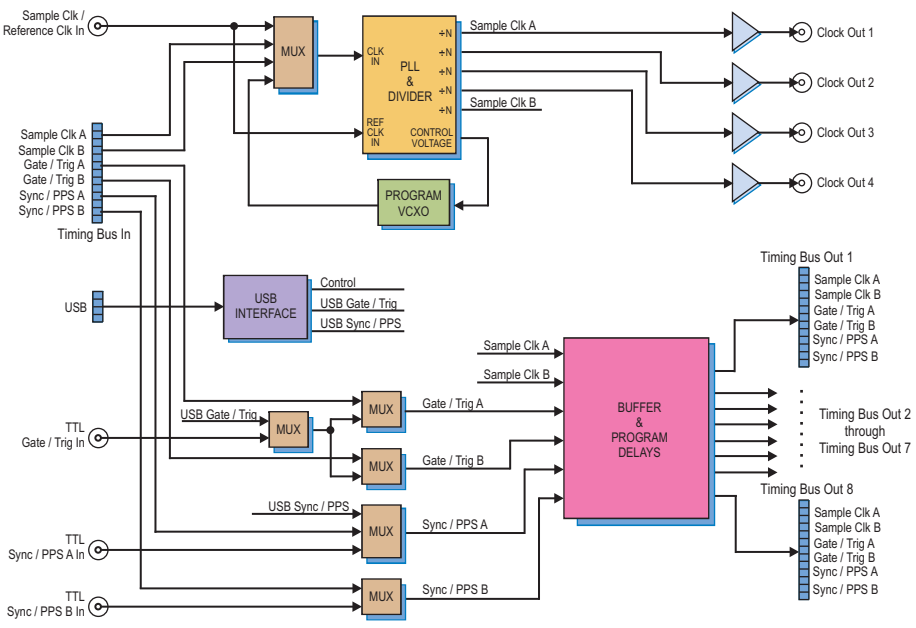
The 7893 also accepts the 26-pin Timing Bus connector used on Cobalt and Onyx boards. This input allows a single Cobalt or Onyx board to generate the timing and clock signals for the 7893 for distribution of up to eight additional boards. This input can also be used to link multiple 7893's for larger systems.

Output Signals

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

Clock Signals

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. In addition, the board is equipped with a programmable onboard VCXO clock generator which can free run or be locked to a user supplied, 10 MHz, typical, system reference. In all cases, the sample clock can be divided by 1, 2, 4, 8 or 16 prior to distribution to the Clock Out SMAs or the timing bus output connectors.



Model 7893: System Synchronizer and Distribution Board - PCIe

USB Interface

The 7893 is programmed via a USB interface. In addition to status and control, the USB interface can be used to generate Gate/Trigger and Sync/PPS signals for distribution to all connected boards.

Physical Characteristics

The 7893 is a single-slot PCIe size board which can be mounted in any PCI or PCIe slot. The board receives power from a standard six-pin PCIe power connector and uses the PCI or PCIe slot solely for physical mounting, with no electrical connections.

Supported Products

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D, 200 MHz transceivers, the 78650 and 78651 two-channel A/D, 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Cobalt 78660 and the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.

Specifications

Sample Clock/Reference Clock Input
- **Type:** Front panel female SMC connector
- **Signal:** Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or 4 to 180 MHz PLL system reference, typically 10 MHz

TTL Gate/Trigger Input
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include gate and trigger

TTL Sync/PPS Input A
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include sync and PPS

TTL Sync/PPS Input B
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include sync and PPS

Timing Bus In
- **Type:** One rear 26-pin connector
- **Signals:** LVPECL bus includes: Sample Clock A & B In, Gate/Trigger A & B In, and Sync/PPS A & B In

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 800 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference (front panel Reference Clock Input), typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for each of five on-board clock buses.

Sample Clock Output
- **Type:** Four front panel female SMC connectors, each can be independently divided
- **Output Level:** +9 dBm, nominal, sine wave

Timing Bus Out
- **Type:** Eight rear 26-pin connectors
- **Signals:** LVPECL bus includes: Sample Clock A & B Out, Gate/Trigger A & B Out, and Sync/PPS A & B Out

Control: Rear USB input for connecting to motherboard on-board USB 8-pin header

Power: Rear 8-pin connector compatible with PCIe power connectors

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Complementary Products

Model 7194: High-Speed Clock Generator- PMC/XMC

The Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Sample Clock Synthesizer

The Model 7194 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector.

The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock

In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock.

The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

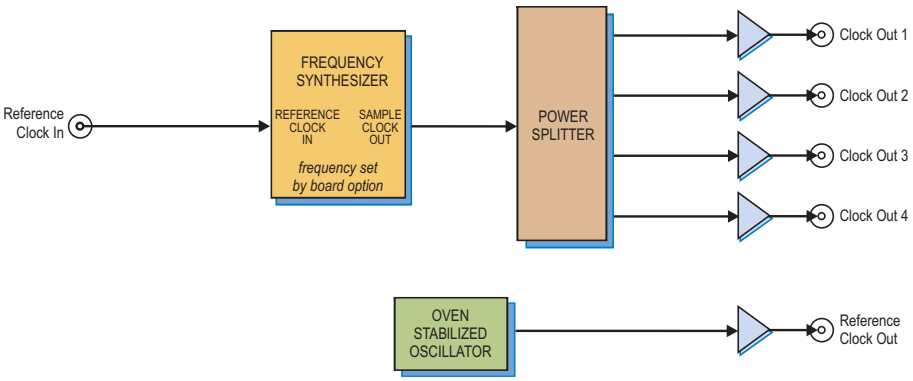
Physical Characteristics

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power.

The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Features

- Provides sample clock for up to four separate XMC Cobalt or Onyx boards
- Locks to user-supplied 10 MHz reference clock or on-board reference.
- OCXO provides an exceptionally precise clock



Contact Pentek for additional sample clock options

Model 7194: High-Speed Clock Generator- PMC/XMC

Also Available

Model	Format
7894	x8 PCI Express
5294	3U OpenVPX - Format 2
5694	AMC
7394	3U cPCI - Single Density
7294	6U cPCI - Single Density
7494	6U cPCI - Double Density

Specifications

Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option
Sample Clock Outputs
- **Type:** Four front panel female SMA connectors
- **Output Level:** +10 dBm, nominal, sine wave

Reference Clock In
- **Type:** Front panel female SMA connector
- **Frequency:** 10 MHz
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave

Reference Clock Out
- **Type:** Front panel female SMA connector
- **Center Frequency:** 10 MHz
- **Output Impedance:** 50 ohms
- **Output Level:** +10 dBm, nominal, sine wave

Frequency Stability vs. Change in Temperature: 50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
- **Daily:** ±10 ppb/day
- **First Year:** ±300 ppb

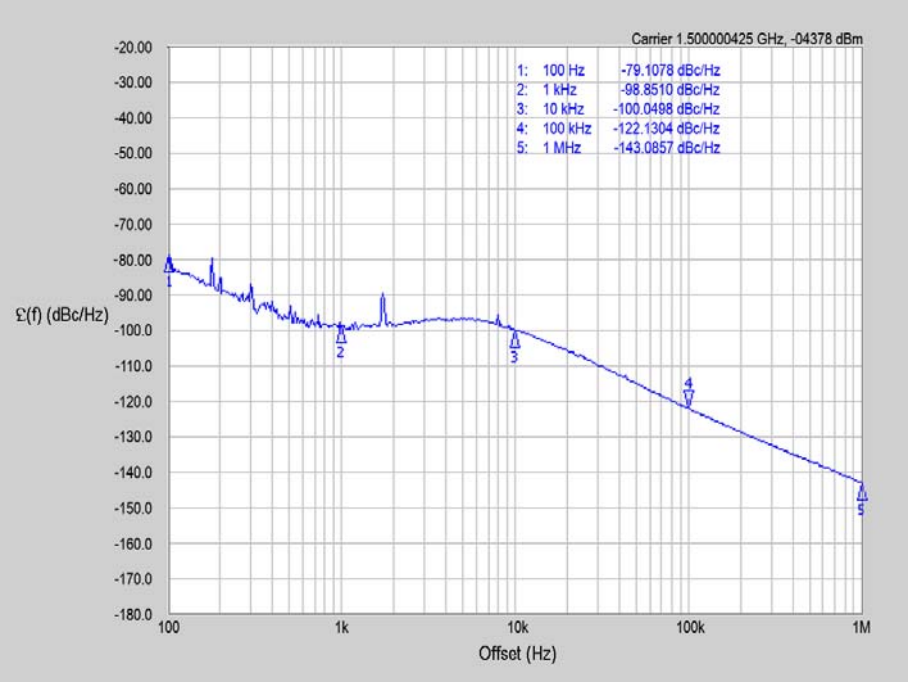
Total Frequency Tolerance (20 years): ±4.60 ppm
Phase Noise
- **1 Hz Offset:** -67 dBc/Hz
- **10 Hz Offset:** -100 dBc/Hz
- **100 Hz Offset:** -130 dBc/Hz
- **1 KHz Offset:** -148 dBc/Hz
- **10 KHz Offset:** -154 dBc/Hz
- **100 KHz Offset:** -155 dBc/Hz

PMC/XMC Interface: Power only on PMC P1 or XMC P15
Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: PMC module, 2.91 in. x 5.87 in.

Sample Clock Phase Noise

Phase Noise (1 Hz BW, typical)



Phase Noise 10.00 dB/Ref -20.00 dBc/Hz

Complementary Products

Model 8266: PC Development System for PCIe Cobalt and Onyx Boards

Features

- 4U 19-inch rackmount PC server chassis, 21-inch deep
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 8 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box test examples
- All I/O cables included

Options

Options are available for high-end multicore CPUs and extended memory support applications that require additional horsepower.

All necessary analog I/O cables are installed and tested, providing SMA connectivity for all analog I/O lines.

General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19″ 4U rackmount chassis that is 21″ deep. Enhanced forced- air ventilation assures adequate cooling for Pentek Cobalt and Onyx boards.

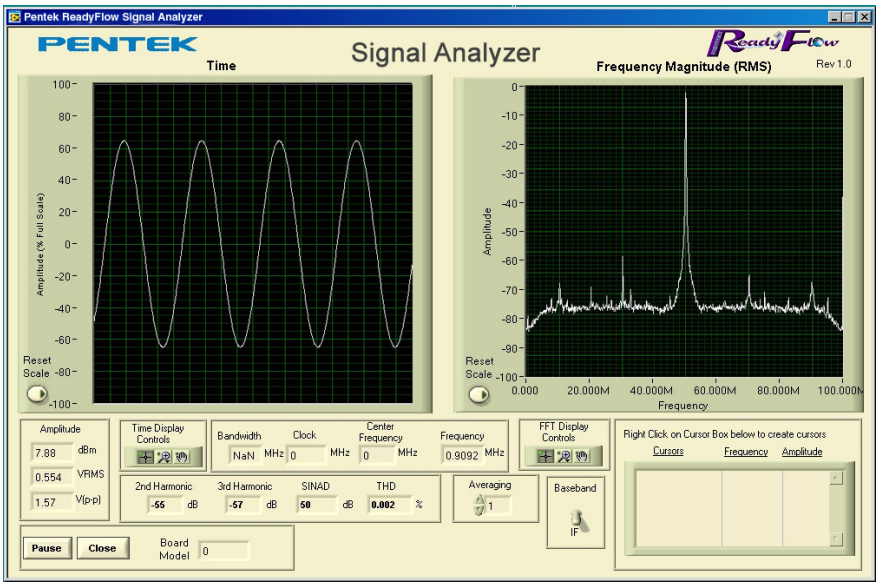
The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

The 8266 supports up to four Pentek Cobalt or Onyx boards. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd-party hardware.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 8 GB
Dimensions: 4U Chassis, 19" W x 21" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-cond.
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



** The Pentek Signal Analyzer is not supported on 64-bit Linux.*

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We're glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

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For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

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All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product's environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek's liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at:

Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900 • fax: 201-818-5697 • email: custsrvc@pentek.com

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