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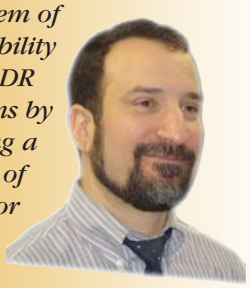
The VITA Radio Transport Protocol for SDR Architectures

In This Issue

- The VITA Radio Transport protocol was developed to provide interoperability between diverse SDR components. More in the feature article.

"The VRT standard resolves the problem of interoperability among SDR applications by providing a rich set of features for data and context packets that can be used for a wide range of applications."



Paul Mesibov, Pentek
Director of Engineering

- **Product Focus:** Model 7141-430 transceiver with 256-channel DDC. Click here
- **Product Focus:** Model 7141-420 transceiver with DDCs and interpolation filter. Click here

Technical Resources

New! Download the 1st edition of the *High-Speed Switched Serial Fabrics Handbook:*
pentek.com/go/pipeserhb

Download the 6th edition of the *Digital Receiver Handbook:*
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Download the 2nd edition of *Critical Techniques for High-Speed A/D Converters in Real-Time Systems:*
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The VITA Radio Transport (VRT) protocol is an emerging standard for Software Defined Radio (SDR) applications. It was developed to provide interoperability between diverse SDR components by defining a transport protocol to convey digitized signal data and receiver settings. The VRT provides an infrastructure to maintain accurate alignment of signal data and discrete events between multiple receivers that are either in the same location or separated by large distances.

Dramatic changes occurring in high-performance radio and signal processing architectures are the result of improved performance and smaller packages of RF and digital receiver components. The changes enable reconfigurable SDR architectures to be deployed for applications once dominated by custom architectures. The emergence of this new technology has led the industry to look for new standards to leverage this capability.

The VRT protocol addresses these requirements by defining a transport packet with unique data and context information. The signal data packets support most digitizers and signal processing formats. The context packets convey information about the internal SDR settings such as frequency, bandwidth, gain and delay and also convey spatial information. Both packet types support time stamping so that data from multiple receivers can be aligned in time to enable coherent and synchronous processing. With these features, the VRT standard makes it possible to correlate information from different SDR providers to enhance signal detection and location capabilities. It thus eliminates dependency upon a single source for receiver and DSP equipment.

VRT Protocol Benefits

The VRT standard does not define the architecture of the signal processing devices. As a result, the equipment vendor is free to define the architecture based on a variety of technologies including ASICs, FPGAs, DSPs, and general purpose PCs. The equipment can be deployed for many radio applications such as signal surveillance, radar, electronic warfare and wireless communications. The capabilities of modern receivers and signal processors make it possible to develop generic products to meet the requirements of all these applications. The commonalities of these types of SDR include:

- One or more high performance analog tuners
- Integrated digital receiver functions including digital downconversion (DDC), channelization, digital spectrum processing, and signal detection
- Dynamic routing of signals within a receiver to the digital receiver resources
- Accurate time stamping of data
- Ability to send one or more of the digital receiver channels out over an industry-standard physical link, most often serialized clock and data.

VRT Packet Features

The VRT standard resolves the problem of interoperability among SDR applications by providing a rich set of features for data and context packets that can be used for a wide range of applications. VRT provides for the interconnection of radio system components through data structures instead of hard wiring. This allows systems to be synchronized using modern gigabit distribution paths — rather than a wired connection — and facilitates applications such as synthetic aperture radar, direction finding, and beamforming.

Figure 1 on the next page shows the structure of the IF data packet. The first word is a header that's common to the IF data and the context packet. The header contains information about the packet type, option bits, a rolling counter and the packet size. This header is followed by optional words that include the stream identifier, the class identifier, time-of-day time stamp and a fractional-seconds time stamp. As an example, in the IF data packet, the header ➤

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Bit 31 • Bit 0
Header (1 Word, Mandatory)
Stream Identifier (1 Word, Optional)
Class Identifier (2 Words, Optional)
Integer-seconds Time Stamp (1 Word, Optional)
Fractional-seconds Time Stamp (2 Words, Optional)
Data Payload (Variable, Mandatory)
Trailer (1 Word, Optional)

Figure 1. The IF data packet class template.

➤ and the optional extended header are followed by the data payload and a 32-bit trailer word. In the context packet, the time stamp field is followed by a 32-bit context indicator field and the selected context fields.

The context packets provide a standardized language for relaying system attributes. The fields for these attributes have sufficient range and resolution to support future technology enhancements. Among others, some of these fields include the radio parameters such as RF and IF frequencies, bandwidth, power levels, internal delays, sampling rates, A/D overflow, temperature, and user-defined parameters. Examples of the range and accuracy of several fields are shown in Table 1. Although these fields provide a large range and fine accuracy, they do not impact link bandwidth because the context packets are sent only when a change in the context information occurs.

A standard documentation package allows for the proper interpretation of system functionality from one vendor to another. The class documentation requirement allows for standard specifications of all aspects of a system or system components so that VRT system integrators can collect specifications from VRT component vendors and understand the precise operation of the entire system.

VRT-based SDR System

Pentek and other SDR providers are beginning to introduce products based on VRT. For example, DRS offers a suite of receiver products in the HF and VHF/UHF frequency ranges that provide digitized VRT output packets as a standard feature. The products utilize a variety of high-speed interfaces such as Gigabit Ethernet, FPDP, RapidIO and others as the link layer for VRT. The products come as VME/VXS boards, or portable modules.

An example system implementation utilizes the DRS Model SI-9147 dual-channel VHF/UHF VXS tuner, connected to the Pentek Model 4207 PowerPC VXS processor board. Integrating the VRT protocol into the product, provides the key capabilities to manage the different types of signal data packets available; to identify the DSP process that created the packets in the radio; to convey the signal routing through various DSP elements; and to relay the delay of the signal route. This information is critical for any location algorithm such as direction finding and beamforming.

Without a VRT type of mechanism, each vendor must provide a custom proprietary mechanism to identify and manage the different signal streams from a receiver, making it more difficult and costly to develop applications that can operate with different receivers.

The DRS Model SI-9147 has individual synthesizers for each channel. This enables multiple channels to be coherently tuned for direction finding and beamforming applications. Dual digitizers, built into the VME/VXS board, provide 16-bit resolution at an 80 MHz sampling rate. The output of each A/D is fed into an FPGA array that routes the data to the delay memory or to one of 36 ASIC DDCs as shown in Figure 2. The DDCs are individually tunable to 32,768 different decimation settings to provide output bandwidths from 1 kHz to 17 MHz. Dozens of different signal data packet options can be selectively chosen. Loading the FPGAs with demodulation or other advanced DSP capabilities can easily lead to hundreds of output combinations from a single receiver.

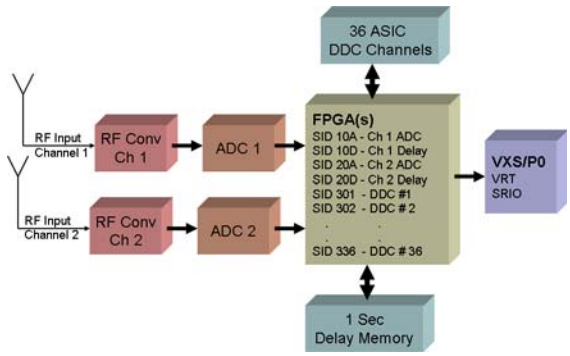

Figure 2. DRS dual-channel receiver enabled with VRT signal data packets.

Shown in Figure 3 on the next page, the Pentek Model 4207 is a single or dual Freescale MPC8641 PowerPC processor VME/VXS board. It features a host of I/O support including dual optical Fibre Channel and gigabit interfaces. It also includes two PMC module sites that are equipped to accept switched-fabric XMC modules. The board also features up to 4 GB of DDR2 SDRAM and a Xilinx Virtex-4 FPGA that supports gigabit serial fabrics and custom programming. The Pentek 4207 is optimized for embedded applications that require high-performance I/O and processing, ➤

Field Name	Min. Range	Max. Range	Resolution
Time Stamp	Present Time	136 years	1 psec or 1 sample
Frequency and BW	–8790 GHz	+8790 GHz	0.95 µHz
Gain or Power	–256 dB or dBm	+256 dB or dBm	1/128 dB or dBm
Sample Rate	0 Hz	+8790 GHz	0.95 µHz

Table 1. Sample of VRT context fields range and resolution.

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➤ such as wideband data acquisition and software radio.

The system shown in Figure 4 was developed to test and prove the feasibility of using VRT as a common transport protocol between these two boards. The system demonstrated the ability to first packetize and time stamp receiver data, then send it to the processor board over multiple lanes of the VXS backplane using serial RapidIO at 3.125 Gb/sec per lane.

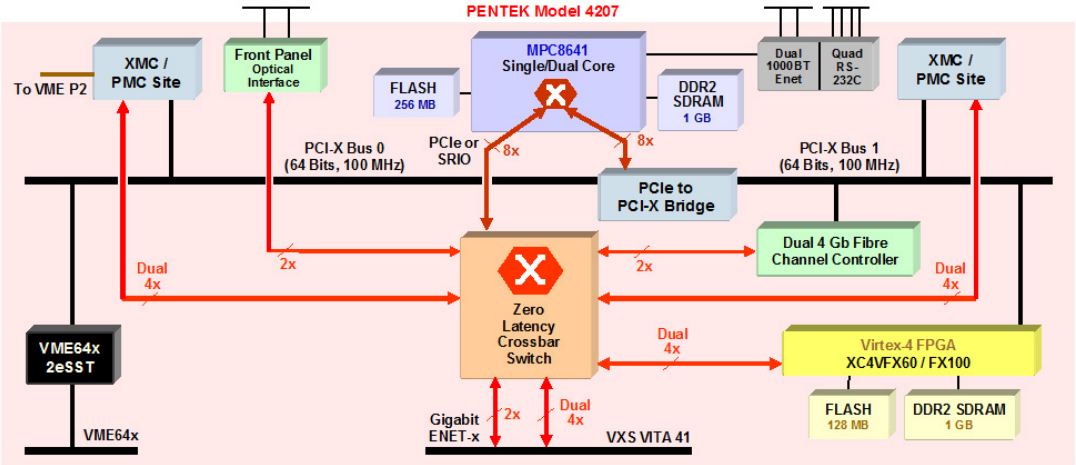


Figure 3. Pentek 4207 PowerPC I/O processor block diagram.

Multichannel VRT System

A typical architecture of a multichannel system uses four SI-9147s to provide eight RF channels that send data to four or more Pentek 4207 processor cards as shown in Figure 5. The architecture uses a Serial Rapid IO switch card to enable dynamic routing of signals from any of the receiver cards to any of the signal processing cards and/or between signal processing cards. The number of combinations of routing signals through a signal processing flow has now increased an order magnitude, from the hundreds described before for a single SI-9147 to thousands of different combinations.

This system can be used for multifunction SDR architectures that can simultaneously implement radar, communications, electronic warfare, and surveillance functions. Utilizing a high-performance fabric, the receiver and DSP resources are dynamically allocated as needed to different functions, which will change based upon the mode of operation and the priority of each function. The typical modes of operation are search, direction finding, and beamforming.

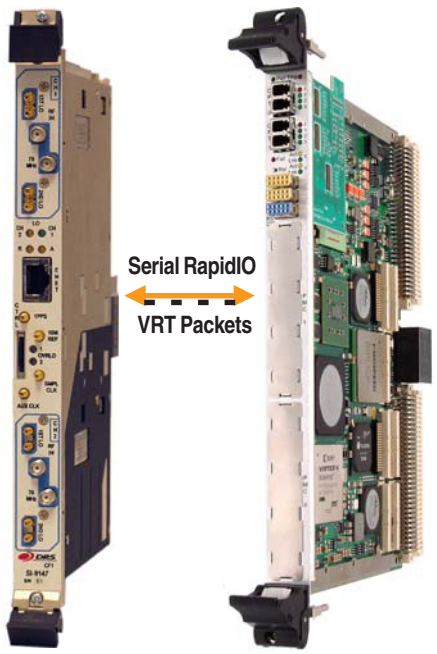


Figure 4. VRT demonstration system.

Summary

With the rise in popularity of gigabit serial networks, VRT provides the mechanism needed to manage the vast variety of signal data and context packets that can be generated by SDR architectures. General-purpose receiver and DSP cards can now be utilized in multifunction architectures with many degrees of freedom regarding the routing of signals from the receiver to the DSP application for each function. For different modes of operation within each application, the number of RF channels will dynamically change and impact the routing of signals from antenna to the DSP function. DRS and Pentek have developed COTS components that enable dynamic resource allocation based on the VRT standard. This example highlights the importance of the VRT standard to describe the signal flow of both analog and digital signals; to identify signals multiplexed onto a complex fabric; and to specify the attributes of each data-flow process, such as the receiver change in center frequency, bandwidth, power, and signal delay.

Credits

This article was excerpted from the paper *The VITA Radio Transport As a Framework for Software Definable Radio Architectures* by Robert Normoyle (DRS Signal Solutions, Gaithersburg, MD Robert.Normoyle@DRS-SS.com) and Paul Mesibov (Pentek, Inc. Upper Saddle River, NJ paul@pentek.com). This paper will be presented at the SDR Forum, October 26–30, 2008, Washington, DC. ❑

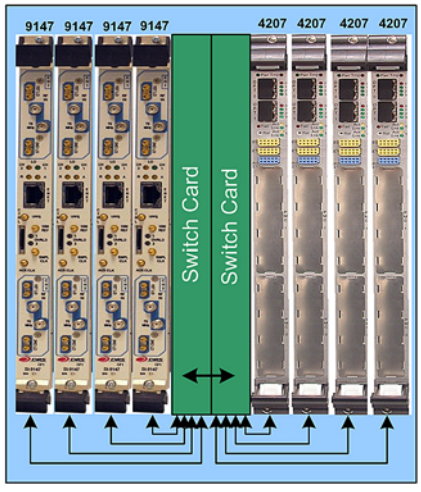


Figure 5. Multichannel system.

Product Focus

Model 7141-430

GateFlow Transceiver with 256-Channel Narrowband DDC Installed Core

General Information

Model 7141-430, Dual Digital Transceiver with 256-Channel Narrowband DDC Core 430, is a complete software radio system in a PMC/XMC module. It includes two A/D and two D/A converters for connection to HF or IF ports of a communications or radar system.

The 7141-430 receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Model 7141-430 commercial

Model 7141-430 conduction-cooled

GateFlow ReadyFlow Board Support Package

Features

- GateFlow Core 430 with 256 channels of narrowband DDCs factory-installed
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256
- Two 125 MHz A/Ds and two 500 MHz D/As included
- LVDS clock/sync bus for multimodule synchronization
- Also available in PCI and cPCI formats

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Flexible Architecture

Core 430 DDC comes factory-installed in the Model 7141-430. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

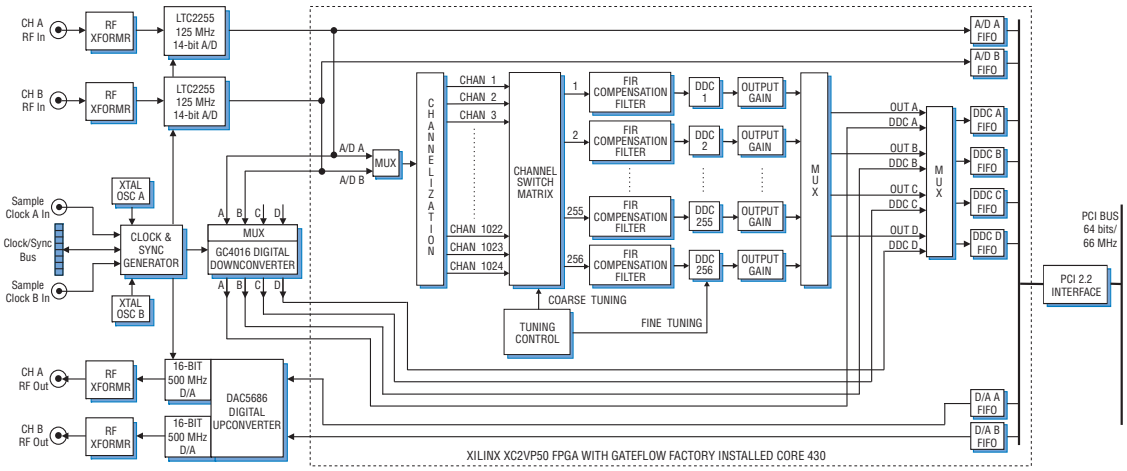
In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either timing bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As.

Performance characteristics are included at the end of this issue. For more information and price quotations on the Model 7141-430 commercial and ruggedized versions, go to: pentek.com/go/pipe7141430. ❑



Product Focus

Model 7141-420

GateFlow Transceiver with Dual Wideband DDC and Interpolation Filter Installed Cores

Model 7141-420 commercial

Model 7141-420 conduction-cooled

GateFlow ReadyFlow Board Support Package

Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576 and bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768 and bandwidth range of 40 MHz to 2.44 kHz
- Two 125 MHz A/Ds and two 500 MHz D/As included
- LVDS clock/sync bus for multimodule synchronization
- Also available in PCI and cPCI formats

General Information

Model 7141-420, Dual Digital Transceiver with Wideband DDC and Interpolation Filter cores, is a complete software radio system in PMC/XMC format. It includes two A/D and two D/A converters for connecting to HF or IF ports of a communications or radar system.

The 7141-420 receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, the module includes Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

Two identical Core 420 DDCs are factory installed in the 7141-420 FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

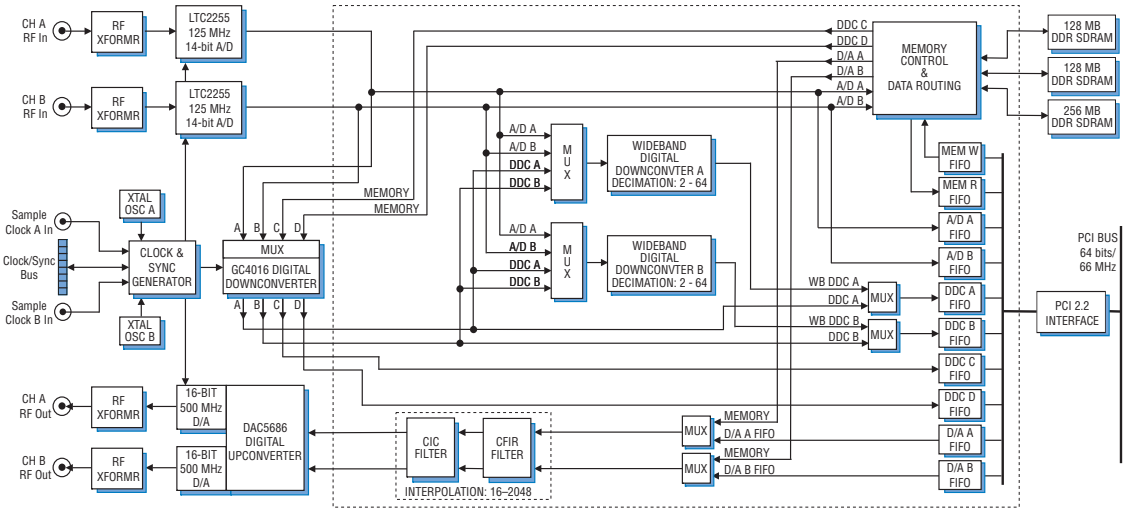
A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

All the standard features are retained including D/A waveform generation, data routing and formatting, and transient capture.

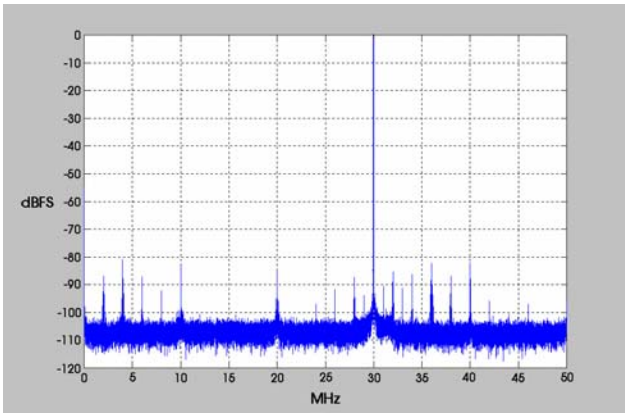
Performance characteristics are included at the end of this issue. For more information and price quotations on the Model 7141-420 commercial and ruggedized versions, go to: pentek.com/go/pipe7141420. ❑



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420

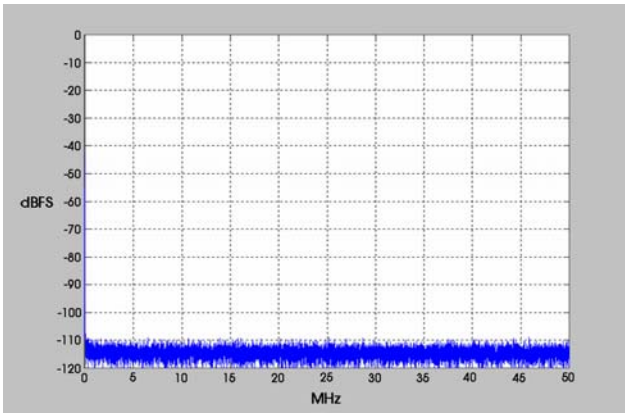
Models 7141-420 and 7141-430
A/D Converter Performance

Spurious Free Dynamic Range



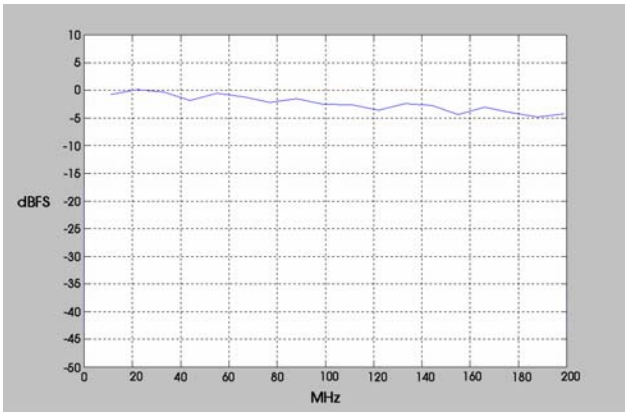
f_{in} = 70 MHz, f_s = 100 MHz

Spurious Pick-up



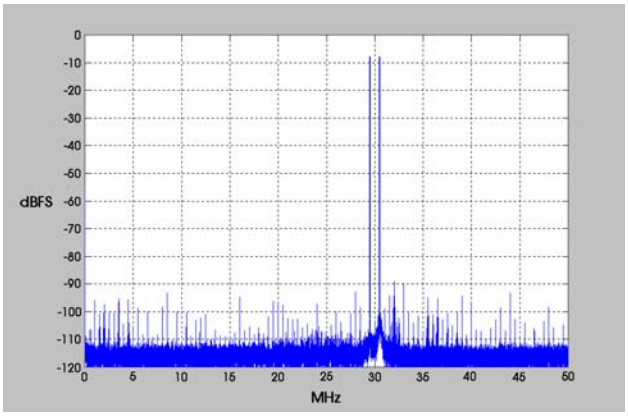
f_s = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



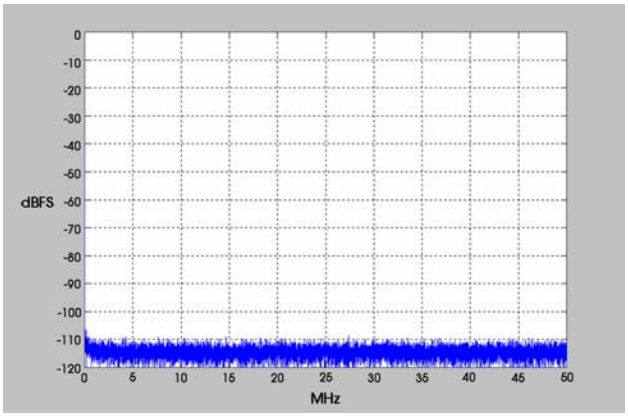
f_s = 100 MHz

Two-Tone SFDR



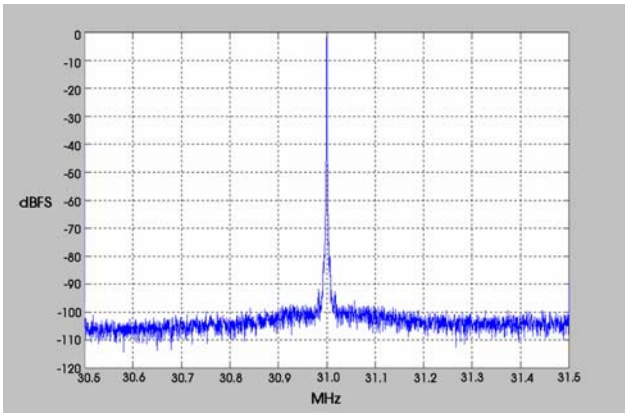
f_1 = 29.5 MHz, f_2 = 30.5 MHz, f_s = 100 MHz

Crosstalk



$f_{in\ Ch2}$ = 69 MHz, f_s = 100 MHz, Ch 1 shown

Phase Noise



f_{in} = 69 MHz, f_s = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz