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The Unmanned Aerial Vehicle Synthetic Aperture Radar System

NASA's Jet Propulsion Laboratory has built a reconfigurable L-band synthetic aperture radar (SAR), specifically designed to acquire airborne repeat-track SAR data for differential interferometric measurements. Differential interferometry can provide key deformation measurements, important for studies of earthquakes, volcanic eruptions and other dynamically changing geophysical phenomena.

Project Objectives

Earth science research often requires crustal deformation measurements at a variety of time scales from seconds to decades. To this end, the NASA Solid Earth Science Working Group has recommended an observational program that includes both airborne and spaceborne capabilities. Since many geophysical processes, such as volcanic eruptions and earthquakes, occur quickly and require immediate response, the program goal is to provide Earth deformation measurements on an hourly basis with global access. While this objective is best supported by a geosynchronous constellation of repeat-pass interferometric SAR satellites, the recommended first step is a low-orbit deformation satellite with a repeat period of about one week. An airborne radar program is also part of this plan to deliver short-time baseline observations and repeat-pass measurements at time scales much smaller than one week and as short as twenty minutes.

Repeat-track interferometry is much more difficult to implement from an airborne platform. The main technical reasons are:

- It is difficult to fly the same pass twice because of wind gusts and turbulence.
- It is difficult to maintain the same antenna pointing on repeated passes due to the varying crosswinds.

System Design

The UAVSAR radar is designed to be flown onboard a UAV (Unpiloted Aerial Vehicle) but it will be initially deployed on the NASA Gulfstream III aircraft. Figure 1 shows the UAVSAR instrument pod attached to the underside of the NASA aircraft during early flight testing. Key measurements the system is designed to make include:

Figure 1. The UAVSAR pod is attached to the underside of the aircraft. (Photo courtesy of DFRC)

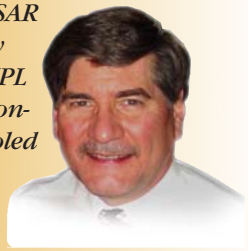
- Precision crustal deformation for measuring earthquakes both during and after a seismic event, monitoring volcanic activity and surface changes induced by human activity
- Polarimetric interferometry that can provide measurements of forest structure and topography; polarimetric radars transmit pulses with both vertical and horizontal polarization
- Polarimetric interferometry to map the vertical structure of an area with vegetation

To obtain valid data on successive passes over a specific area, the aircraft must fly in a trajectory that is within a cylindrical space of 10 meters in diameter. Furthermore, the radar antenna must be steered with 1 degree accuracy over a range of ±20 degrees in azimuth. To meet these requirements, the Gulfstream was modified by NASA's Dryden Flight Research Center (DFRC) to include a Precision Autopilot that controls the aircraft trajectory using the input from a precision real-time differential GPS (Ground Positioning System) designed and assembled by JPL with COTS components. The system also employs an electronically steered flush-mounted antenna ➤

In This Issue

- JPL has built a synthetic aperture radar system that's designed to acquire data for airborne interferometric measurements. More in the feature article.

"Pentek is proud to participate in the development of the UAVSAR system by supplying JPL with our conduction-cooled Model 6821 215 MHz, 12-bit A/D converter along with our ReadyFlow and GateFlow software packages."



Rodger Hosking, Pentek Vice President and Cofounder

- **Product Focus:** Model 7150 PMC/XMC Quad 200 MHz 16-bit A/D. Click here
- **Product Focus:** Model 7151 256-Channel Downconverter. Click here

Technical Resources

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➤ that's pointed in the desired direction based on real-time attitude angle measurements. The key parameters of the radar design are given in Table 1.

Parameter	Value
Frequency	1.26 GHz
Bandwidth	80 MHz
Pulse Duration	5–50 µs
Polarization	Quad
Range Swath	16 km
Look Angle Range	25°–65°
Transmit Power	3.1 kW
Antenna Size	0.5 m × 1.6 m
Operating Altitude	2,000–18,000 m
Ground Speed	100–250 m/s

Table 1. Radar Parameters

Figure 2 is a simplified block diagram of the UAVSAR radar. The radar has been designed to minimize the number of interfaces with the aircraft for improved portability. The aircraft supplies the pod with 28 V DC power and receives position information from the pod's differential GPS unit. The desired flight paths are generated by the Ground Data System and loaded into the Precision Autopilot and the Automatic Radar Controller (ARC). The ARC is the main control computer and is designed to operate in a fully autonomous mode or to accept commands from the Radar Operator Workstation (ROW). The Control and Timing Unit (CTU) controls the timing of all the transmit and receive events and thus interacts with many radar digital and radio-frequency electronics. The active array antenna consists of 24 L-band transmit/receive modules that feed 48 radiating elements within the 0.5 m by 1.5 m array. The photograph of Figure 3 on the next page, shows how the various subsystems are arranged within the pod.

Digital Electronics Subsystem

The Digital Electronics Subsystem (DES) provides the overall timing and control signals for the radar as well as the telemetry and data acquisition functions. All the digital units are housed in a custom VME card cage. Coordination and control is through the ARC, the master computer. The ARC flight software controls the system in both attended and unattended flight operations. The ARC software utilizes the Wind River VxWorks real-time operating system.

Precision timing of the radar pulse generation, ADC operation, and antenna commands are essential for proper radar operation. The CTU unit was designed by JPL using a Xilinx FPGA. It generates all the radar timing signals for the Arbitrary Waveform Generator (AWG), antenna, radar receivers and the data acquisition.

After each transmitted pulse, the radar opens a receive window and digitizes the return signal. The radar employs an offset sampling scheme whereby it records real rather than complex data. To meet the Nyquist sampling rate, it samples the return data at 180 MHz which is more than twice the radar bandwidth of 80 MHz. With pulse repetition rates up to 1 kHz per data channel and receive window durations of up to 150 msec, the radar generates a large amount of data. The ADC board is the Pentek Model 6821, 215 MHz, 12-bit VME board. JPL uses the conduction-cooled version of this board to handle the extreme environments encountered in the UAVSAR pod. Onboard data rate reduction uses an optional block-floating point quantization algorithm implemented in one of the Model 6821 FPGAs. The algorithm allows the user to select how many bits are retained from each data sample, anywhere from 12 to 2 bits. By supplying a user-defined exponent for each 128-sample block, the dynamic range is maintained.

Once the returned data is digitized, it's buffered and written to disk along with an ancillary header and time tag. Data storage is provided by a COTS JBOD array with 1.8 TB capacity.

RF Subsystem

The RF subsystem consists of a frequency synthesizer that provides a 10 MHz ➤

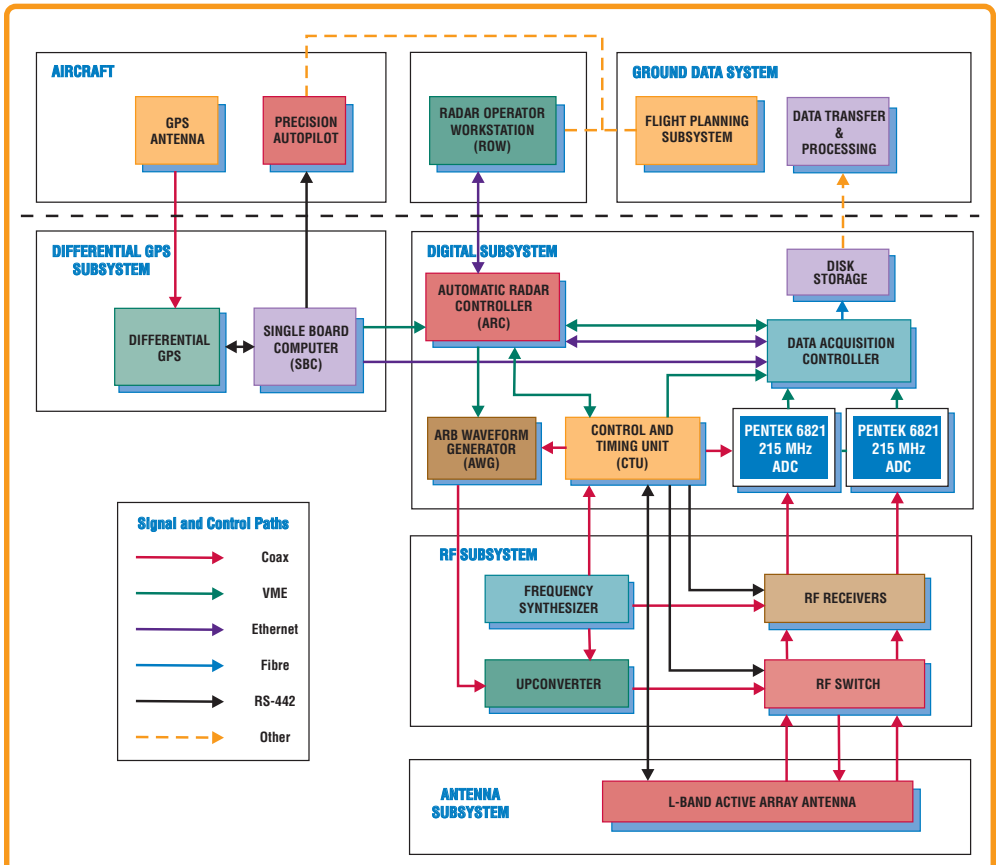


Figure 2. Simplified Block Diagram of the UAVSAR including the aircraft, GPS, and ground system interfaces.

The Unmanned Aerial Vehicle Synthetic Aperture Radar System

➤ reference signal for frequency generation, supplies a local oscillator for the upconverter and the receivers, and a timing signal for the AWG. Upconversion of the AWG center frequency of 137.5 MHz to the desired radar transmit center frequency of 1,257.5 MHz and routing of the signal to the antenna or receivers is done by the upconverter unit. Dual L-band receivers take the return signals from the transmit vertical and horizontal polarization signals, translate them down to center frequencies of 45 MHz and inject them into the two Model 6821 ADCs for digitizing.

Navigation Subsystem

While standard GPS position accuracy is 5–10 meters, the UAVSAR differential GPS uses correction information and real-time software to achieve accuracy better than one meter. This subsystem is a blend of COTS components coupled with the specialized software hosted on a single board computer.

Differential Interferometry

Repeat-pass airborne radar interferometry requires sophisticated signal processing algorithms to generate the desired deformation and associated scientific data. The UAVSAR Ground Data System consists of the hardware and software necessary to process and archive raw data and the derived scientific data.

A detailed discussion of the processing methodology is beyond the scope of this article. Suffice it to say that the airborne flight tracks are not known sufficiently well in advance. It is thus necessary to use the collected data themselves to refine the time-varying baseline between flight tracks, reprocess the data with updated flight track information, then proceed with interferometric processing. Figure 4 shows a UAVSAR image of Mount St. Helens, perhaps most famous for its catastrophic volcanic eruption on May 18, 1980.

Figure 3. Photograph of the UAVSAR with the cover removed shows how the electrical subsystems are arranged within the pod. (Photo courtesy of JPL)

A Look into the Future

Ultimately, the goal of the UAVSAR system is not simply to make surface deformation measurements, but to use these measurements to achieve a better understanding of the underlying physics of solid earth processes. Geophysical algorithms that take the deformation maps and invert them for quantities of interest, e.g. fault depth and orientation of seismic sources are being developed by Stanford University as an integral component of the ground data system. Future application of UAVSAR might include support in response to natural hazards, such as an earthquake, as these algorithms and the system mature. ❑

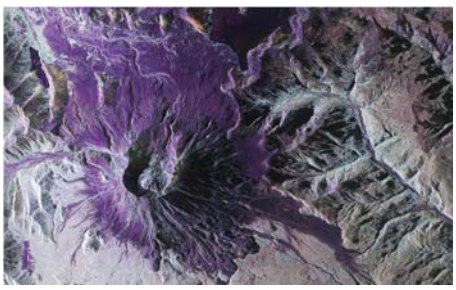
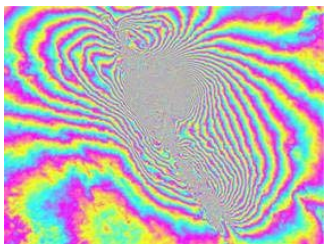
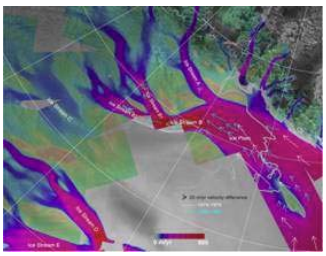


Figure 4. This false color, composite image of Mount St. Helens was constructed by assigning colors (red, blue and green) to three of the polarimetric layers collected by the UAVSAR from an altitude of 41,000 feet. Although covered by snow at the time, many features within the lava dome of Mount St. Helens are visible as the radar partially penetrates the snow layer. (Photo courtesy of JPL)



Interferogram showing surface deformation of the 1999 Hector mine earthquake. (Photo courtesy of JPL)



Interferogram showing rapid evolution of ice. (Photo courtesy of JPL)

Close-up photograph of the UAVSAR Pod attached to the underside of the aircraft. (Photo courtesy of DFRC)

Another close-up photograph of the UAVSAR Pod with the electronics cover removed. (Photo courtesy of DFRC)

Product Focus

Model 7150

Quad 200 MHz, 16-bit A/D PMC/XMC Module with two Virtex-5 FPGAs

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O on P4

General Information

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems.

Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched-fabric interfaces.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +10 dBm into 50 ohms with transformer coupling into four 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

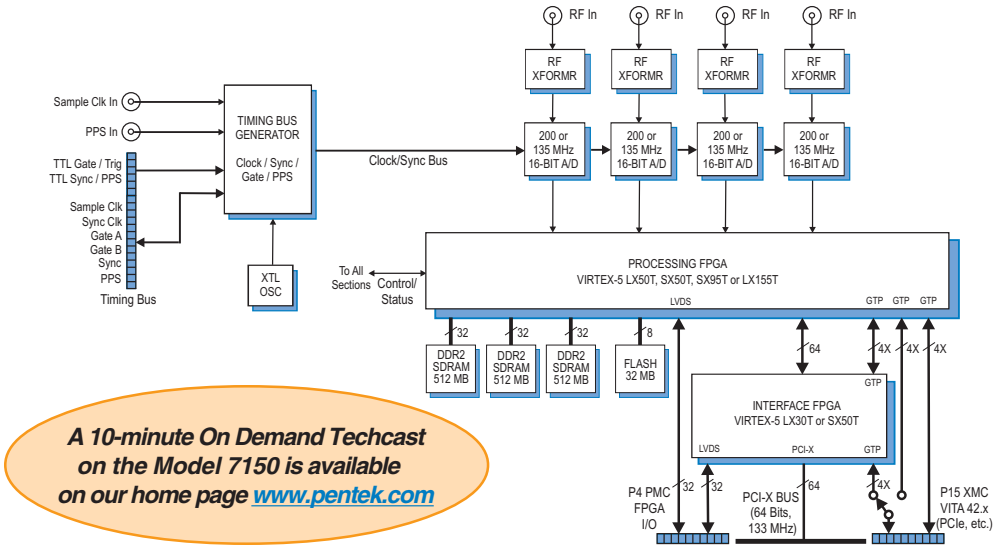
The Model 7150 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory- shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T and LX110T among others.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX110T in the processing FPGA position for 110,592 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as a VLXT family or an LXT family part, providing not only interface functionality, but additional processing resources up to an additional 640 DSP48E Slices.

Optionally, the P4 PMC connector may be fitted with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.



A 10-minute On Demand Techcast on the Model 7150 is available on our home page www.pentek.com

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Forore information and a price quotation go to: pentek.com/go/pipe7150. ❑

Product Focus

Model 7151

256-Channel Digital Downconverter with Quad 200 MHz, 16-bit A/D PMC Module

ReadyFlow Board Support Package

Features

- 256 channels of DDC
- Four 200 MHz 16-bit A/Ds
- DDC decimation from 128 to 1024 in steps of 64
- Common decimation factor within each DDC bank
- Different decimation factors between banks
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVDS clock/sync bus for multi-module synchronization

General Information

Model 7151 is a 4-channel, high-speed digitizer designed for processing baseband RF signals or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 256-channel installed DDC (digital downconverter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

Model 7151 uses the industry standard PMC daughtercard format compatible with numerous carrier boards for VME, PCI, and CompactPCI.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +10 dBm into 50 ohms with transformer coupling to four 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

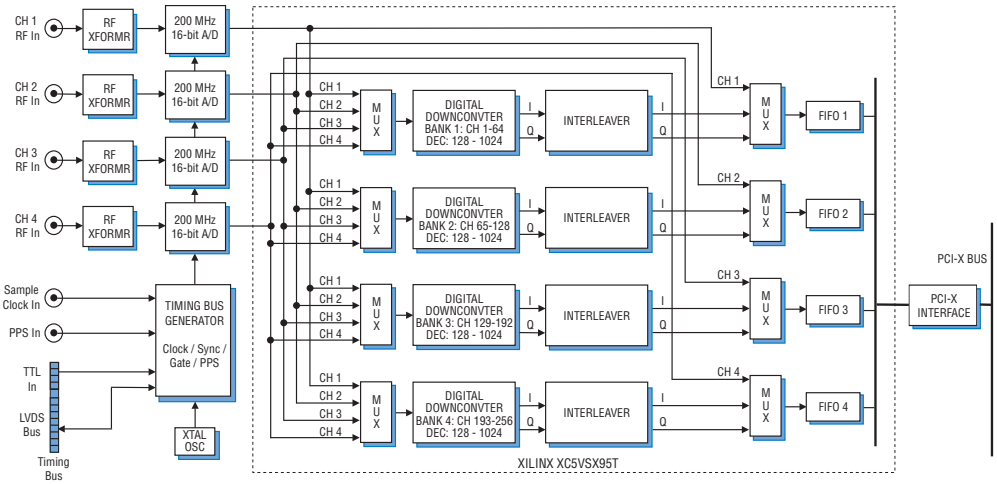
Each of the 256 DDCs has an independent 31-bit tuning frequency setting that ranges from DC to $f_s/2$, where f_s is the A/D sample rate.

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 190 MHz, the available output bandwidths range from 148.4 kHz to 1.2 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.



Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Forore information and a price quotation go to: pentek.com/go/pipe7151. ❑