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The Pentek Pipeline
A quarterly publication for engineering system design and applications.

In This Issue

Dane du Plessis is a Ph.D. student at the University of Cape Town. He is interested in multistatic ISAR imaging and has an undergraduate background in physics and electrical engineering. Currently, he works on system integration of NeXtRAD with several other team members.

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A Pentek Transceiver Provides the SDR Interface for the NeXtRAD Multistatic Radar System

by Dane Du Plessis

NeXtRAD is a dual-band, dual-polarization, multistatic radar system under development at the University of Cape Town (UCT) in collaboration with University College London (UCL). The primary mission of the system is to collect multistatic data of small radar cross-section maritime targets embedded in sea clutter.

NeXtRAD is a multi-sensor network comprised of three stations (or nodes) separated by several hundred meters, all focussing on a common target area as shown in Figure 1. Only node 0 generates and receives radar signals, while nodes 1 and 2 are receive only. The system requires a usable bandwidth of 50 MHz to achieve a range ➢

Figure 1. Typical Deployment Configuration of NeXtRAD

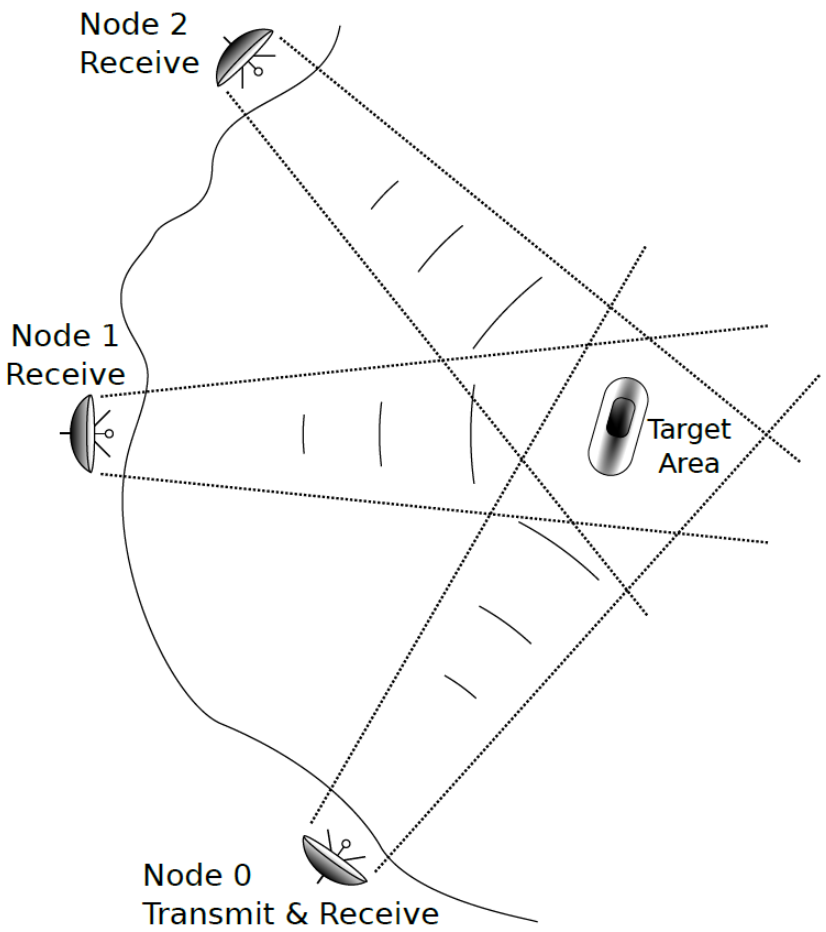
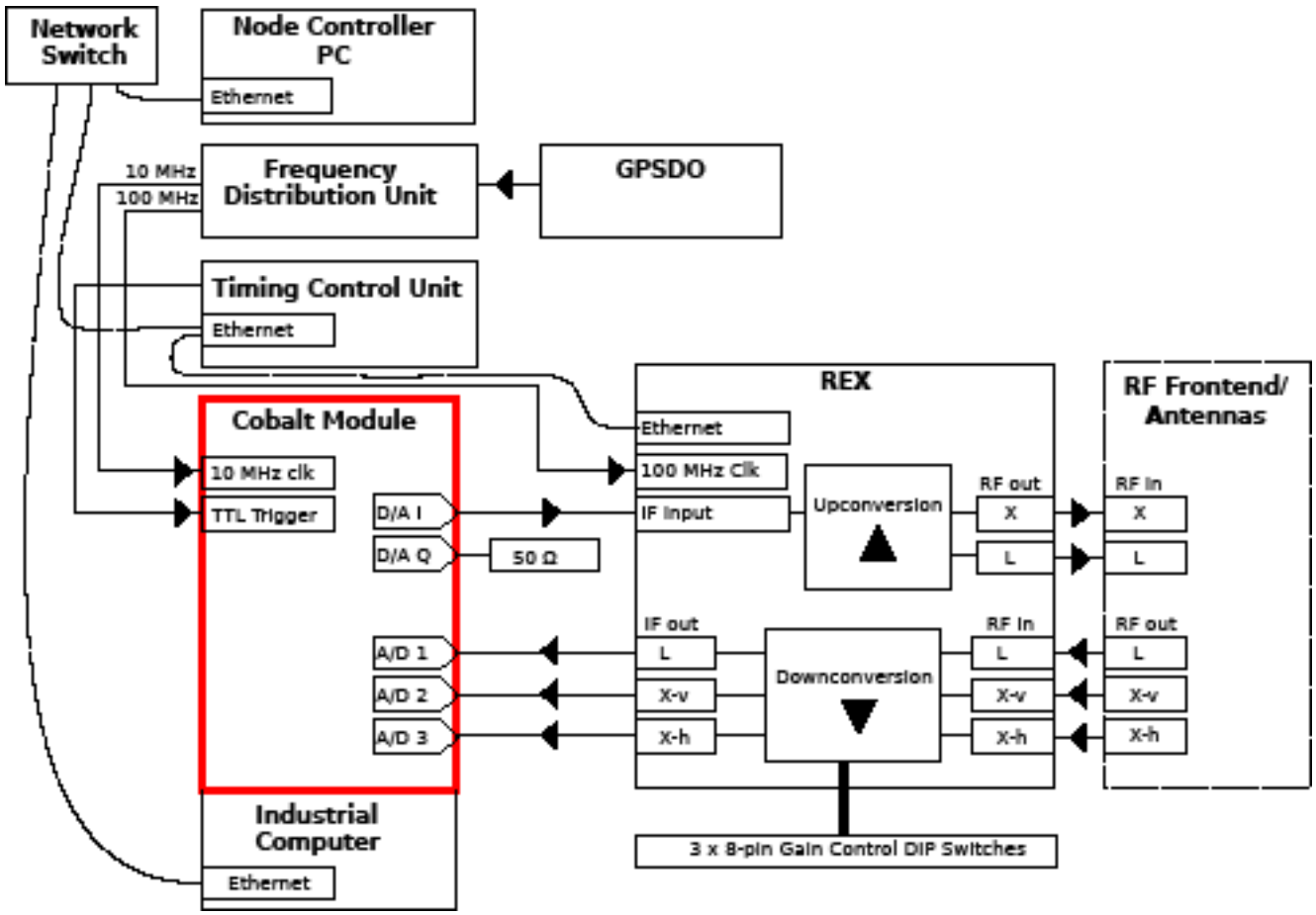


Figure 2. A System Block Diagram of the Transmitting Node of NeXtRAD



resolution of three meters. Each node has dual-polarized L- and X-band antennas (IEEE definition) with a 10-degree beamwidth.

This arrangement effectively forms a pair of bistatic radars in combination with a monostatic radar, which means that target data can be simultaneously acquired from three perspectives. This topology has advantages over single-sensor radars. NeXtRAD is a more capable version of NetRAD, a single-frequency multistatic radar developed by UCT and UCL.

During the early stages of the NeXtRAD project, Pentek's Cobalt® Model 71621 transceiver system was identified as a suitable software-defined radio interface for the system. This article presents the early stages of the development of NeXtRAD, which uses Pentek's Model 71621 module as the digital transceiver of the system in a monostatic configuration.

NeXtRAD System Overview

The active node of the NeXtrad multistatic system consists of the following (see Figure 2):

- Software-defined radio (SDR) interface
- Radio frequency (RF) receiver and transmitter
- FPGA-based timing control unit (TCU)
- High-power amplifier

Pentek's Cobalt Model 71621 (Figure 3) was selected as the SDR interface because it is well-suited to the radar's requirements, providing three A/D converters and a dual-channel 800 MHz D/A converter.

NeXtRAD is a pulse-Doppler radar, which requires that waveform generation and digitization be fully coherent at each node. To achieve coherency, each node is supplied a very stable 10 MHz reference signal from a local GPS-disciplined oscillator (GPSDO), which is distributed via a frequency distribution unit (FDU) to the Cobalt module and to the receiver exciter (REX). This ensures that there is no phase drift between oscillators in a given node, and that the relative phase of oscillators between any two nodes is constant. ➢

The Cobalt module can be configured to accept the 10 MHz signal from its front panel SSMC clock input. The GPSDO also supplies a trigger pulse which precisely synchronises the start of a radar measurement. After an initial trigger event from the GPSDO, the TCU takes over and delivers the trigger pulse to the Cobalt module at the pulse repetition frequency (PRF).

Signal Planning

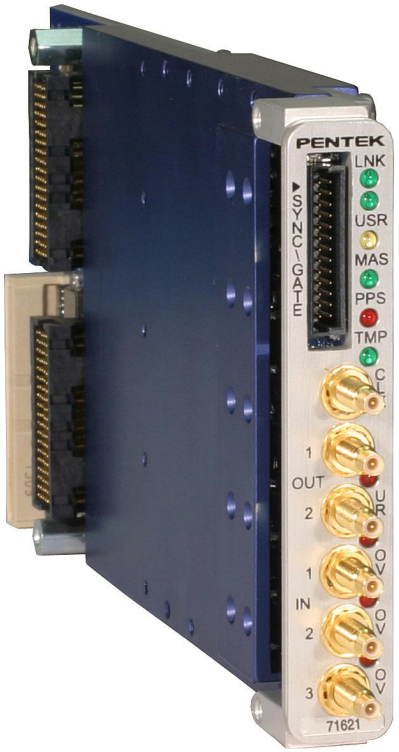
The transmitted pulse is generated by the Cobalt module in the active node of the sensor network. The system employs linear frequency-modulated pulses with 50 MHz bandwidth and duration of 1 to 10 micro seconds, at a PRF from 1 to 2 kHz. The Cobalt module is able to supply the 50 MHz bandwidth signal on a 125 MHz intermediate frequency (IF) at a 720 MHz output frequency from one of its two available 16-bit D/A output channels. The REX upconverts the IF waveform to either L- or X-band. After amplification, the waveform is transmitted via the appropriate antenna to illuminate the target area with either vertical or horizontal polarization.

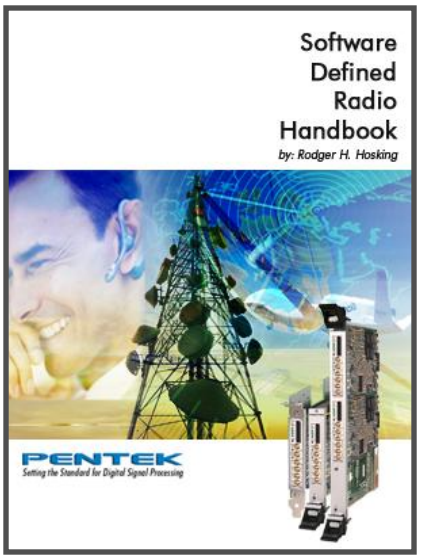
Transmitted energy is scattered in many directions by the target scene. Antennas at each node location intercept only a tiny fraction of that energy. The L-band signal is captured in either vertical or horizontal polarization, and two X-band channels simultaneously record both polarizations. Receivers in each node amplify and downconvert the received signals to the 125 MHz IF analog signal. A dedicated A/D channel on the Cobalt module records the single L- and two X-band waveforms.

The signal planning for the transmit and receive chains is similar to that described in a tracking radar application in Pentek Pipeline Vol. 19, No. 2, "Radar Topics, Applications, and Pentek Products". In NeXtRAD, the waveform engine on the Cobalt module stores a variety of waveforms in the onboard DDR3 RAM. Waveform generation is triggered by an LVTTL rising edge delivered to the trigger input on the Cobalt module's front panel. The data input rate to the Texas Instruments DAC5688 D/A module is 180 MSPS. The digital upconverter (DUC) in the D/A translates the spectrum from 0 Hz to the IF. With an interpolation factor of 4, the output sample rate of the DAC is increased to 720 MSPS. The intermediate frequency signal is then upconverted to RF by the REX for amplification.

On the receive chain, the RF signal received at the antennas is downconverted to the IF for digitization by the A/D modules on the Cobalt module. The same ➢

Figure 3. Cobalt Model 71621:
3-Ch 200 MHz A/D with DDC & 2-Ch 800 MHz D/A with DUC, Virtex-6 FPGA



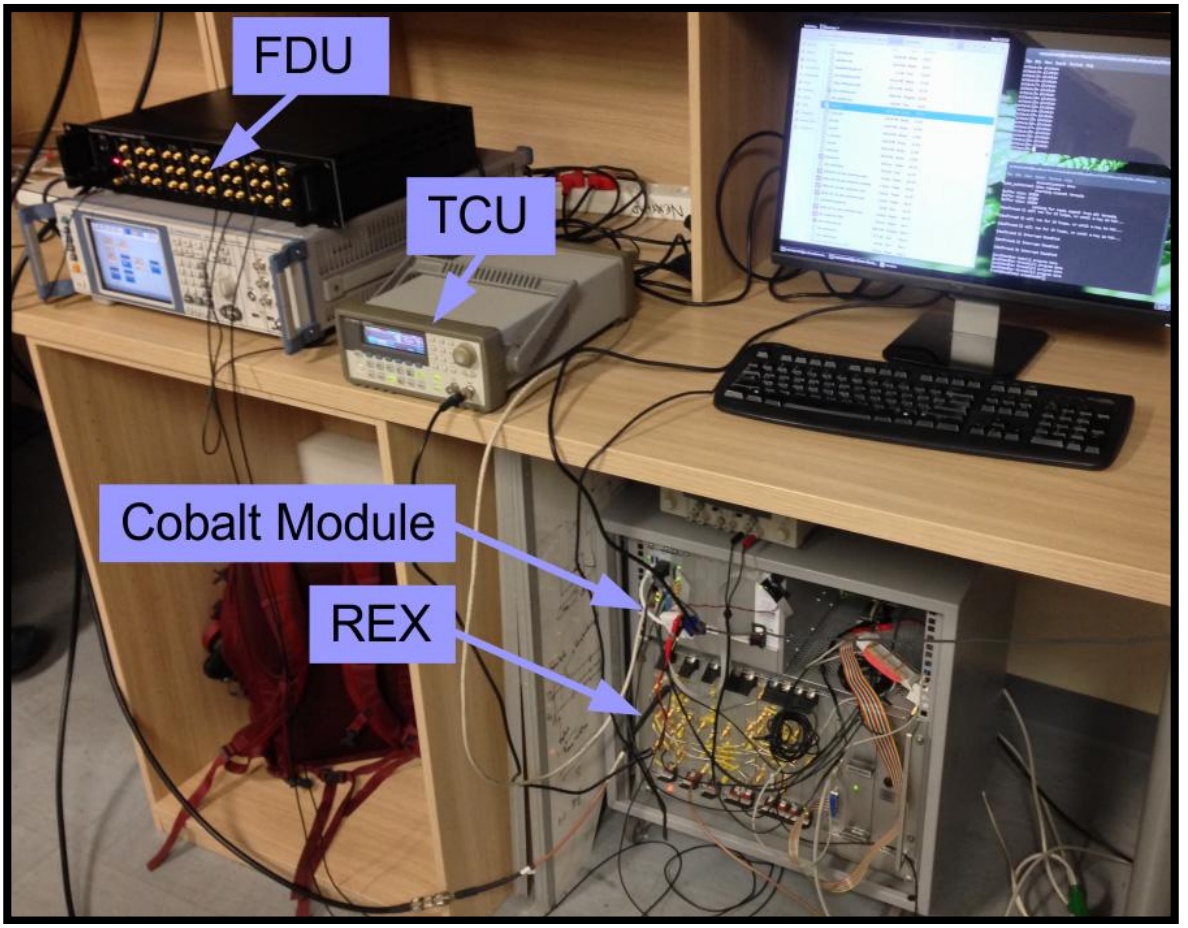


Software Defined Radio Handbook

SDR (Software-Defined Radio) has revolutionized electronic systems for a variety of applications including communications, data acquisition and signal processing. This handbook shows how DDCs (Digital Downconverters) and DUCs (Digital Upconverters), the fundamental building blocks of SDR, can replace legacy analog receiver and transmitter designs while offering significant benefits in performance, density and cost.

To download this FREE resource, click **here!**

Figure 4. The hardware testing setup for the low-power prototype. Labeled are the frequency distribution unit (FDU), the timing control unit (TCU), the Cobalt module, and the receiver exciter (REX).



trigger signal is used to initiate digitization at each pulse. The ADC is tuned to sample at Fs = 180 MHz. This places the incoming signal in the second Nyquist zone and results in the spectrum being translated to the first Nyquist zone from 0 to Fs/2, i.e., from 30 to 80 MHz.

Tuning the digital downconverter IP core on the Cobalt module to 55 MHz and setting the decimation factor to 2 translates the incoming signal to DC and produces IQ samples at Fs/2 = 90 MHz. A helpful explanation of undersampling is given in "Putting Undersampling to Work," which you can download here. The downconverted, 16-bit complex samples are then transferred via the PCIe 8x interface to the host computer's memory for post-processing.

An important consideration for the coherency of the radar is that the numerically controlled oscillators in the digital upconverter of the D/A and the digital downcovnerter IP core on the FPGA need to be reset to a known value on each rising edge of the external trigger. If this is not done, an unpredictable phase term is introduced to the IF signal from the D/A, and also to the discrete baseband signal generated by the digital downconverter (DDC).

The phase of the digital sine and cosine terms generated in the DUC and DDC can be reset to zero on rising edges of the external trigger with proper configuration of the control registers for the DAC5688 and the DDC IP core. This ensures that phase offsets introduced to the radar signal on generation or digitization can be ignored in post-processing as they do not vary between pulse repetition intervals.

Initial Testing and Results

The controller software for the Cobalt module was developed using Pentek's ReadyFlow® software libraries, in conjunction with an arbitrary waveform generator, spectrum analyzer, and an oscilloscope. The digitization and waveform generation chains were developed and tested in separate controller programs before fusing these programs into a working source. A simple IF loop-back test using one of the D/A output channels and a signal splitter was sufficient do most of the development required for the digital transceiver before introducing the REX and other subsystems.

The hardware configuration shown in Figure 4 was used to test a low-power (<24dBm transmit power) bench-top prototype of the active node, using an ➢

AWG to supply a rising-edge trigger to the Cobalt module and signal generators to supply synchronized reference signals to the REX and the Cobalt module.

Using this system, it was possible to detect moving targets by their Doppler shift at close range, as shown in Figure 5. This data shows the doppler shift of a moving human target at approximately 75 meters from the transmitter, using a 0.5 micro second duration pulse with 50 MHz of bandwidth. Radial target velocity v and Doppler shift are related by the equation

```
v=c/2(Fd/Fc)
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where **c** is the speed of light, **Fd** is the Doppler shift, and **Fc** is the carrier frequency. With **Fc** = 8.5GHz (X-band) and **Fd** = 100 Hz at t=5s in the graph of Figure 5, the target is inbound at approximately 1.7 m/s. The large object seen moving from approximately 10 to 22 seconds and then from 30 to 32 seconds was a car backing out of a parking bay and driving away.

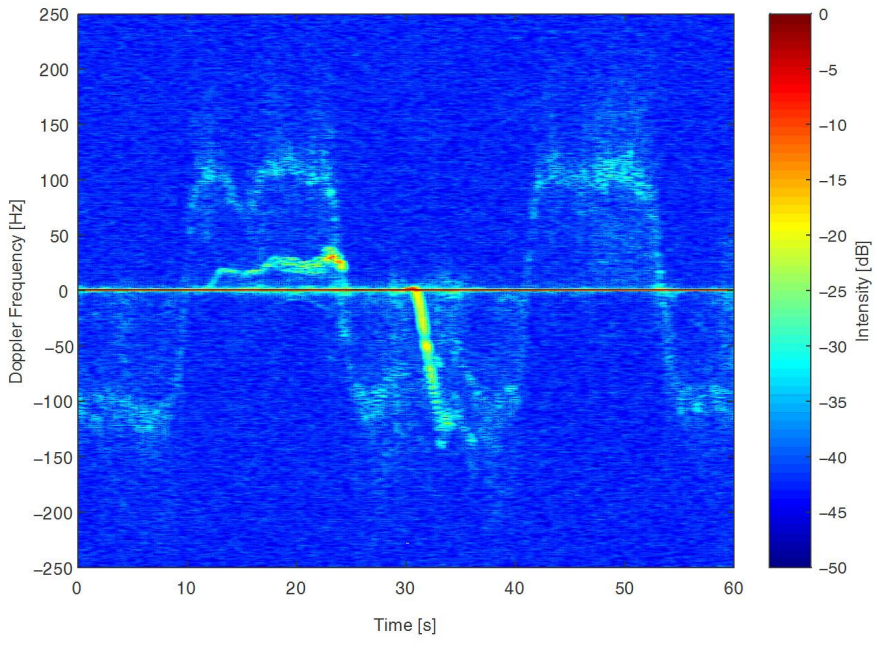
Passive nodes are essentially identical to the active node, except for the transmitters which are not needed. Using virtually the same controlling software for the Cobalt module in the active node, passive nodes can record waveforms at precisely the same moment as in the active node.

Summary

The initial testing of the Cobalt module in the active node of the system demonstrated that the Pentek Model 71621 was well-suited to a pulse-Doppler radar application. With the required additional hardware, the passive nodes can be introduced to the network with minor alterations to code for the active node's digital transceiver. Overall, the Cobalt module met our requirements for phase stability and bandwidth, and it was easily integrated with the existing receiver exciter for the active node.

The author would like to thank the following organizations for their generous financial support of the NeXtRAD project: ONR Global, the IET for the AF Harvey Research Prize, the South African National Defence Force, and the National Research Foundation of South Africa. ❐

Figure 5. A time against Doppler-shift of a moving human target at approximately 75 m range using an X-band signal.



Model 71821: A New Jade Architecture Module Ideal for Digital RF Memory Applications and More

Model 71821 is a three-channel, high-speed data converter with programmable DDCs (digital downconverters). Based on the Xilinx Kintex Ultrascale FPGA, this XMC module can be used in many high-performance applications.

Summary

- Multi-channel, wide-bandwidth, low latency and synchronous XMC module
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- One digital upconverter (DUC)
- Two 800 MHz 16-bit D/As
- Jade architecture with Xilinx Kintex Ultrascale FPGA offers price, power and processing performance advantages
- Navigator Design Suite expedites development and custom IP integration

The Model 71821 is ideal for engineers building a Digital RF Memory (DRFM) application where multi-channel inputs can digitize an incoming RF input signal at bandwidths up to 80 MHz and then generate a processed version of that RF signal as an analog output with very low and deterministic latency.

For DRFM radar applications, an incoming radar pulse is digitized and sent to the FPGA, which can apply a range of DSP algorithms before delivering the modified signal to the D/A for transmission back to the radar to simulate a reflected pulse. These algorithms are intended to confuse, deceive, or disable the radar, depending on mission objectives. Being a coherent representation of the original signal, the transmitting radar will not be able to distinguish it from other legitimate signals it receives and processes as targets.

If the signal is stored in memory, it can be used to create false range targets both behind (reactive jamming) and ahead of (predictive jamming) the target intended for protection. Slight modifications in frequency simulate Doppler shifts to create false target velocity. DRFM can also be used to create distorted phase-fronts, which is essential for countering monopulse radar angular measurement techniques.

"Our military, defense and aerospace customers can now take advantage of the Jade Architecture and our Navigator Design Suite," said Bob Sgandurra, director of Product Management of Pentek. *"Access to over 90 Pentek IP modules with industry-standard AXI4 interfaces reduces development costs and time through graphical design entry and high-level point-and-click interconnects."*

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing, data capture and routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. ➢

Model 71821

A/D Acquisition IP Modules

The Model 71821 features three A/D Acquisition IP modules for easily capturing and moving data. Each IP module can receive data from any of the three A/Ds or a test signal generator. Powerful linked-list DMA engines move the A/D data through the PCIe interface in a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate.

This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary. Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved, including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

D/A Waveform Playback IP module

The Model 71821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily generate waveforms stored in either on-board memory or host memory for both D/As. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

The Jade Architecture

The Pentek Jade architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by over 50% with equally impressive reductions in cost, power dissipation and weight. As the central feature of the Jade architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. A 5 GB bank of DDR4 SDRAM is available for custom applications. The memory to Gen. 3 x8 PCIe link can sustain 6.4 GB/s data transfers. Eight additional gigabit serial lanes and LVDS general purpose I/O lines are available for custom solutions.

Navigator Design Suite

Pentek's Navigator Design Suite was designed from the ground up to work with Pentek's Jade architecture and Xilinx's Vivado Design Suite®, providing an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility. Graphical design entry for Xilinx and Pentek AXI4-compliant IP modules using the Xilinx IP Integrator greatly speeds development tasks.

The Navigator Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek-sourced designs and Navigator BSP (Board Support Package) for creating host applications. Users can work efficiently at the API level for software development and with an intuitive graphical interface for IP design. The Navigator BSP is available for Windows and Linux operating systems.

SPARK System

With a Pentek 8266 SPARK® PC, 8264 SPARK 6U VPX, or 8267 SPARK 3U VPX development system, work can begin immediately on applications. A SPARK system saves engineers time and expense associated with building and testing a development system and ensures optimum performance of Pentek boards.

SPARK development systems are ready for immediate operation with software and hardware installed. In many applications, the SPARK development system can become the final deployed application platform.

Form Factors

The Model 71821 XMC module is designed to operate with the wide range of carrier boards in PCIe, 3U & 6U VPX, AMC, and 3U & 6U CompactPCI form factors, with versions for both commercial and rugged environments.

For more information:

For more information, go to http://www.pentek.com/go/71821

Contact us!

For the latest pricing, delivery and available options, please fill out this form and your request will be delivered to the appropriate department. To learn more about our products or to discuss your specific application please email our sales department at sales@pentek.com, contact your local representative or Pentek directly [+1 (201) 818-5900]. ❐

Model 71851: A New Jade Architecture Module for Wideband Signal Capture and Generation

Model 71851 is based on the Xilinx Kintex Ultrascale FPGA and features two 500 MHz, 12-bit A/Ds with multiband digital down converters (DDCs), one digital upconverter (DUC) and two 800 MHz 16-bit D/As..

Summary

- Wideband, low-latency, synchronous XMC module
- Two 500 MHz 12-bit A/Ds with multiband DDCs
- Wideband digital upconverter feeds two 800 MHz 16-bit D/As
- Jade architecture with Xilinx Kintex Ultrascale FPGA offers price, power, and processing performance advantages
- Navigator Design Suite expedites development and custom IP integration

Application Scenario: The Model 71851 offers a well-matched 200 MHz bandwidth on both the receive-side and on the transmit-side, which provides the complementary solution necessary in many high-speed data acquisition, waveform generation, communications, satcom, UAV, and radar applications.

One high-performance application, requiring wide bandwidth signal generation and capture, is a ground-penetrating radar system that can detect hazards hidden below the surface. The Model 71851 can be used in a low-altitude aircraft or UAV as the front-end to this type of system. The Model 71851 has the bandwidth and processing power necessary to create signals that can penetrate the ground at a greater depth and then capture return signals with greater resolution while allowing the aircraft to fly at a safe traveling velocity to eliminate detection.

"Not only do customers of the Jade Model 71851 benefit from its lower cost, lower power and additional processing power, they can slash application design time with Pentek's Navigator development tools," said Robert Sgandurra, director of Product Management. He added, *"By listening to customer requests, Pentek has added features in the IP and software to improve the functionality of our boards, such as the new operational modes for the D/A converters in the 71851. The previous IP module was limited to feeding data to both D/A channels in tandem, but now streams for the two D/As are fed from two separate DMA engines. While retaining the previous synchronous capability, customers also start and stop each output waveform data stream independently, providing more flexibility for more advanced applications."*

A/D Converter Stage

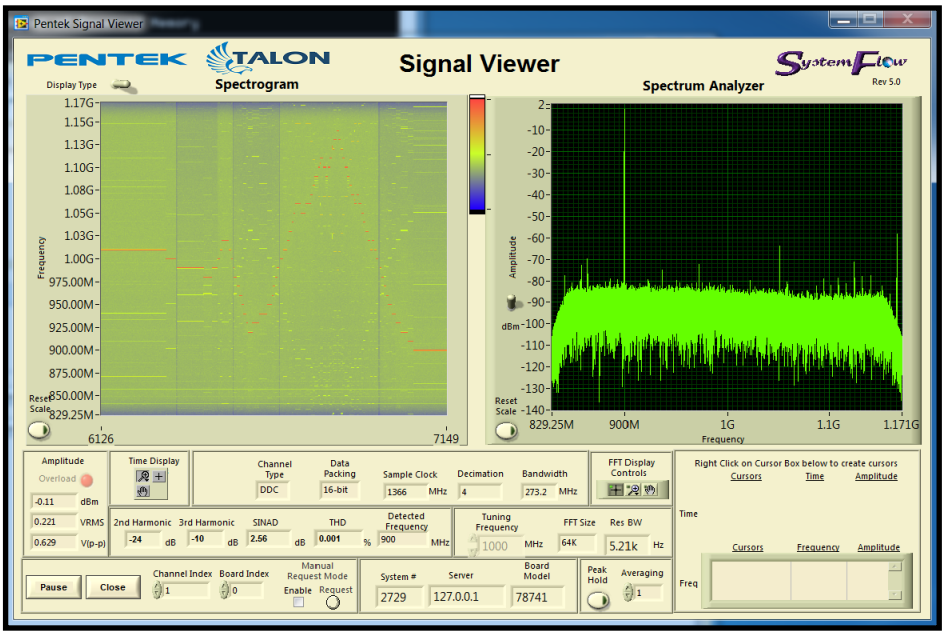
The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463 for those that need better resolution. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing, data capture and routing to other module resources.

Other features:

Some features of Model 71851 are similar to or the same as Model 71821. See

- Digital Upconverter and D/A Stage
- Clocking and Synchronization
- A/D Acquisition IP Modules
- D/A Waveform Playback IP module
- The Jade Architecture
- Navigator Design Suite
- SPARK System
- Form Factors

Or go here for more Model 71851 information. Or Contact us! ❐



Pentek's Talon Recorders' SystemFlow Software Touts New Features and Enhancements

Pentek has added new features and enhancements to its Talon® SystemFlow® software that improve the ease-of-use and recording capabilities of the entire line of Talon Recording Systems. The optimized enhancements to SystemFlow benefit radar, SIGINT and communications recording applications where reliability, speed and data integrity are mission-critical.

SystemFlow is the software interface that is integrated into every Talon recorder. The software includes the graphical user interface (GUI) that is used to control the recorder with point-and-click configuration management, a client/server communication interface, NTFS file system support, and an application programming interface (API) for custom user applications and control. Signal analysis tools include a virtual oscilloscope, spectrum analyzer, and spectrogram to monitor signals before, during, and after data collection. A summary of the new enhancements to the SystemFlow software is provided below.

"Each of our customers has a unique recording need," stated Chris Tojeira, director and chief architect of the Talon Recording Systems. *"We've listened carefully to customer feedback and have added features and enhancements that expand the recording and display capabilities of our high-performance Talon recorders, all while making the systems easier to use."*

Ease-of-Use Features and Capability Improvements

Auto File Naming: An auto-file-naming facility allows files to be automatically named intuitively using date, time-of-day, and channel information.

One-Click Profiles: Unique recording system configurations can be saved and then later retrieved with a single click, minimizing mistakes made by field operators.

Segmented Recording: A segmented recording option allows large recording sessions to be recorded as smaller, manageable files. Operators select the desired segment size.

Data Extraction Utility: The SystemFlow File Viewer provides a signal analysis tool for analyzing recordings. A built-in data extraction utility allows users to quickly and easily scan through a recording to find signals of interest and extract them to smaller, more manageable files.Time stamping is preserved during the data extraction process.

Targeted Recording Modes

Looped Recording: Looped recording runs indefinitely, overwriting the oldest data while operators wait for an interesting event to be captured. Loop buffer size is user-selectable to support hours, days, or even weeks of continuous recording storage.

Pulsed Radar Recording: Data is recorded only when the recording gate signal is true. A metadata packet with information about the corresponding pulse, including the pulse number, time stamp, and pulse width, can be used to reconstruct the pulse train and preserve the exact time it was recorded. This is useful for radar systems, where the user only ➢

wants to capture the signal during the range gate.

GPS functions for Target Triangulation and Time Stamping

Auto-Initiated Recording: Using a 10 MHz reference and 1PPS pulse from local GPS receivers allows multiple systems to automatically start recording synchronously.

GPS Position Tracking: Periodically logs latitude, longitude and altitude during signal recordings on flight missions.

Enhanced Display Feature:

SystemFlow Signal Viewer: The viewer now includes a scrolling spectrogram display to quickly view the entire spectrum under surveillance over time.

Data Security Measures:

AES 256-bit Encryption: Optional AES 256-bit encryption provides data security for sensitive information.

Instant Secure Erase: Optional Instant Secure Erase offers an extremely quick means to sanitize disks.

Talon Recorder Family

Pentek's Talon Recording Systems are high-speed recording and playback systems capable of streaming data to disk in real time. Storage capacity options allow contiguous recording for hours and even days. A variety of front ends allow users to record analog or digital signals. They are available in portable, rackmount, and small form factor configurations, allowing operation in a variety of environments.

RTV Value Systems: These economically priced entry level systems for benign environments are available with optional GPS time and position stamping and IRIG-B time stamping.

RTS Laboratory Systems: Intended for benign environments, they offer great flexibility in channel count. They can store hundreds of terabytes of data on HDDs (hard disk drives). These recorders come in a rack-mountable PC server chassis.

RTR Rugged Systems: The rugged series comes in a portable (briefcase style) or rack-mountable PC server chassis. Both use SSDs (solid state drives) to handle operational shock and vibration. Enhanced cooling capabilities support higher-temperature environments (up to 55°C.) The RTR series recorders provide maximum streaming data rates.

RTX Extreme Systems: The extreme rugged series are flight certified, capable of handling high levels of shock and vibration as well as high-altitude use. The RTX series chassis use Pentek's QuickPac® drive hot-swap packaging technology for quick removal and replacement of data storage SSDs, especially useful during flight missions where aircraft time is critical.

Availability:

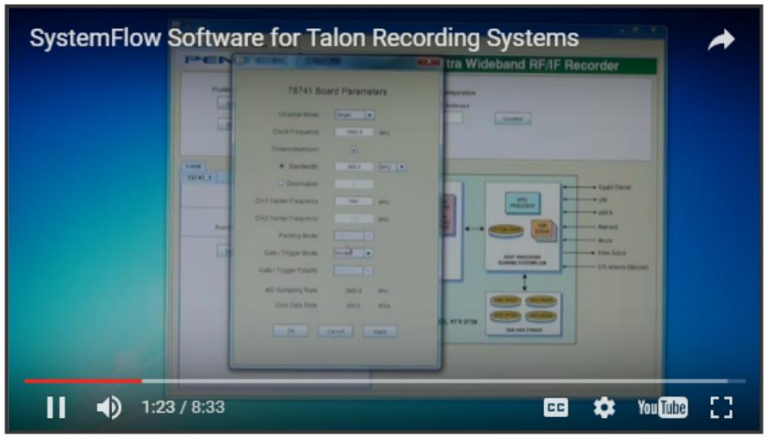
The SystemFlow software is included with the purchase of any new Talon recording system, and is not sold separately. Some of the new enhancements are available as standard features and some are available upon request.

For more information:

More information about SystemFlow software can be found here:
http://www.pentek.com/go/systemflow

To access the Talon FAQs, go here:
http://www.pentek.com/go/talonFAQ

To download the Talon catalog, click on the image below. ❒



Take a video tour of SystemFlow software
Click on the image above to view the video.