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The Pentek Pipeline
A quarterly publication for engineering system design and applications.

In This Issue

- **Feature:** In this issue, Bob Sgandurra discusses the challenges of FPGA design and how Pentek's new Navigator Design Suite addresses these challenges.

"FPGA logic design and the software to control it are intimately tied together. This relationship and the need to keep FPGA IP changes and software changes in sync are a reality that must be managed in the design environment of sophisticated FPGA-based systems."

Bob Sgandurra, Director, Product Manager of Pentek

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Navigating FPGA Design

by Bob Sgandurra, Pentek, Inc.

Over the past 35 years, there has been a constant progression of technologies for performing digital signal processing. Some of these have been in the form of processors dedicated to the task of efficiently executing complex math in parallel such as Digital Signal Processors (DSPs) from Texas Instruments and Analog Devices and other specialized processors from other manufacturers.

Another path has been to exploit the specialized processing engines inside more general-purpose processors from companies like Intel and Motorola, or to re-purpose highly parallelized processors like Graphics Processing Units (GPU) for DSP applications like RADAR.

In each of these examples, it has been the software engineer's job to create programs or applications for a fixed hardware architecture. This might be accomplished by programing on the "bare metal" and accessing internal registers and resources of the processor directly, or through the window of an operating system that manages the processor's resources.

Field Programmable Gate Arrays

This paradigm changed with the introduction of programmable logic devices, and specifically with the advent of **Field Programmable Gate Arrays (FPGAs)**. An FPGA's logic is a mesh of gates and interconnects that have no function until a logic design is loaded into the array connecting the gates to form circuits. Modern FPGAs can contain millions of logic gates and thousands of embedded DSP processors, allowing FPGA hardware designers to create extremely sophisticated and complex application-specific hardware functions. And this is where the job of the software engineer takes a turn.

A New Challenge for the Software Engineer

With fixed targets like Texas Instruments DSPs or Intel processors, the software engineer writes programs for a static and well-defined hardware architecture. But with FPGAs, the functions and even the interfaces into the hardware are determined by which logic design the FPGA engineer uses to configure the FPGA, and this can change with different iterations of the design.

FPGA logic design and the software to control it are intimately tied together. This relationship, and the need to keep FPGA IP changes and software changes in sync, are a reality that must be managed in the design environment of sophisticated FPGA-based systems. ➢

Increasing Complexity = An Increasing Challenge

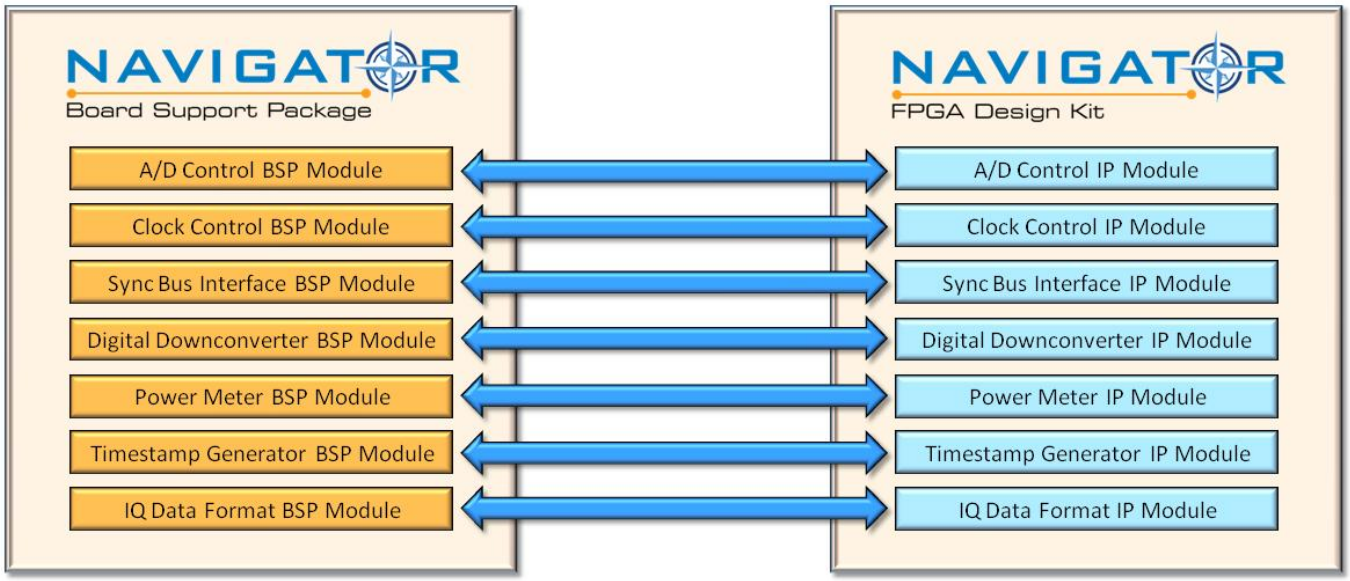
The increasing complexity of high-performance FPGAs has made the task of the FPGA designer increasingly demanding. The logic design, sometimes called Intellectual Property or IP, is typically created using VHDL or Verilog, which are hardware description languages for designing processing logic. Although these languages are the cornerstone of FPGA design, new tools and design environments can improve design efficiency, particularly when designing for very large FPGAs with millions of gates.

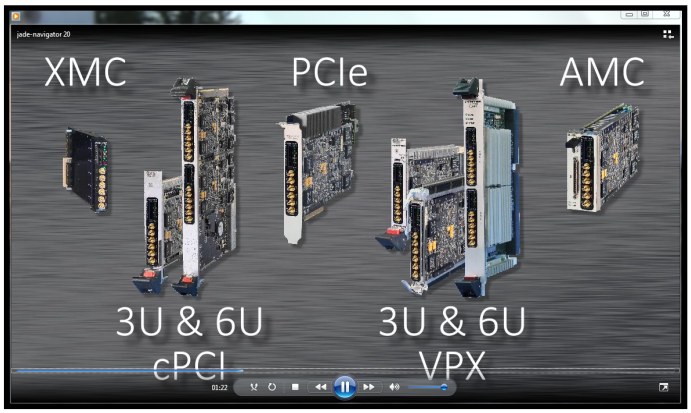
Pentek's Navigator Helps Navigate the Complexity

Pentek's new **Navigator™ Design Suite** (see Figure 1) addresses these challenges with solutions for both FPGA and software engineers. The Navigator Design Suite was designed from the ground up to work with Pentek's new **Jade™** architecture products and provides an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility.

The Navigator Design Suite contains two separate but closely related products: the **Navigator FPGA Design Kit (FDK)** for integrating custom IP into Pentek-sourced designs and the **Navigator Board Support Package (BSP)** for creating host applications. Users are able to work efficiently at the API level for software development and with an intuitive graphical interface for IP design. Let's look at two design scenarios and how the Navigator Design Suite can be used in each. ➢

Figure 1. Navigator Design Suite





Watch the Video!

This four-minute video provides a quick overview of Pentek's new Jade family of products and new Navigator Design Suite software.

To watch the video, go here:

http://www.pentek.com/go/jade-navvideo.

Scenario 1: No FPGA Customization Needed

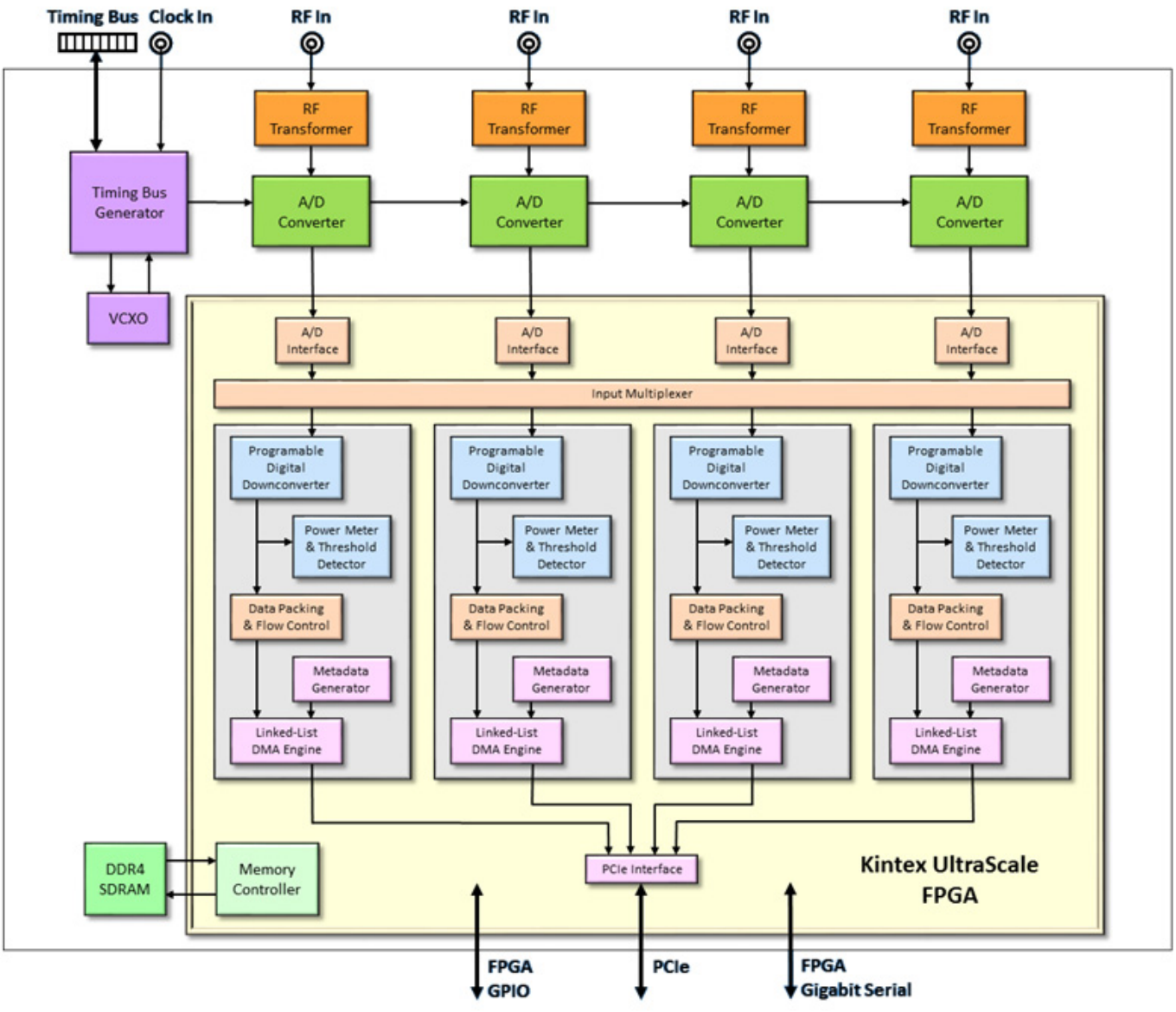
Found at the center of every Pentek data acquisition and processing hardware product is an FPGA. Pentek's new Jade family uses a Xilinx® Kintex® Ultrascale® FPGA. Like all Pentek products, Jade includes a full suite of built-in FPGA-based functions (see Figure 2). In the case of an A/D converter product, these functions include:

- an A/D data acquisition engine,
- a fully-programmable DDC,
- power meters and a threshold detect function,
- a timestamp and metadata creation engine, and
- a linked list DMA engine that allows users to customize data transfers to a host computer.

In many cases, users will find that the built-in functions satisfy all the requirements of their application and no custom FPGA IP is needed. For these users, the FPGA looks like just another piece of hardware with fixed functions and a fixed interface for status and control.

In this situation, the **Navigator BSP API** is the best solution for creating applications that control the Jade hardware. Provided as a C-callable high-level API, many of the most commonly used built-in functions can be controlled with simple ➢

Figure 2. Jade Model 71861 Built-in FPGA Functions



commands. In addition, example programs and the included Signal Viewer (see Figure 3) allow users to immediately start acquiring and displaying data in the time and frequency domains without the need for creating any code.

Scenario 2: Customizing the FPGA IP

But what if an application requires special processing that only custom IP can provide? (See Figure 4.) The solution is the **Navigator FDK**. It was created to work directly with the Xilinx Vivado® Design ➢

Figure 3.Signal Viewer

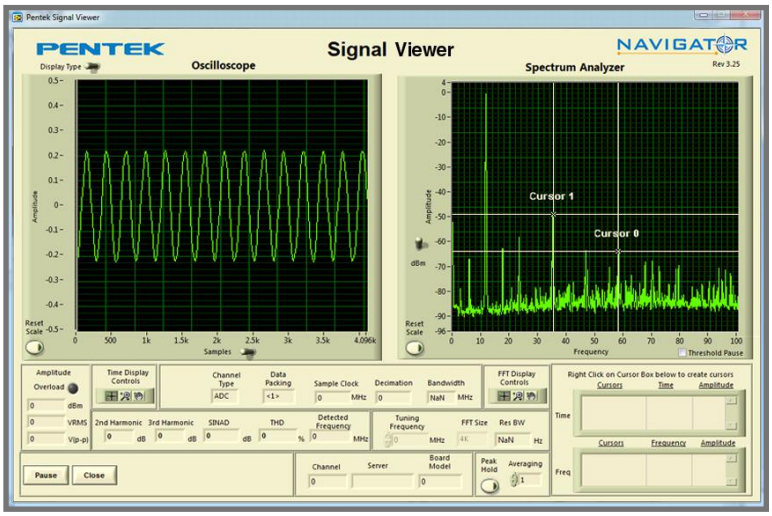


Figure 4. User-Created IP

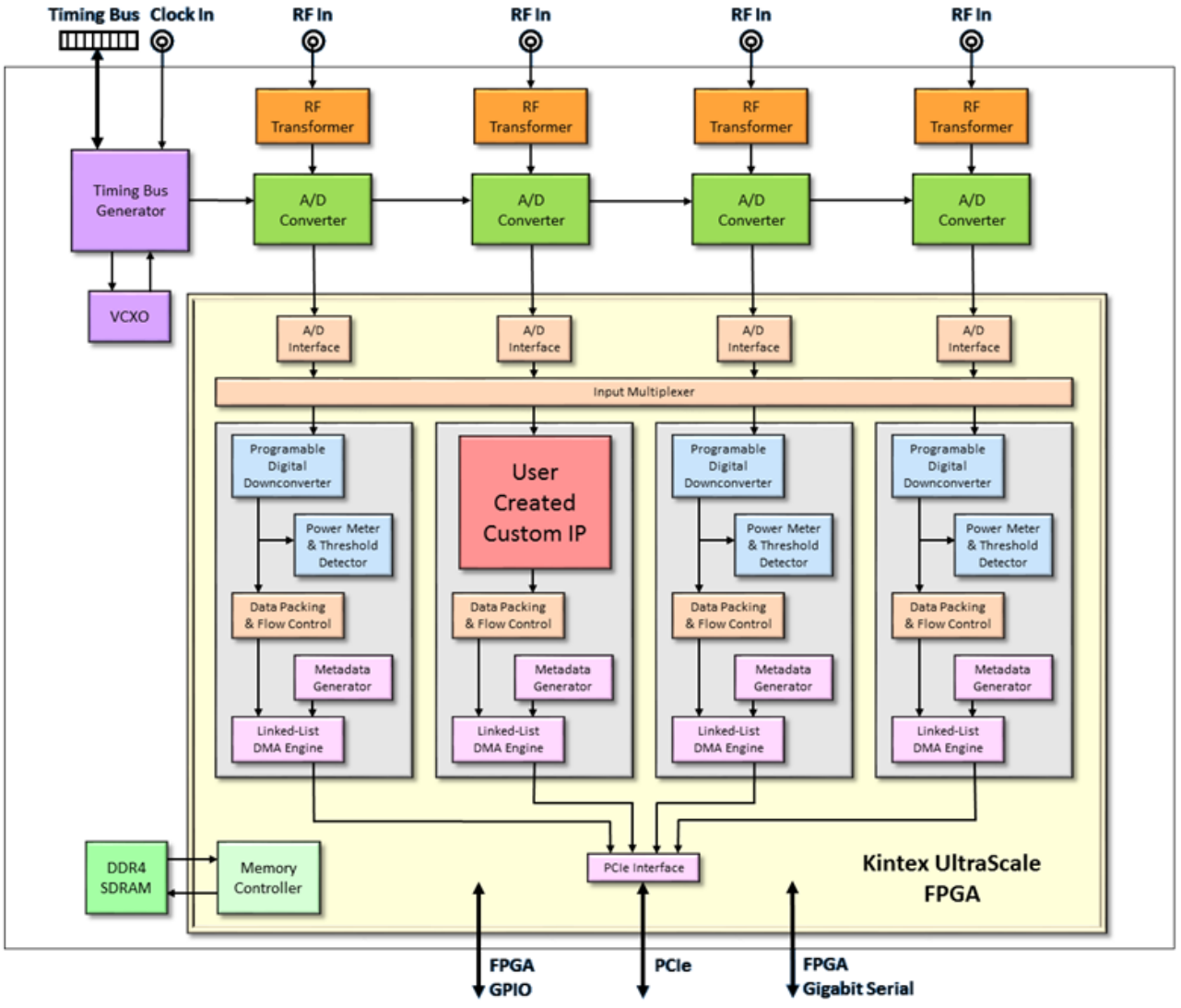
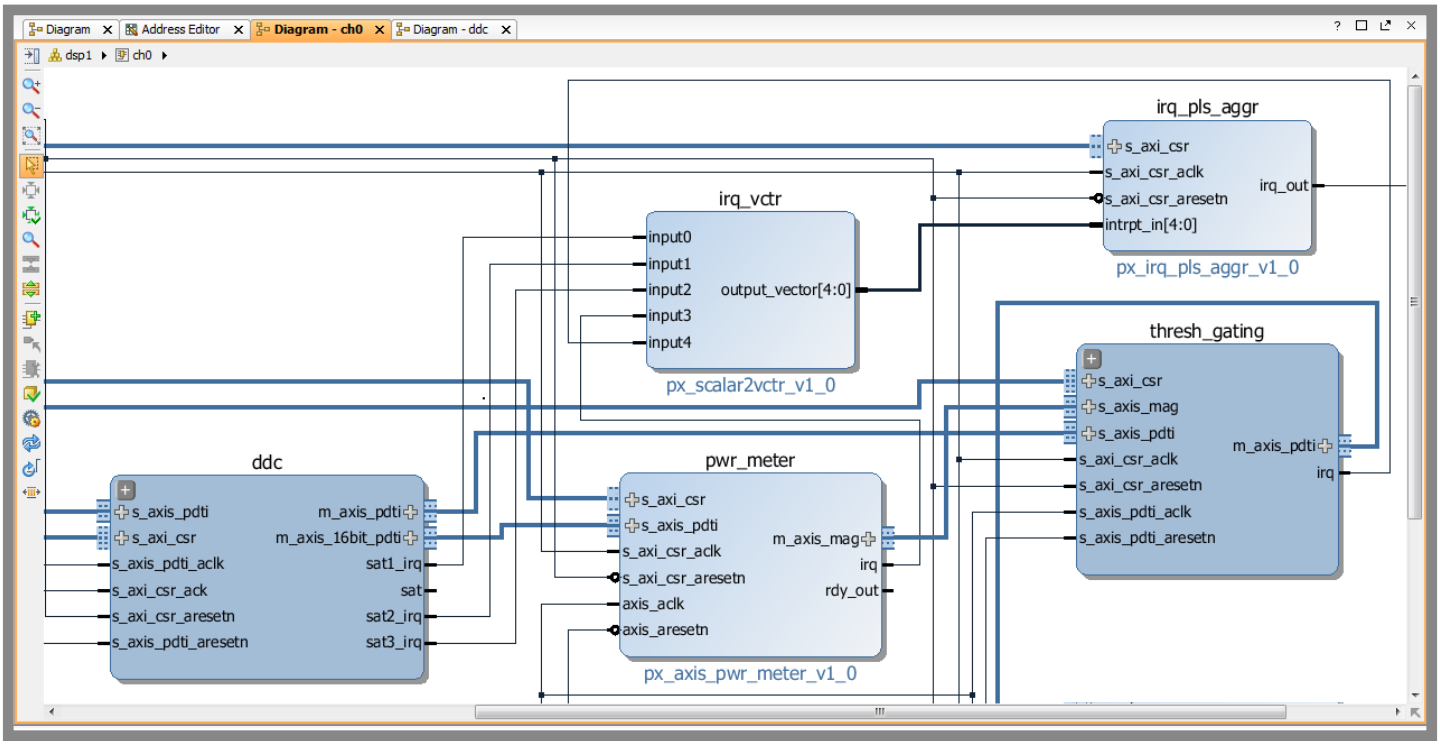


Figure 5. Jade Model 71861 Navigator FDK Design in IP Integrator



Suite and creates a seamless environment for developing IP on Pentek products. The Navigator FDK leverages two new features in Vivado to greatly streamline IP development: the **AXI4 standard** and the **IP Integrator**.

The AXI4 Standard

AXI4 is the 4th generation of an interface specification from ARM® commonly used in the semiconductor industry. Xilinx has adopted this standard to create AXI4-compliant plug-and-play IP. The benefits can be seen immediately:

- AXI4 consolidates an array of different possible interfaces into a single well-defined interface.
- AXI4 manages differences in bus speed and width when connecting IP blocks.
- AXI4 allows easier integration of IP from different sources when all IP is using the same interface.
- AXI4 still allows enough flexibility to enable IP designers to tailor the interconnects to meet system performance requirements.

Navigator FDK follows the AXI4 standard. For Pentek's Jade data acquisition and processing products, the FDK includes the complete IP that is factory-installed in the board. This includes all interface, processing, data formatting, DMA functions, etc. IP designers can modify or replace functions as needed to match application requirements, and will find immediate compatibility with Xilinx IP and third-party IP that uses AXI4. Designers who create their own custom IP using the AXI4 standard will find integration with the Pentek-supplied IP straightforward.

The IP Integrator

So how is the FPGA design actually edited? This is where Navigator FDK exploits another new feature of Vivado: the IP Integrator (see Figure 5). The concept of creating FPGA designs by connecting blocks in a graphical interface, similar to drawing a schematic, is not new, but Xilinx's IP Integrator makes it a practical solution.

To edit a Pentek product design, an FPGA engineer opens the Navigator FDK design in Vivado. He then has immediate access to the entire board design as a block diagram. Individual IP cores can be removed, modified, or replaced with custom IP to meet the application's processing requirements. Because all blocks have AXI4 interfaces, connections between blocks can simply be "drawn" with wires or buses and the AXI4 interface handles the "housekeeping" of different bus speeds or widths.

Viewing an FPGA design as a block diagram enables the designer to see the data flow and simplifies the design processes by working at the "interface" and not the "signal" level. If, at any time, a designer needs to work with the VHDL code directly, it is always accessible in a source window, as well as full on-line documentation for every Pentek IP core. ➢

Once a board's function has been modified by changing FPGA IP, it is most likely that changes will need to be made in the software controlling the board to support the new function (see Figure 4). While the Navigator's API is ideal for creating applications for the board, it assumes the board functions have not changed from the factory-installed set.

The Role of Navigator BSP

Once custom IP is introduced in the FPGA, the Navigator BSP module library is the solution for modifying or creating new software. Designed to work with the Navigator FDK, the Navigator BSP is structured to simplify this process. Each Navigator IP core module found in the FDK has an equivalent software module with a similar name in the Navigator BSP (see Figure 1). Changes made to an IP module can be easily traced back to the BSP module to make the necessary changes to control the new IP. This one-to-one relationship between IP and software greatly simplifies the task of keeping IP and software in sync.

Learning More: The IP Core Tutorial

The Navigator FDK's plug-and-play compatibility depends on IP cores following the industry standard AXI4 interface specification. A great place to start learning more about AXI4, Xilinx's IP Integrator, and Pentek's Navigator FDK is the *Navigator IP Core Tutorial*. This 100-page guide introduces the AXI4 interface and how it's used in Navigator and IP design. It also includes a complete learning lab to follow in Vivado that shows how to create a new core that is immediately compatible with Xilinx and Pentek IP.

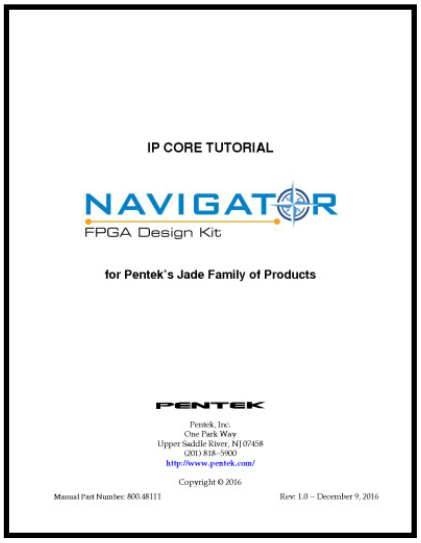
To get this tutorial, contact Mario Schiavone at 201-818-5900 or mario@pentek.com.

For more information about Pentek's Navigator Design Suite, go to http://www.pentek.com/go/navigator.

For more information about Pentek's Jade products, go to http://www.pentek.com/go/jade.

This issue of Pipeline also features three Jade boards: Pentek's First Jade™ XMC Modules: Models 71841, 71861, and 71131 .

To watch a video about Jade and Navigator, go here: http://www.pentek.com/go/jadenavvideo. ❒



Pentek's IP Core Tutorial

Two Recent Webcast Seminars

To view a webinar, click here, register, and launch the presentation.

FPGAs: A Game Changer for Military Communications

FPGAs have been a force multiplier for military signal processing applications that require modularity and flexibility. For military communications applications, they enable designers of software defined radio and satellite communication systems to develop open-architecture, configurable board-level FPGA solutions for use in current and new systems. This webinar covers the implementation of FPGAs in military communication systems - from challenges to benefits.

Military ISR Sensors and Embedded Signal Processing

Industry experts discuss how embedded signal processing solutions are empowering the sensor chain in military intelligence, surveillance, and reconnaissance (ISR) systems.

JADE

"Pentek's new Jade architecture gives our customers unprecedented levels of performance at significantly lower product cost.

We also created new software development tools to align with the latest industry standards and Xilinx development tools, providing a more intuitive and productive development environment."

Rodger Hosking,
Vice President of Pentek

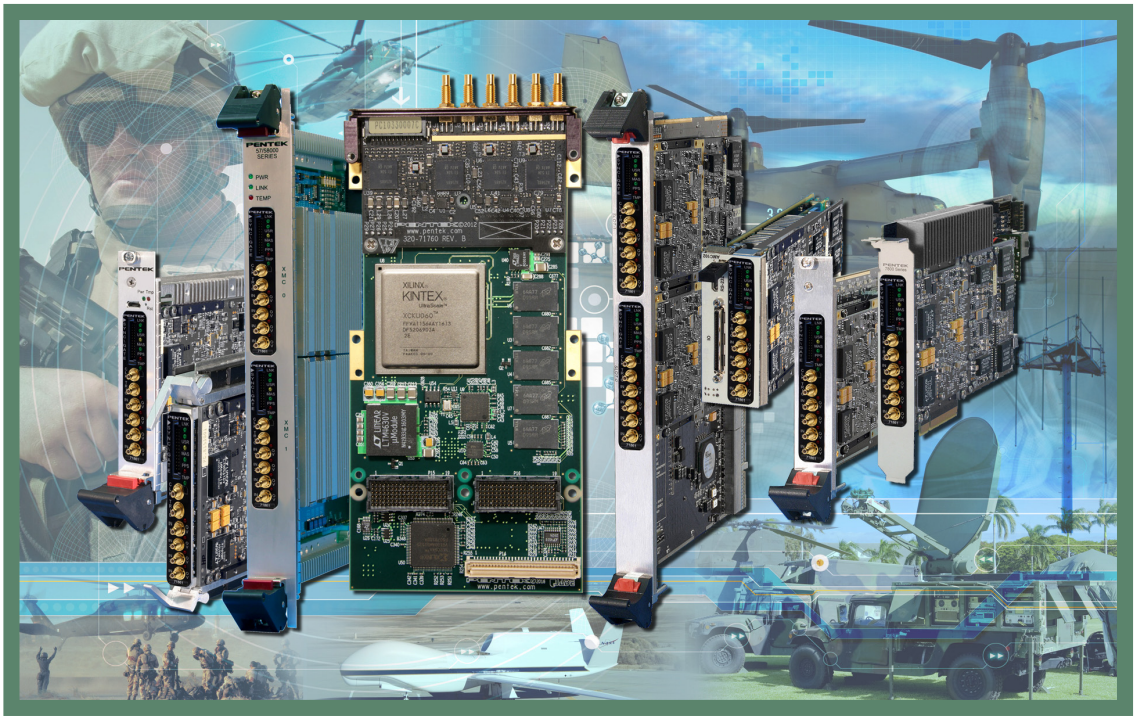
In September 2016, Pentek introduced the new Jade™ family of XMC products. Evolved from the proven designs of the Pentek Cobalt® and Onyx® architectures, Jade is based on the Xilinx flagship Kintex UltraScale FPGA, which significantly raises the digital signal processing (DSP) performance by almost 50 percent. Equally impressive are reductions in cost by 39 percent and power dissipation by 23 percent.

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

The Jade architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. The board features a Gen.3 x8 PCIe interface along with eight additional gigabit serial lanes and LVDS general-purpose I/O for custom solutions.

As the central feature of the Jade architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering, and memory control. The Jade architecture organizes the FPGA as a container for data processing applica-tions where each function exists as an intellectual property (IP) module.

The Navigator™ Design Suite was designed from the ground up to work with Pentek's new Jade architecture and provides an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility. The Navigator Design Suite is described in more detail in the previous article: "Navigating FPGA Design" on page 1. ❐



All Jade modules are available in XMC, PCIe, 3U/6U VPX, AMC, and rugged versions.

Pentek's First Jade™ XMC Modules: Models 71841, 71861, and 71131

Also available in VPX, cPCI, AMC, and rugged versions

Model 71841

Designed for extremely wideband signal applications, the Jade Model 71841 XMC module is available in either of these configurations:

- **1-channel, 3.6 GHz 12-bit A/D**
- **2-channel, 1.8 GHz 12-bit A/D**

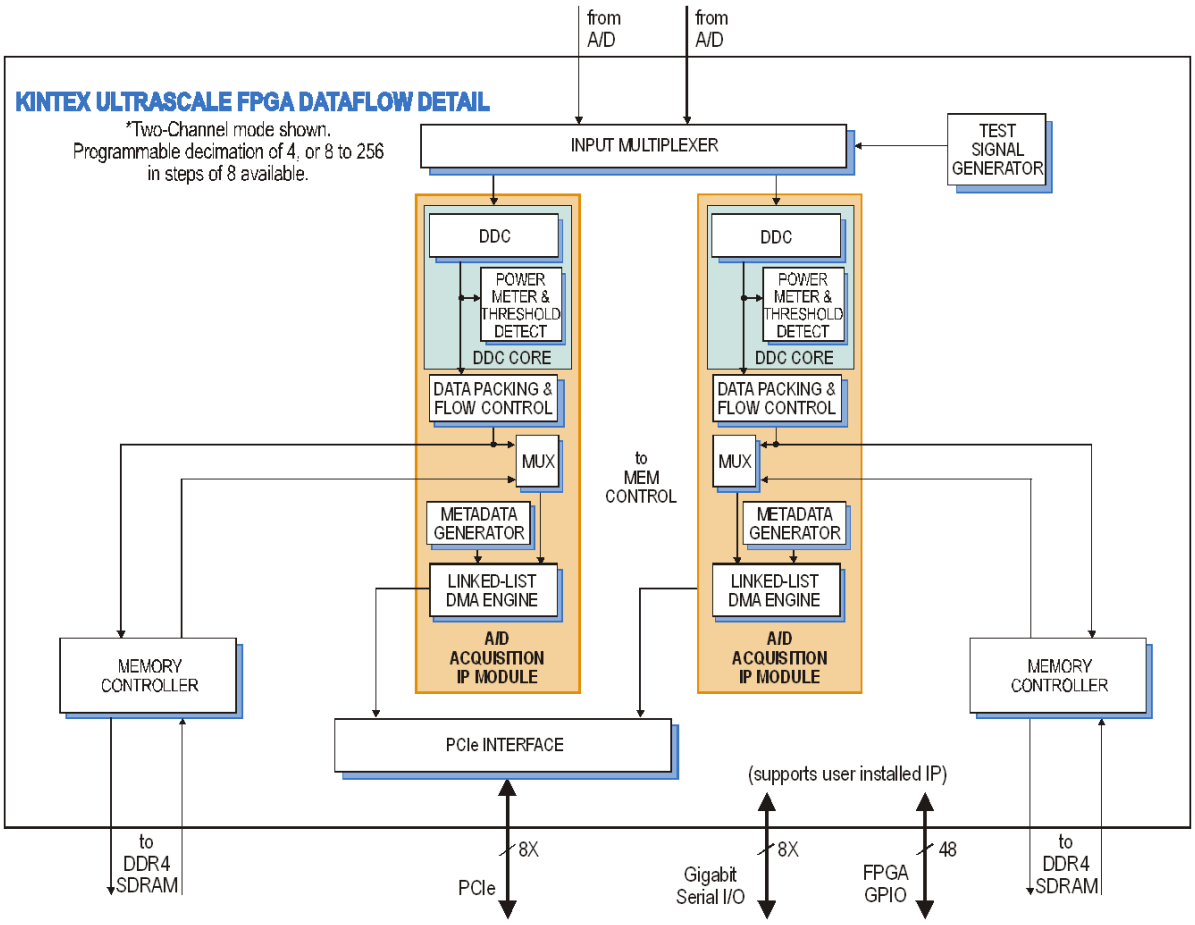
Model 71841 is based on a Xilinx Kintex Ultrascale FPGA (see Figure 6).

The Model 71841 comes preconfigured with a suite of built-in functions for data capture, synchronization, time tagging and formatting, making it an ideal turn-key interface for radar, communications or general data acquisition applications. The Model 71841 features an A/D acquisition IP module and a programmable DDC for easy data capture and moving.

Single-channel mode decimation can be programmed to 8, or 16 to 512 in steps of 16. Dual-channel mode decimation can be programmed to 4, or 8 to 256 in steps of 8, with both channels sharing the same decimation rate. In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting ranging from DC to the A/D sampling frequency.

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate up to 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode ➢

Figure 6. FPGA Dataflow Detail for Jade Model 71841



"Model 71841 significantly boosts performance, with considerable savings in power consumption, cost, and weight. Our customers are excited to take advantage of the Jade Architecture and our new Navigator tool suite for their next development projects."

Paul Mesibov,
Vice President, Engineering,
Pentek

with a sampling rate up to 1.8 GHz and input bandwidth of 2.8 GHz. The full scale input level can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in synchronization feature supports A/D synchronization across multiple modules.

For more information about Jade Model 71841, go to http://www.pentek.com/go/71841.

Model 71861

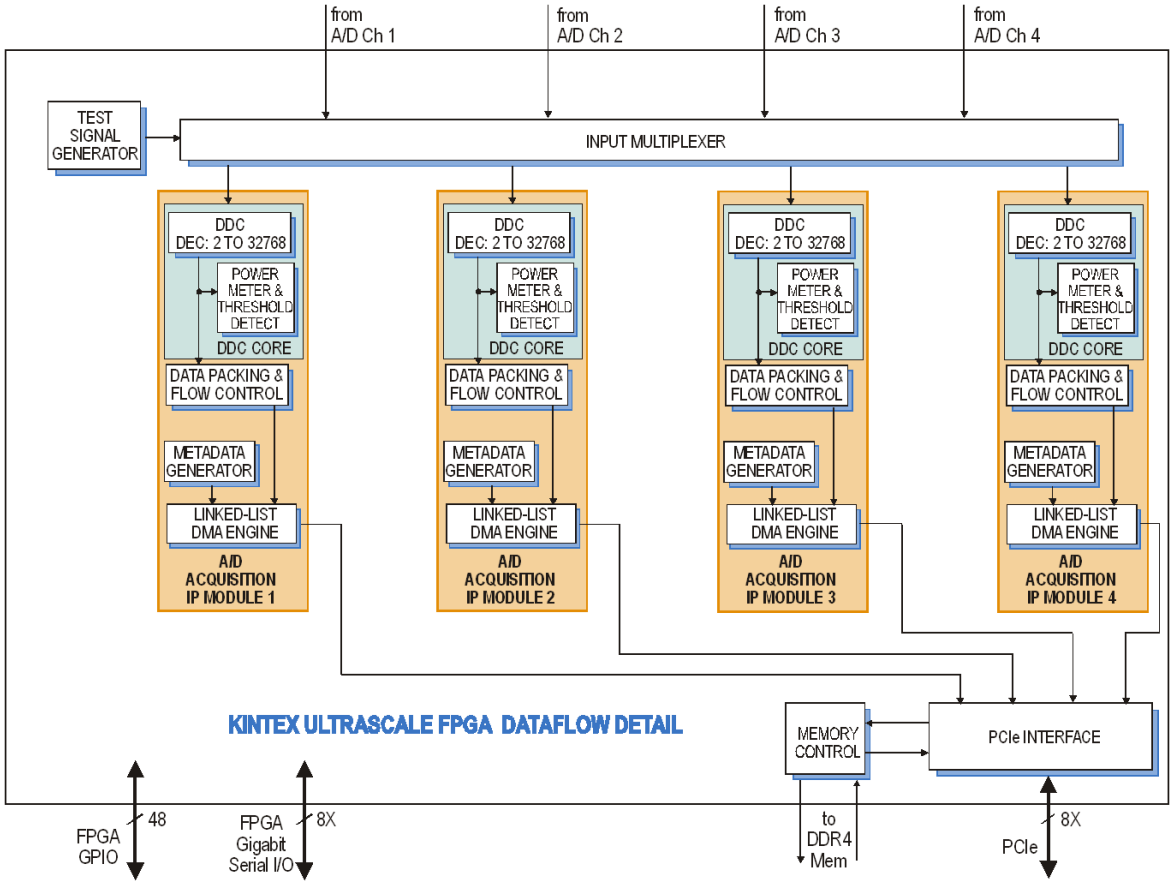
The Jade Model 71861 is a multichannel, high-speed data converter with programmable DDCs . It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP (see Figure 7).

It includes four A/Ds, a complete multiboard clock and sync section and the option for a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other module resources.

For more information about Jade Model 71861, go to http://www.pentek.com/go/71861. ➢

Figure 7. FPGA Dataflow Detail for Jade Model 71861



Model 71131

The Jade Model 71131 is a multichannel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O (see Figure 8).

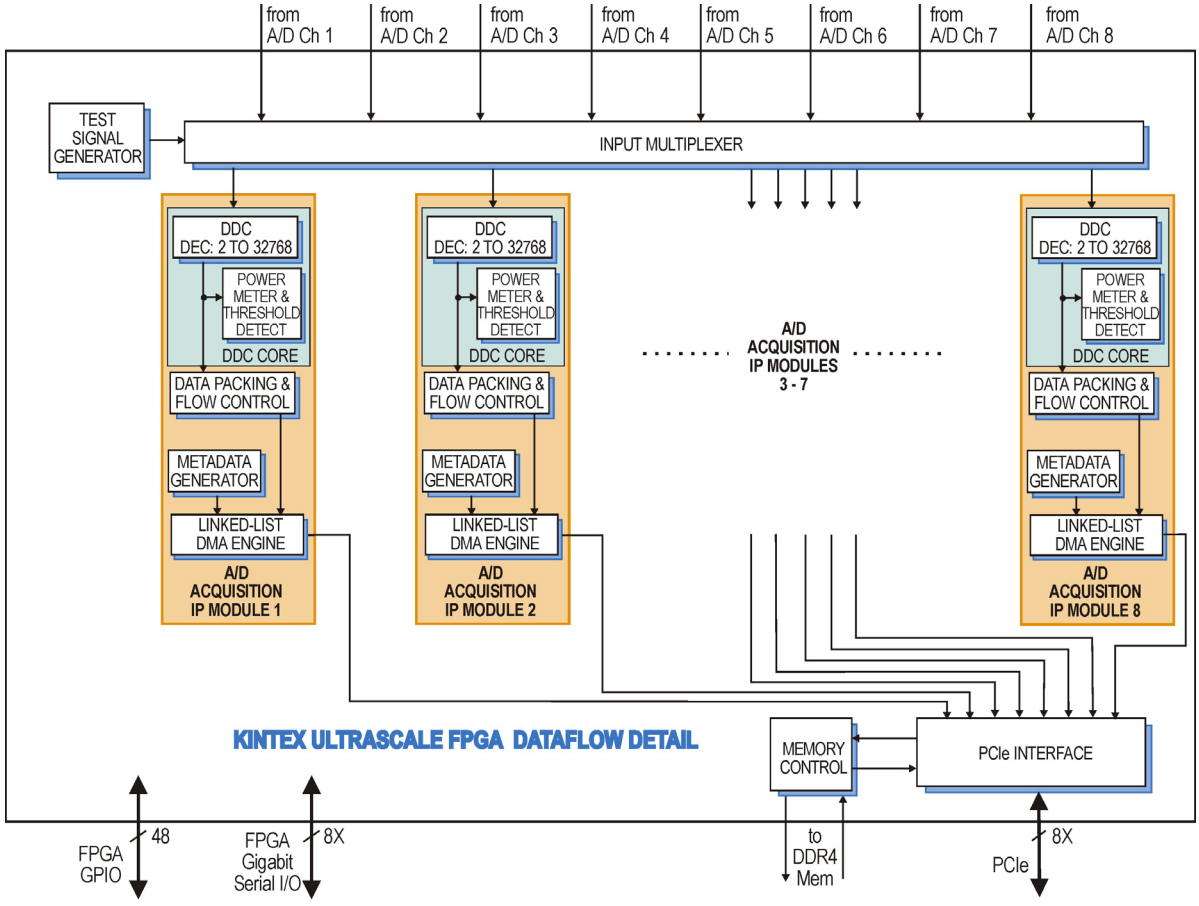
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71131 to operate as a complete solution for many applications, thereby saving the cost and time of custom IP development.

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other module resources.

For more information about Jade Model 71131, go to http://www.pentek.com/go/71131. ❐

Jade Model 71131

Figure 8.FPGA Dataflow Detail for Jade Model 71131



Pentek Introduces a New Portable, Rugged Sentinel Intelligent Signal Scanning Recorder

Pentek's **Talon® RTR 2623** offers the following features:

- **Scan and search from 20 MHz to 6 GHz at 30 GHz/sec scan rate**
- **Automatically tune, detect and record signals of interest**
- **Capture instantaneous RF signal bandwidths up to 40 MHz**
- **Portable and rugged system for mobile applications**
- **Storage capacities to 30 TB**

The Talon RTR 2623 combines and exploits the power of a Pentek Talon recording system with a fully-integrated 6-GHz RF downconverter. The Sentinel capability adds intelligent signal scanning with real-time signal monitoring and detection that is fully user configurable.

The Talon RTR 2623 is configured in a small-footprint portable package measuring only 16.0" W x 6.9" D x 13.0" H and weighing 30 pounds. The portable and rugged RTR 2623 recorder is a grab-and-go portable recorder suitable for mobile military, security, and government intelligence (SIGINT, COMINT, and ELINT) applications. The recorder performs in nearly any mobile platform, even when subject to challenging levels of vibration.

A Pentek Model 78621 Cobalt® transceiver module serves as the data acquisition engine of the Talon RTR 2623. Its 200 MHz 16-bit A/D converter provides 86 dB of spurious-free dynamic range and 74 dB of SNR. A digital downconverter provides frequency zooming for signal bandwidths as low as a few kHz. The Model 78621 is coupled to a 6 GHz RF tuner front end with excellent dynamic range across its entire spectrum.

The Talon RTR 2623 Sentinel Intelligent Scanning Recorder:
"Intelligence is Now Portable"

Sentinel users can scan the entire available spectrum or select a region of interest. Selectable-resolution bandwidth allows for the trading of sweep rate for a finer resolution and better dynamic range. RF energy in each band of the scan is detected and presented in a waterfall display. Any RF band can be selected for real-time monitoring or recording. The Sentinel hardware resources are controlled through enhancements to Talon's SystemFlow® software package.

***"The RTR 2623 can reliably and intelligently capture massive amounts of signal data in real-time, all within a compact, rugged, and highly portable package,"* said Rodger Hosking, vice-president of Pentek. *"The deep storage capacity provides hours and hours of data capture and the intuitive user interface outclasses other types of equipment on the market,"* he added.**

Talon Sentinel recorders are built on a Windows 7 Professional workstation with an Intel Core i7 processor and provide both a GUI and API to control the system. Systems are fully supported with Pentek's SystemFlow software for system control and turn-key operation.

The SystemFlow software has been enhanced to include intelligent scanning and integrated control of the RF tuner and optional RF upconverter. The software provides a GUI with point-and-click configuration management and can store custom configurations for single-click setup. It also includes a virtual oscilloscope, spectrum analyzer, and spectrogram to monitor signals before, during and after data collection. For more information, go to http://www.pentek.com/go/pipe2623. ❐

A New Rugged and Lightweight Portable Talon RF/IF Signal Recorder

Pentek's **Talon RTR 2727A** offers the following:

- **Digitizes up to four channels of analog RF/IF signals at 500 MS/sec**
- **Built-in digital down-conversion with programmable bandwidth**
- **Real-time aggregate recording rates up to 4.0 GB/s**
- **SSD RAID storage capacity up to 30.7 TB using NTFS files**
- **SystemFlow GUI control panel for fast, intuitive operation**

The Model RTR 2727A rugged portable recorder targets applications needing to record and reproduce high-bandwidth signals. A complete PC workstation, the RTR 2727A provides high data capacity and aggregate recording rates of up to 4.0 GB/s in a four-channel system.

The RTR 2727A offers up to sixteen hot-swap solid state drives (SSDs) with a combined capacity to 30.7 TB sustained hours of continuous recording. The system features recording and playback of RF/IF signal frequencies up to 700 MHz with signal bandwidths up to 200 MHz. Available data converters include 500 MHz 12-bit A/Ds or 400 MHz 14-bit A/Ds and 800 MHz 16-bit D/As.

At the heart of the RTR 2727A are Pentek Cobalt® Virtex-6 software radio boards featuring A/D and D/A converters, digital downconverters, digital upconverters, and complementary FPGA IP cores. Optional GPS time and position stamping allows the user to record this critical signal information.

"The RTR 2727A offers nearly ten times the storage capacity of its predecessor in a 25% smaller package. Its SSDs, highly resistant to shock and vibration, and its optional DC power supply support operational environments for aircraft, ships, and vehicles," **said Rodger Hosking, vice-president of Pentek.** ***"This portable instrument is ideal for IF/RF signal recording and playback in radar, communications and other high frequency applications."***

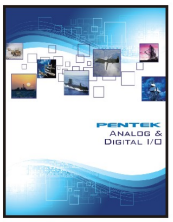
The RTR 2727A is housed in a rugged, lightweight chassis measuring only 16.0" W x 6.9" D x 13.0" H and weighing less than 30 pounds. This extremely portable workstation features 100% aluminum alloy construction, reinforced with shock-absorbing rubber corners and an impact-resistant protective glass for the high resolution 17" LCD monitor.

The hot-swappable SSD array is available in configurations from 1.9 TB to 30.7 TB and supports RAID levels 0, 1, 5, or 6. The SSDs are meticulously qualified by Pentek for optimum use in rugged and portable applications. By using hot swappable solid-state drives, the recorders exhibit high immunity to shock and vibration for ground vehicles, ships and aircraft.

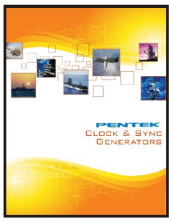
For more information, go to http://www.pentek.com/go/pipe2727A. ❐

TALON
RTR RUGGED
RECORDER

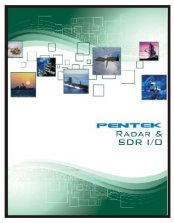
Product Catalogs You Can Download



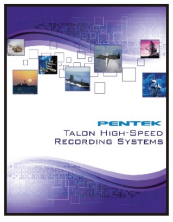
Analog & Digital I/O



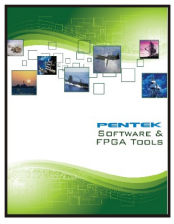
Clock & Sync Generators



Radar & SDR I/O



High-Speed Recorders



Software & FPGA Tools

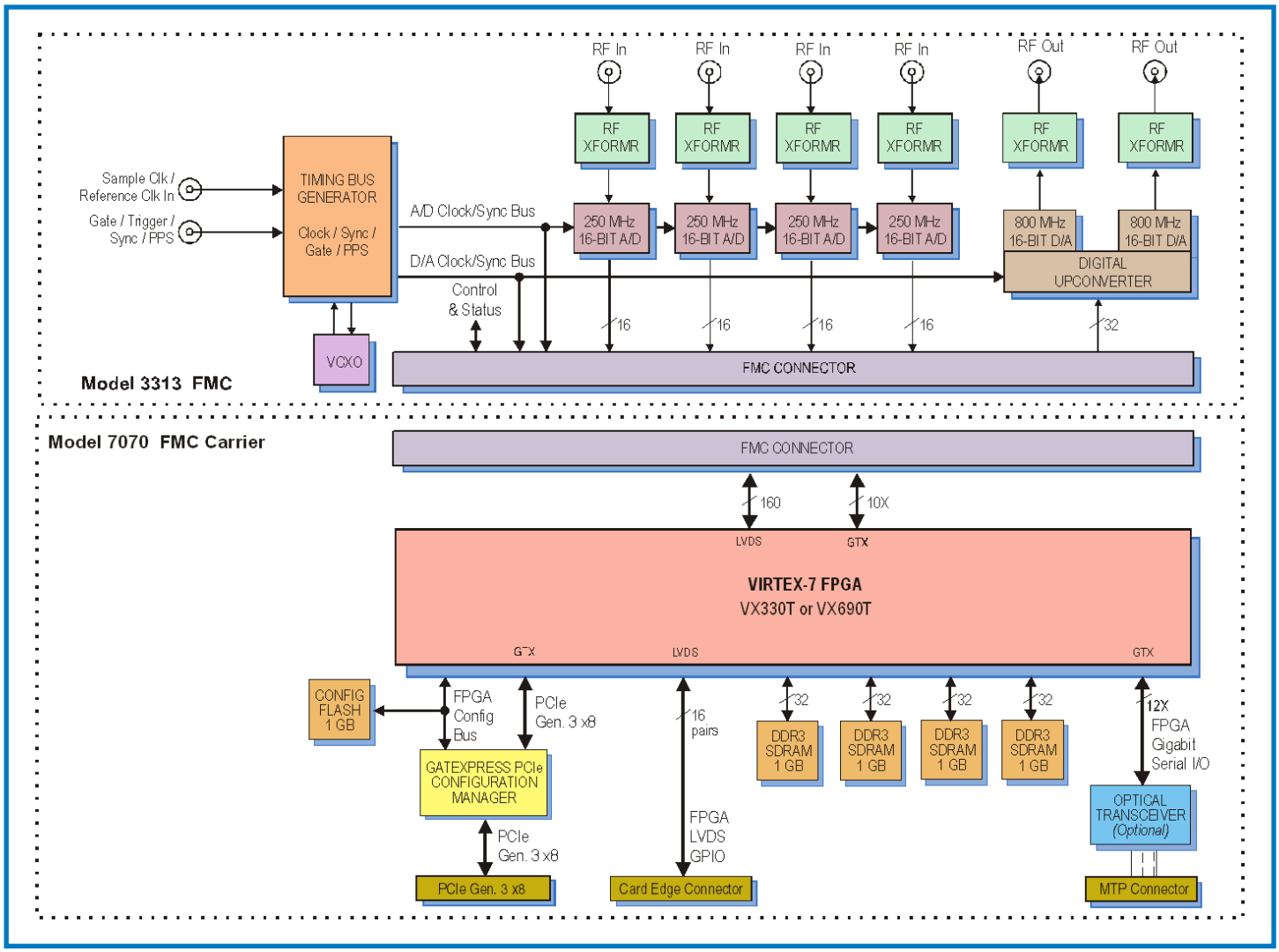
Two New FlexorSet® FMC Multichannel, High-Speed A/D & D/A Modules: Models 5973-313 (3U VPX) and 7070-313 (PCIe)

- **Four 250 MHz 16-bit A/Ds and two 800 MHz 16-bit D/As**
- **Complete transceiver for 100 MHz signal bandwidths**
- **FPGA-based digital downconverters (DDCs) and digital upconverters (DUCs)**
- **3U VPX and PCIe form factors with Virtex-7 FPGA**
- **Fully turn-key for immediate operation out-of-the-box**

The FlexorSet® Model 5973-313 for 3U VPX and Model 7070-313 for PCIe platforms consist of an FMC installed on either of two Flexor FMC carriers with Virtex-7 FPGAs. The Flexor Model 3312 FMC features four 250 MHz, 16-bit A/Ds and two 800 MHz, 16-bit D/As, which are supported with matching digital down converters and interpolation filters as intellectual property (IP) installed in the FPGA.

"These FlexorSet combinations include the most commonly required IP functions for data acquisition and signal generation applications," said Rodger Hosking, vice-president of Pentek. ***"Because of these pre-configured functions and supporting software, our customers can start capturing and generating signals within minutes after opening the box."***

Each FlexorSet is a multichannel, high-speed data converter sub-system with ➢



a highly programmable analog I/O signal interface suitable for connection to HF or IF ports of a communications or radar system, and supporting signal bandwidths up to 100 MHz. The built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each includes four 250 MHz, 16-bit A/Ds using two Texas Instruments ADS42LB69s. A single Texas Instruments DAC5688 provides a digital upconverter and two 800 MHz, 16-bit D/As. Four banks of DDR3 SDRAM provide a generous 4 GB of storage for data processing. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-313 and Model 7070-313 include optional copper and optical gigabit serial connections to the Virtex-7 FPGA for custom I/O.

"The FlexorSet concept saves us a tremendous amount of time in setting up our recording systems for customers," stated Chris Tojeira, director of Pentek's Talon Recording Solutions. ***"We can integrate these into our recorders straight out-of-the-box and immediately start to capture signals, saving us a tremendous amount of development time and getting us to deployment much faster."***

Bundling for Seamless Integration

Both FlexorSets come pre-configured with a suite of built-in functions for data capture, synchronization, time tagging and formatting, all tailored and optimized for the FMC and carrier. This IP enables high performance capture and delivery of data to provide an ideal turn-key signal interface for radar, communications or general data acquisition applications, eliminating the integration effort typically left for the user when integrating the FMC and carrier.

Development Tools and Software Support

FlexorSets provide a development and deployment platform for custom IP: Pentek's GateFlow® FPGA design kit. GateFlow gives users access to the factory-installed IP at the source level, allowing them to extend or even replace the built-in functions.

Pentek's GateXpress® PCIe configuration manager supports dynamic FPGA reconfiguration though software commands as part of the runtime application. This provides an efficient way to reload the FPGA, which reduces development time during testing. For deployed environments, GateXpress enables reloading the FPGA without the need to reset the host system, ideal for applications that require dynamic access to multiple processing IP algorithms.

Pentek's ReadyFlow® Board Support Package is available for Windows and Linux. The ReadyFlow C-callable library contains a suite of initialization, control and status functions, as well as a set of pre-compiled examples to accelerate application development.

For more information, go to http://www.pentek.com/go/5973-313 or http://www.pentek.com/go/7070-313 . ❐

SPARK Development Systems

Spark Rapid Development with a SPARK Development System!

Whether you are interested in using a Jade, Flexor, Onyx, or Cobalt product, a SPARK system can get you off to a fast start.

The SPARK Development Systems are fully-integrated platforms for Pentek boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

For more information, go to http://www.pentek.com/go/pipeSPARK.