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The Pentek Pipeline

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A quarterly publication for engineering system design and applications.

In This Issue

- Designers battle the challenges posed by the harsh environments in which mil-aero software boards must operate. More in the feature article.

"While thorough product testing is essential, the integrity and reliability of any system must be designed in from the beginning using guidance and practices best gained through experience."

Rodger Hosking, Pentek Vice President and Co-founder

- **Product Focus:** Talon RTR 2736A
- **Product Focus:** Flexor Model 7070

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- Sign up for a free subscription to The Pentek Pipeline
- Sign up for Virtex-7 Onyx product update
- *Updated* edition of the *High-Speed Recording Systems Handbook*
- *Updated* edition of the *High-Speed Switched Serial Fabrics Handbook*
- *Updated* edition of the *SDR Handbook*
- *Updated* edition of the *FPGAs for Software Radio Systems Handbook*

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Board-Level Design Challenges for Military Software Radios

Designers of mil-aero software radio boards must ensure outstanding signal quality and reliability across a diverse range of harsh operating environments. Size constraints and high component density require clever solutions for thermal management, shielding, filtering, noise reduction, power dissipation, and mechanical layout. Designers deal with these challenges using strategies developed only by tackling each issue, often through trial and error.

Wideband Data Conversion

Modern radar and communication systems use wideband signals for improved range, resolution, and information content. Since virtually all of these systems now exploit DSP for maximum performance, the radio signals must first be digitized using high-speed A/D converters. Capable of operating at sampling rates of 5 GHz and above, they can deliver a single stream representing up to 2 GHz of bandwidth, avoiding the cumbersome band-splitting strategies previously required.

Unlike pure analog RF circuitry, which can be shielded in metal compartments, A/D converters present an existential confluence of analog and digital domains. Clock and data lines of an A/D can radiate spurious signals that contaminate its analog input, thereby reducing dynamic range and limiting system performance.

High-power digital circuits like FPGAs act as powerful RF transmitters, broadcasting energy through thousands of I/O pins. On-board switching power supplies, delivering up to 30 amps of current, operate at frequencies well within the input signal band. Making matters worse, small embedded system modules like XMCs must be densely populated, forcing close proximity of data converters, FPGAs, memories, power converters, and data buffers.

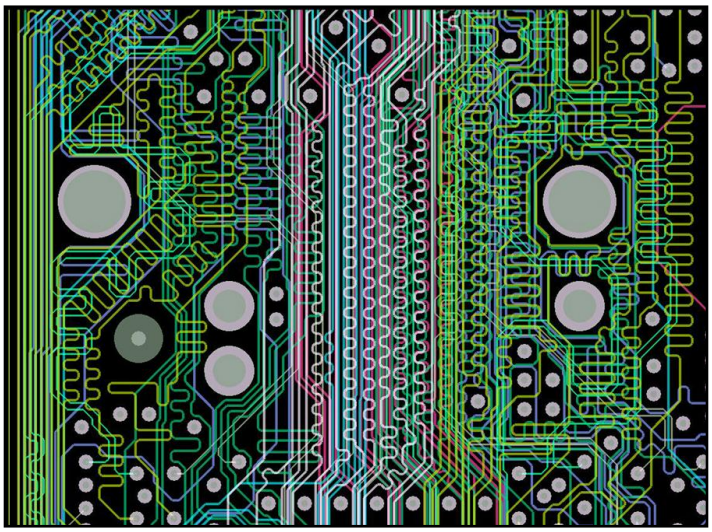


Figure 1. *Length matching between circuit board traces of gigabit serial links requires extra loops and curves to ensure simultaneous arrival at the receivers.*

Maintaining analog signal purity requires extreme care in component placement, signal routing, shielding, isolation, as well as scrupulous power supply regulation, bypassing and filtering. Power and ground

Board-Level Design Challenges for Military Software Radio (continued)

planes are perforated by thousands of vias, thus compromising their integrity and effectiveness. Fully automated routing often yields a trace pattern that makes the right connections but fatally corrupts critical analog signals.

A successful strategy usually requires human component placement and manual analog signal layout, followed by carefully guided semi-automatic routing of the digital signals. The final design requires inspection of each layer by an experienced engineer. Even so, hidden problems may not be resolved without two or more cycles of revisions and testing of the finished product.

High-Speed Data Links

During the last five years, software radio components have shifted heavily from parallel buses to multi-gigabit serial interconnections. Unlike traditional parallel bus backplanes, virtually all new embedded systems use serial links between boards and modules as evidenced by the shift from VMEbus to VPX.

The parallel LVDS data lines of data converter devices are also now being replaced by JESD204B serial links, taking full advantage of the rich complement of serial interfaces on the latest FPGAs and ASICs. This reduces power dissipation, offers scalability to higher rates, and dramatically drops the number of wires between devices by a factor of 8 or more. Operating at serial rates of 3.125, 6.25 and 12.5 Gbits/sec, JESD204B also supports lane bonding so that multiple serial lines can be aggregated to boost transfer rates.

Traditional DDR memories with parallel address and data buses are making way for a radically new memory called the Hybrid Memory Cube (HMC). It uses serial packets for reading and writing into vertical regions of stacked memory planes. Each packet contains a header with address and control information along with space for payload data. Featuring up to four access ports, each HMC holds up to 8 GB of data and supports read/write bandwidths as high as 320 GB/sec.

Reaping the many benefits of serial links forces circuit board designers to obey more stringent layout rules. Each serial lane uses two wires as a differential pair, which must be carefully matched in length to maintain signal integrity, often to within a few mils. The routing path of the pair may curve, adding extra length to the outside trace. Automated routing tools can compensate by adding extra loops and curves to undo the length discrepancies as shown in **Figure 1**. Additionally, bonded (multiple) lane interfaces like those between an A/D and an FPGA must maintain a common length across all lanes.

Other pitfalls for serial link circuit board design are impedance discontinuities along the traces, causing degraded transmission as the serial bit rate increases. Especially problematic are vias, connectors, stubs and pads. Running serial lanes across two different ground planes must be avoided, and special attention must be paid to the dielectric characteristics of the circuit board. Even the weave pattern of the laminate can distort the co-planarity of the traces, limiting the maximum usable bit rate. These effects can be modeled to a certain extent, but often the design can be fully validated only by product testing.

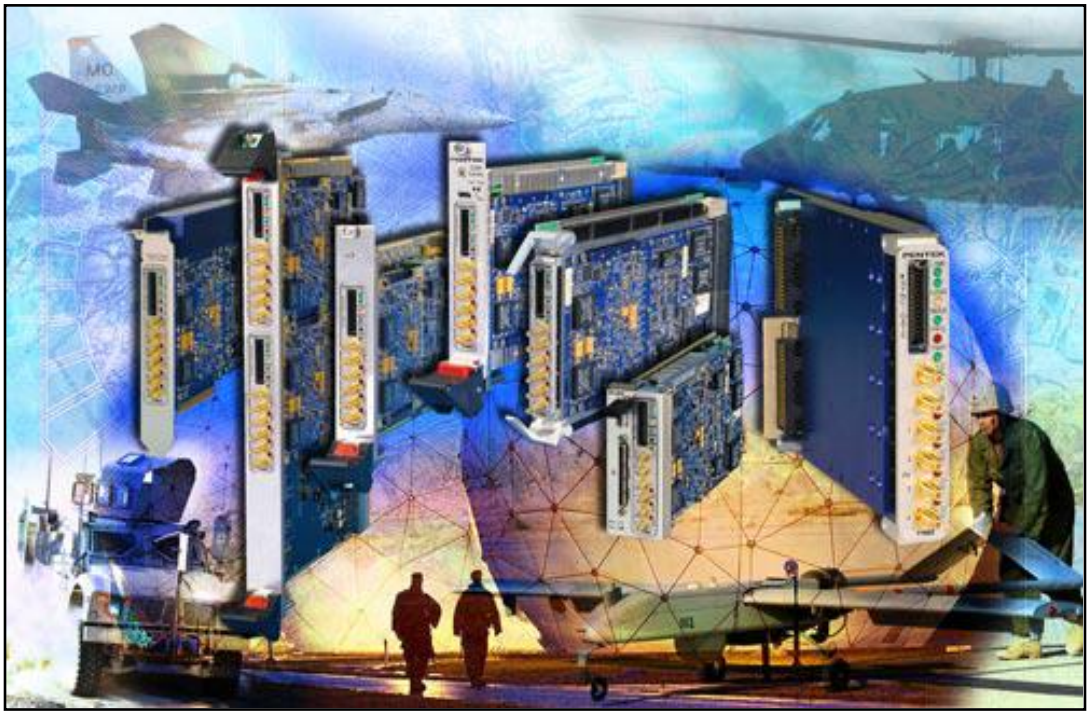


Figure 2. *Pentek products based on the Model 71663 XMC module. This four-channel, high-speed A/D converter with 1100 GSM DDCs accepts IF signals from an RF tuner. It can capture all transmit and receive signals in both upper and lower GSM bands. For more information: pentek.com/go/pipe71663*

Thermal Management

Although shrinking silicon process geometry helps reduce power dissipation for a given function, it also means more functions per package. As a result, next generation devices dissipate about the same total power as the previous generation,

Board-Level Design Challenges for Military Software Radio (continued)

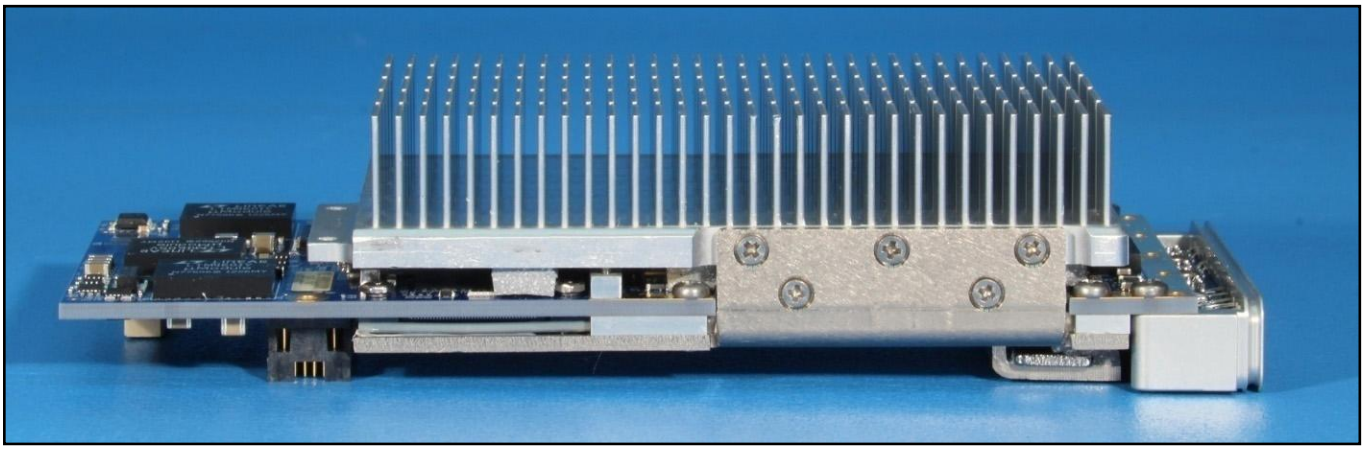


Figure 3. *An air-cooled XMC module uses a highly-effective nickel-plated copper band to pull heat from a large FPGA on the underside of the board into an aluminum finned heat sink sitting in the airflow.*

and removing this heat is a critical part of any system design. Some board vendors merely place components on a circuit board, and leave the thermal management task to their customers as part of system integration. This approach often requires expensive last-minute remedies that usually increase development costs and extend delivery times.

Conduction cooling techniques were first developed for older device packaging with through-hole pins that transferred heat to internal copper planes of the circuit board. Compression clamps along the edges of the board drew heat into metal card guide channels of the chassis.

Today, virtually all high power devices use ball grid array packaging, where most of the heat is delivered to the top surface of the package, exactly opposite of those early components. Now, the most popular strategy is a metal plate extending across the board, making thermal contact with all of the lids of hot devices, and bringing the heat to the metal side channels with clamps along the edges. Unfortunately, these metal plates must accommodate a wide variety of components, each with different heights and shapes. This mandates a custom plate uniquely milled with recesses for each device. To ensure good thermal transfer, conductive compound heat pads are installed on top of each device, conforming to fill the recess in the plate.

Forced air cooling is often more challenging due the number of variables. PC-based systems present an infinite combination of PCIe slot positions, fan types and placement, ventilation hole patterns, drive bay location, and power supply configuration. When necessary, creative heat sink designs can pull heat from high-power components like FPGAs around to the opposite side of the board where fins can engage with much more effective airflow, as shown in **Figure 3**. Fortunately, military radios usually use open architecture chassis like VME, VPX, CompactPCI, or MicroTCA, all of which offer more dependable airflow streams.

Attaching a mezzanine module to a carrier board presents yet a different problem. For example, most XMC modules have FPGAs on the same surface that faces the component side of a SBC carrier board, often sporting large processors. Not only are two high-power devices now radiating heat into each other, but the air space between the boards is greatly reduced. Often the best solution is a custom metal plate between the XMC module and carrier board that conforms to the top lids of hot devices on both boards. This alone is extremely effective for conduction-cooled systems. For air-cooled systems, the metal plate can also incorporate fins around the sides of the XMC module to access suitable airflow.

Responsible board vendors include temperature sensors at critical points around the board to help evaluate the effectiveness of thermal management strategies for each type of chassis. Thresholds can be set to automatically generate an interrupt to the host CPU for out-of-limit conditions. This facility can be incorporated in the operational software to serve as a useful health monitoring facility for deployed systems.

The Whole Package

Other requirements like shock, vibration, altitude, humidity, EMI radiation and susceptibility, and environmental threats like salt, sand, and dust may require extreme measures, depending on the limits. If even only one of these factors is not properly addressed, the radio system can fail, possibly jeopardizing a mission or even the war fighter himself. While thorough product testing is essential, the integrity and reliability of any system must be designed in from the beginning, using guidance and practices best gained through experience. ❐

Product Focus

Talon® RTR 2736A

Talon Serial FPDP Rugged Portable Recorder

Features

- Designed to operate under conditions of shock and vibration
- Portable system measures 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Shock-and-vibration-resistant SSDs perform well in vehicles, ships, and aircraft
- Up to eight I/O channels
- Supports Flow Control, CRC, and Copy/Loop mode as a receiver and transmitter
- Supports 1.0625, 2.125, 2.5, 3.125, and 4.25 GBaud link rates
- Copper, single-mode and multi-mode fiber interfaces available
- Real-time aggregate recording rates up to 3.2 GB/sec

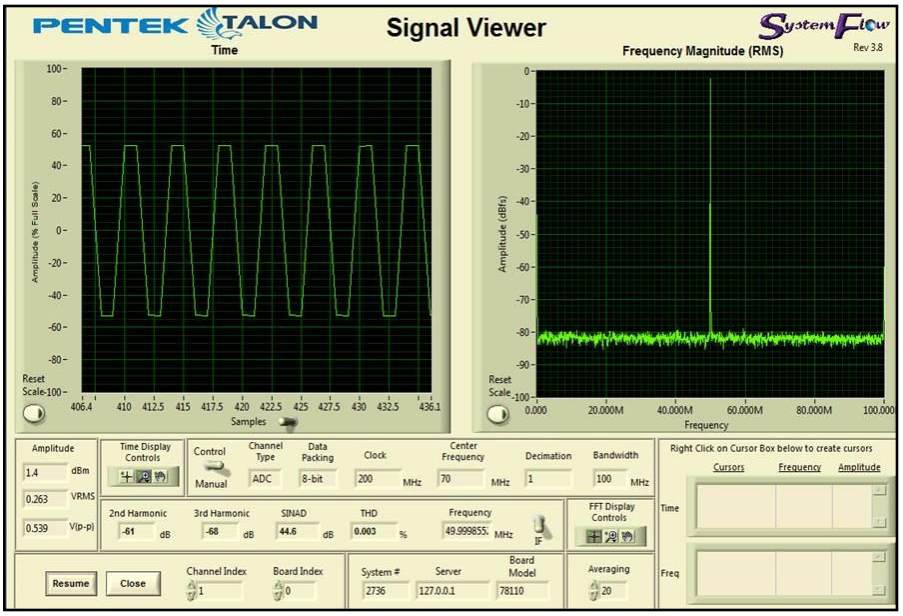
The new portable Talon® RTR 2736A can record and play back multiple serial FPDP data streams. The new Talon portable chassis boasts a smaller footprint that is lighter in weight, and provides double the storage capacity, number of channels and the recording rates of the previous generation of Talon portable recorders. It also supports AC and DC power options.

The RTR 2736A is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.2 GB/sec.

The RTR 2736A can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multimode fiber, to accommodate all popular serial FPDP interfaces. It can both receive and transmit data over these links and supports real-time data storage to disk.

TALON RTR RUGGED RECORDER

"Our first generation of sFPDP recorders has been a big hit with our customers. We're excited to provide a portable system with twice the storage capacity and speed of the previous generation," said Chris Tojeira, Recording Systems Director for Pentek. "By using the standard NTFS file system, our customers enjoy instant access to recorded files. This saves hours of file conversion required in competing recorders," he added.



Rugged Chassis

The RTR 2736A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 15.3 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 1, 5, and 6, provide a choice for the required level of redundancy.

SystemFlow Software

The RTR 2736A includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing users to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal before, during, and after a recording session. These tools include a virtual oscilloscope and a spectrum analyzer. For more information, go to: pentek.com/go/pipe2736A ❐

Product Focus

Flexor® Model 7070

Flexor Virtex-7 Processor and FMC Carrier - PCIe

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGA
- GateXpress supports dynamic FPGA recognition across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2, and 3) interface up to x8
- Optional user-configurable 12X optical gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Commercial and extended-temperature versions available

The new Flexor® Model 7070 is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF, or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

Board Architecture

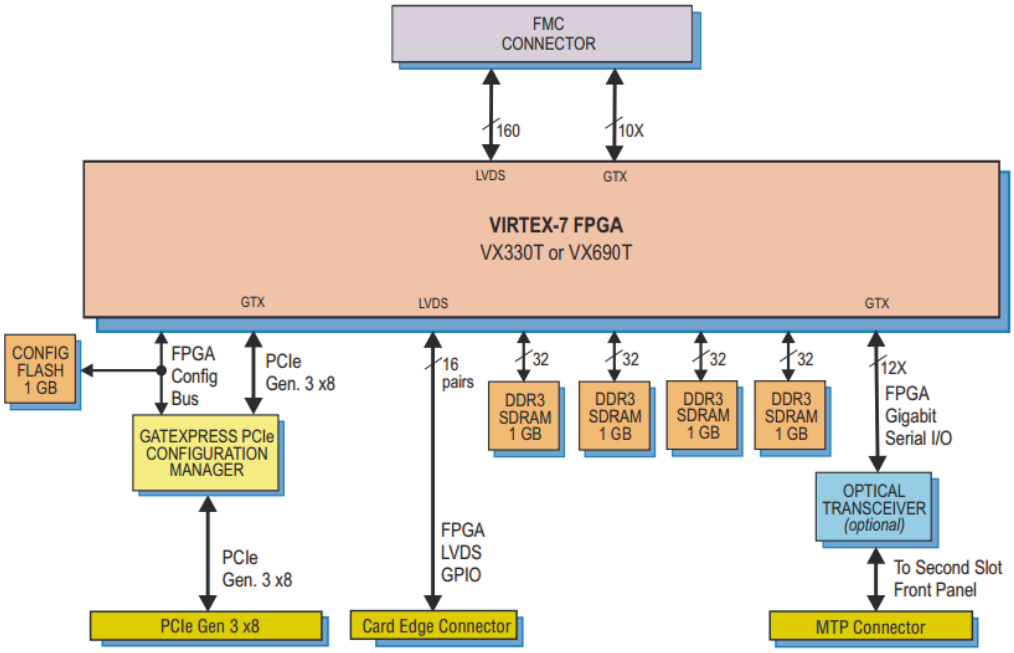
Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 retains all of the key features of that family. As a foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC module, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing, and sample - count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070 and installed FMC to operate as a complete solution without the need to develop any FPGA IP.



Model 7070 - Flexor Virtex-7 Processor and FMC Carrier - PCIe (continued)

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

The 7070 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/ decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and a card edge connector for custom I/O. For applications requiring custom gigabit links, up to 12 high-speed, full-duplex FPGA GTH lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on a PCIe slot panel that can be installed in an empty, adjacent PCIe slot. When configured with a VX330T FPGA, four duplex lanes are available.

The 7070 architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

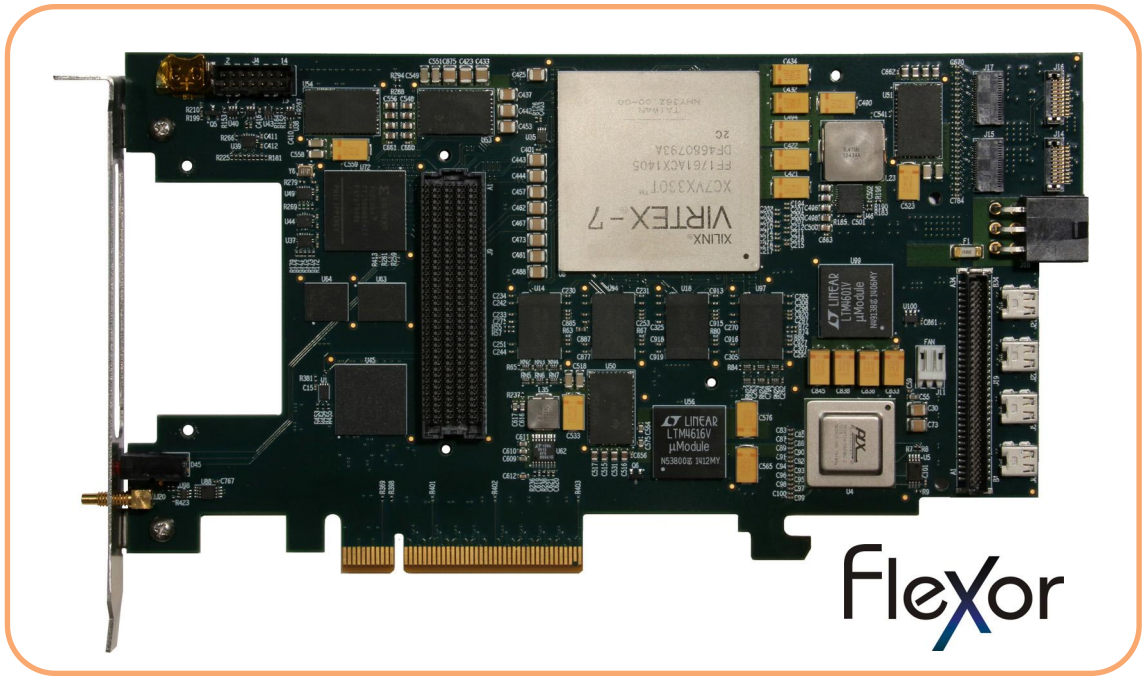
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power- up, the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation, simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.



For more information, go to: pentek.com/go/pipe7070 ❐

Test Drive Pentek's Talon Recording Systems

with the Free SystemFlow Simulator

SystemFlow

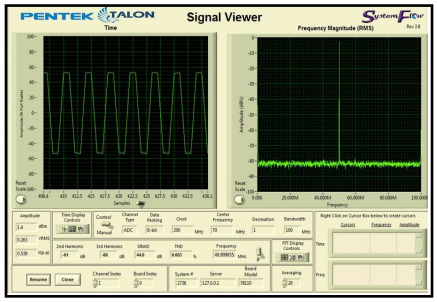
The SystemFlow Simulator

The SystemFlow® Simulator demonstrates the Configuration, Record, Playback, and Status screens to show the intuitive controls and indicators of the recorder. It also includes the SystemFlow Signal Viewer which displays simulated live signals being digitized and recorded by a Pentek analog signal recorder. The SystemFlow Signal Viewer includes a virtual oscilloscope and a virtual spectrum analyzer for signal monitoring in both the time and frequency domains.

SystemFlow API

The virtual server provides live, interactive operation for training or development. The user can easily switch between different recording systems in the Talon recording system product line. The intuitive user interface and API provide a simple transition from one Talon recorder to another.

- Live, interactive Talon recording system simulation
- SystemFlow API for developing and testing custom user interfaces
- Evaluation and training tool.



Pentek's SystemFlow Simulator for Talon analog and digital recording systems includes a virtual recorder server application that simulates disk and I/O transactions for a complete and realistic recording environment.

FREE Talon SystemFlow Simulator Download Now!

Develop a Custom User Interface

Developers can use the SystemFlow API as a tool for developing their own UI to control the Talon recording system prior to delivery, saving valuable development time.

Remote Control Made Easy

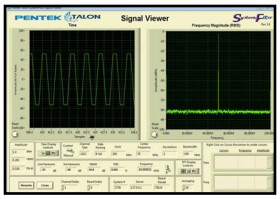
The socket-based client-server architecture allows system engineers to get a head-start for the setup and test of the remote control of their Talon recording system.

Develop a Custom User Interface

With the SystemFlow Simulator, users can create system profiles containing all parameters and operational modes for easy recall in future recording sessions. All this, before ordering their recorder!

Video Spotlight

View SystemFlow Software for Talon Recorders



Topics include: API, GUI, Signal Viewer and Analyzer, and the NTFS file system

Start Application Development Today!

Model 8266 PC Development System for PCIe Onyx and Cobalt Boards

The Model 8266 resolves the typical hardware and software compatibility obstacles inherent in new PC development platforms. All hardware is installed in appropriate slots with proper cabling, power, and cooling strategies, and optimized BIOs. For more information: pentek.com/go/pipe8266

Video Spotlight

The Latest Design Strategies using Xilinx Virtex-7 for Software Radio

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Analog & Digital I/O


Clock & Sync Generators


Radar & SDR I/O


Processors


Software & FPGA Tools


High-Speed Recorders