Model 78861	4-Channel 200 MHz A/D with DDC	Kintex UltraScale FPGA	x8 PCIe Board

Features

- Exceptional dynamic range and analog signal integrity
- Xilinx® Kintex® UltraScale™ FPGA
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (Digital Downconverters)
- 5 GB of 2400 MHz DDR4 SDRAM
- Sample clock synchronization to an an external reference
- Programmable frequency synthesized sample clock generator
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Powerful DMA controllers for moving data
- Multichannel, multiboard synchronization with clock/sync bus
- Optional clock/sync generator for multiboard systems
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- SPARK® fully-integrated development system
- Free lifetime applications support

JADE

Applications

- Complete radar and software radio interface solution
- Communication receiver
- Radar receiver
- Analog signal interface for digital recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The Jade Architecture

Evolved from the proven designs of Pentek's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78861 factory installed functions include four A/D acquisition modules for simplifying data capture and tagging, and a set of specialized DMA engines for efficient data transfers between the board and a host computer.

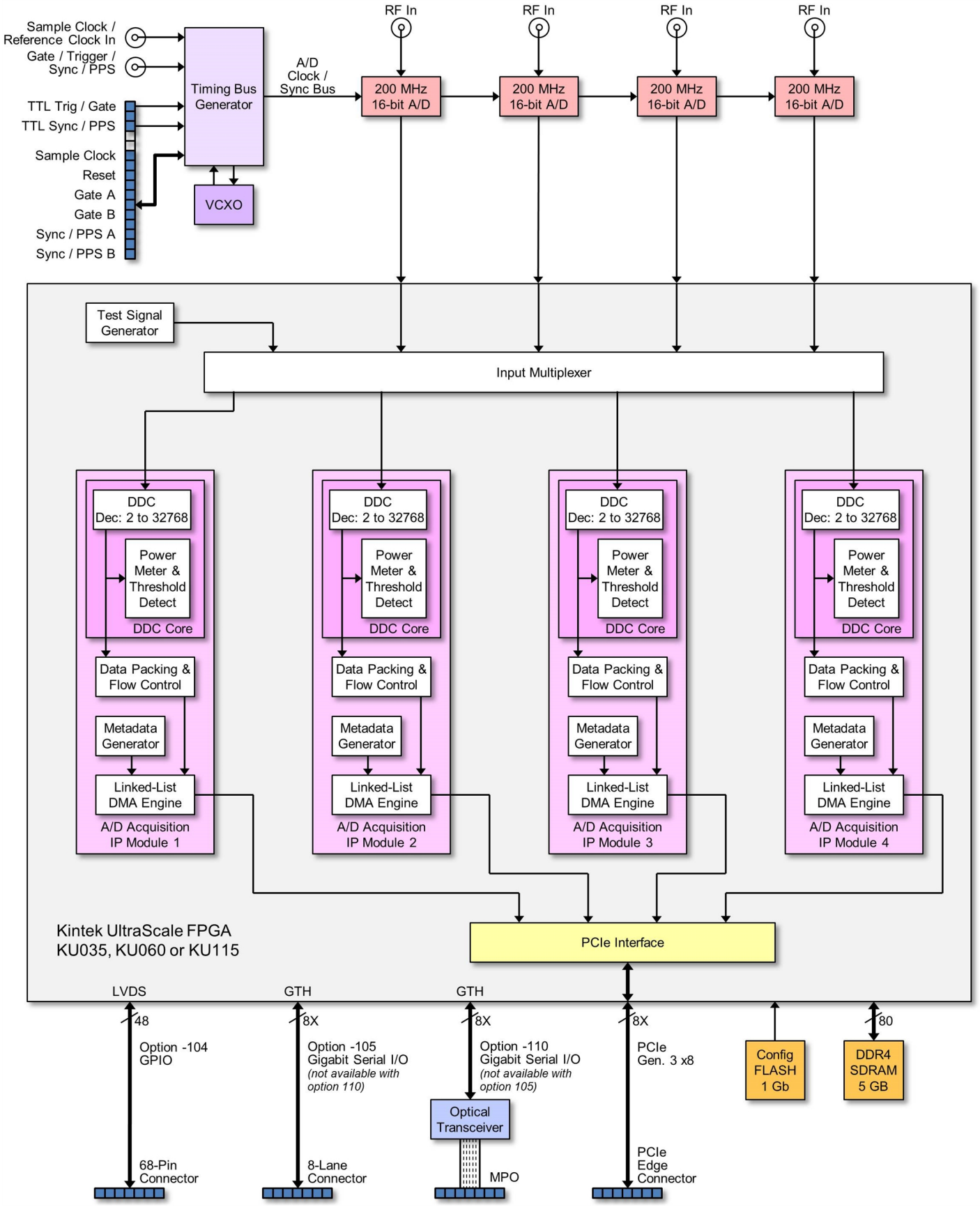
Additional IP includes: four powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory control; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These factory-installed applications enable the 78861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Xilinx Kintex UltraScale FPGAs

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

78861 Block Diagram

Click on a block for more information.



A/D Converter Stage

The board's analog interface accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

A/D Acquisition IP Modules

The 78861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

For systems requiring high-channel counts, Model 7893 System Synchronization and Distribution board can synchronize up to eight 78861s.

Memory Resources

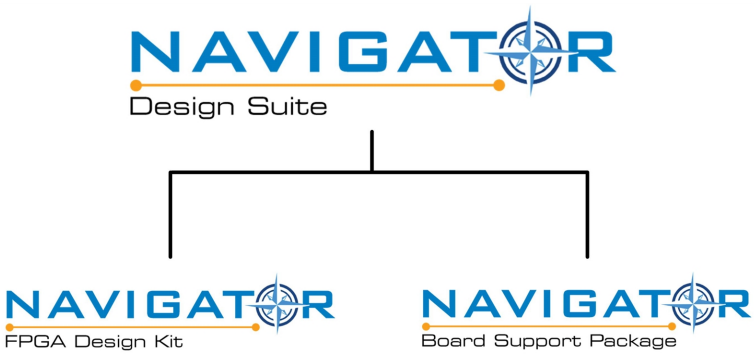
The 78861 architecture includes a 5 GB bank of DDR4 SDRAM memory. This resource is used by the board's built-in functions for data storage and buffering, but can also be used for custom applications. The Navigator FDK provides a memory controller as well as guidance on the most efficient use of the memory when creating IP functions.

PCI Express Interface

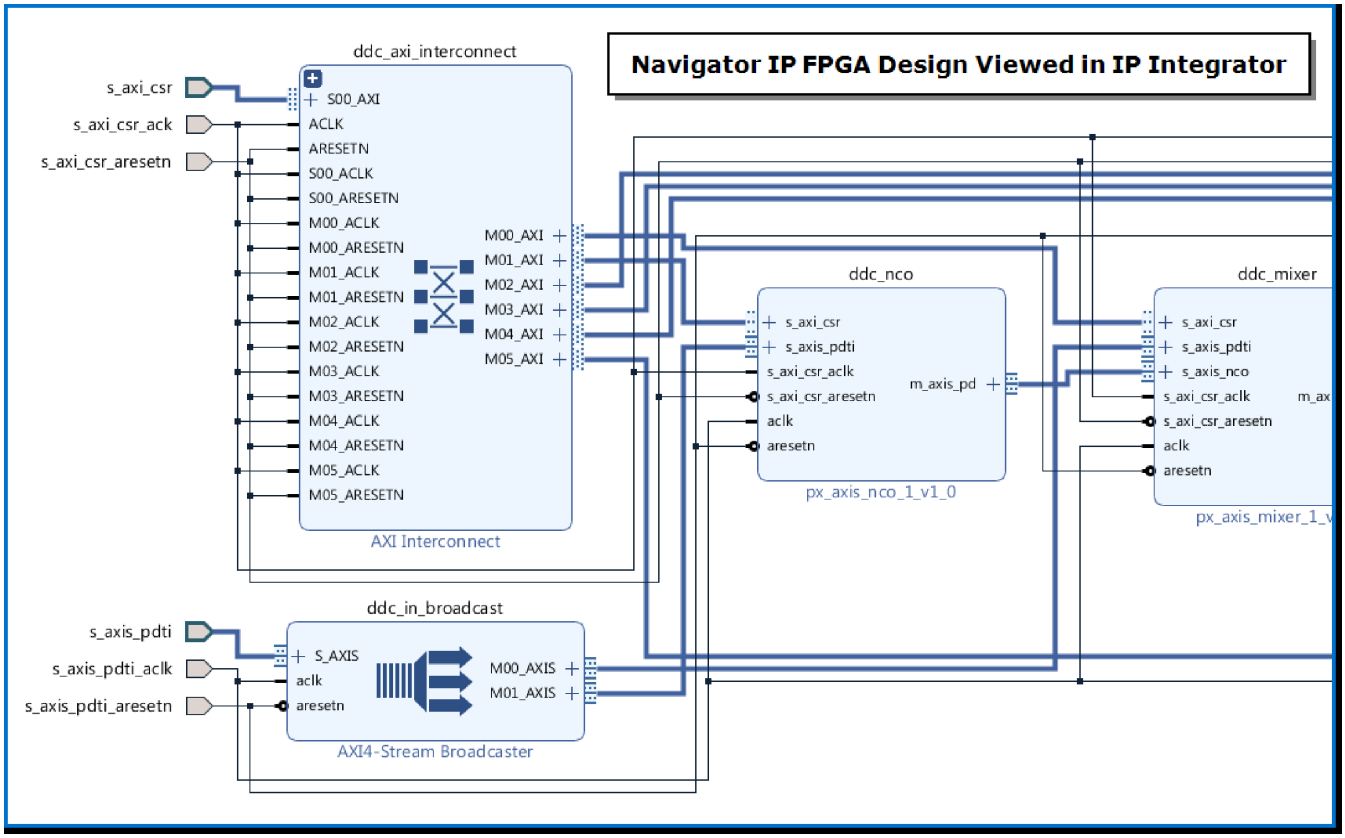
The 78861 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Navigator Design Suite

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

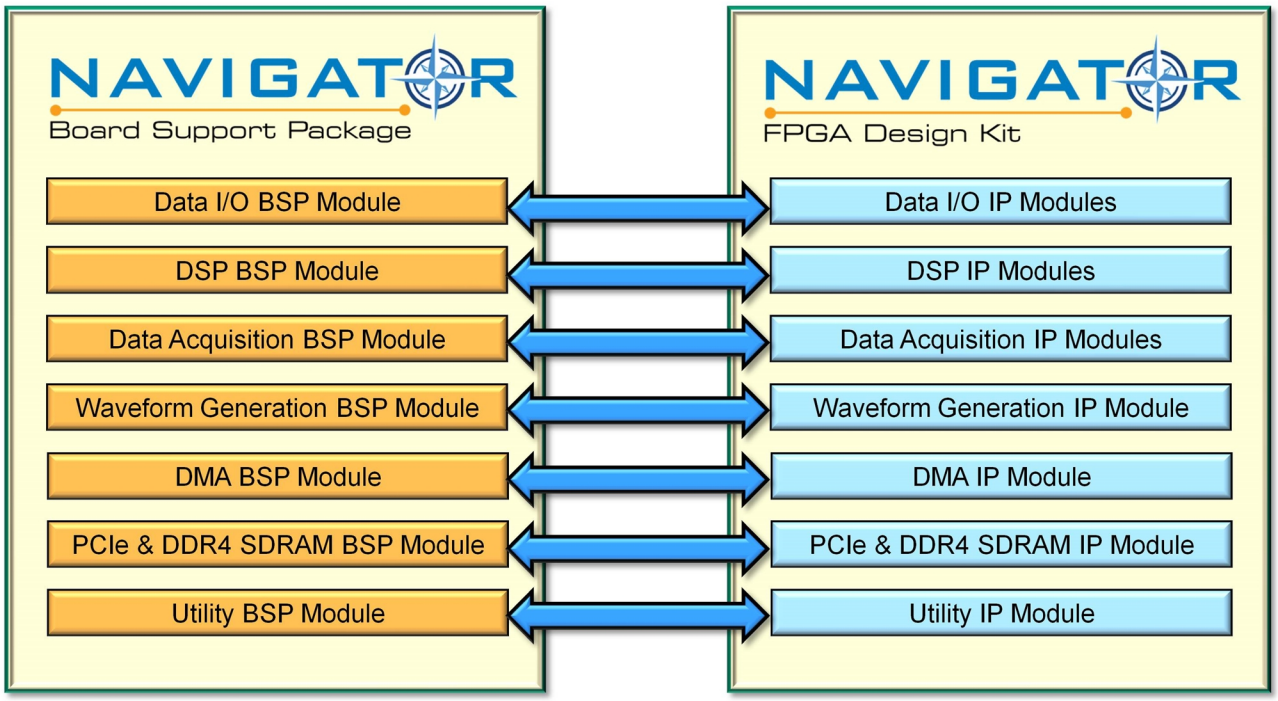


The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.



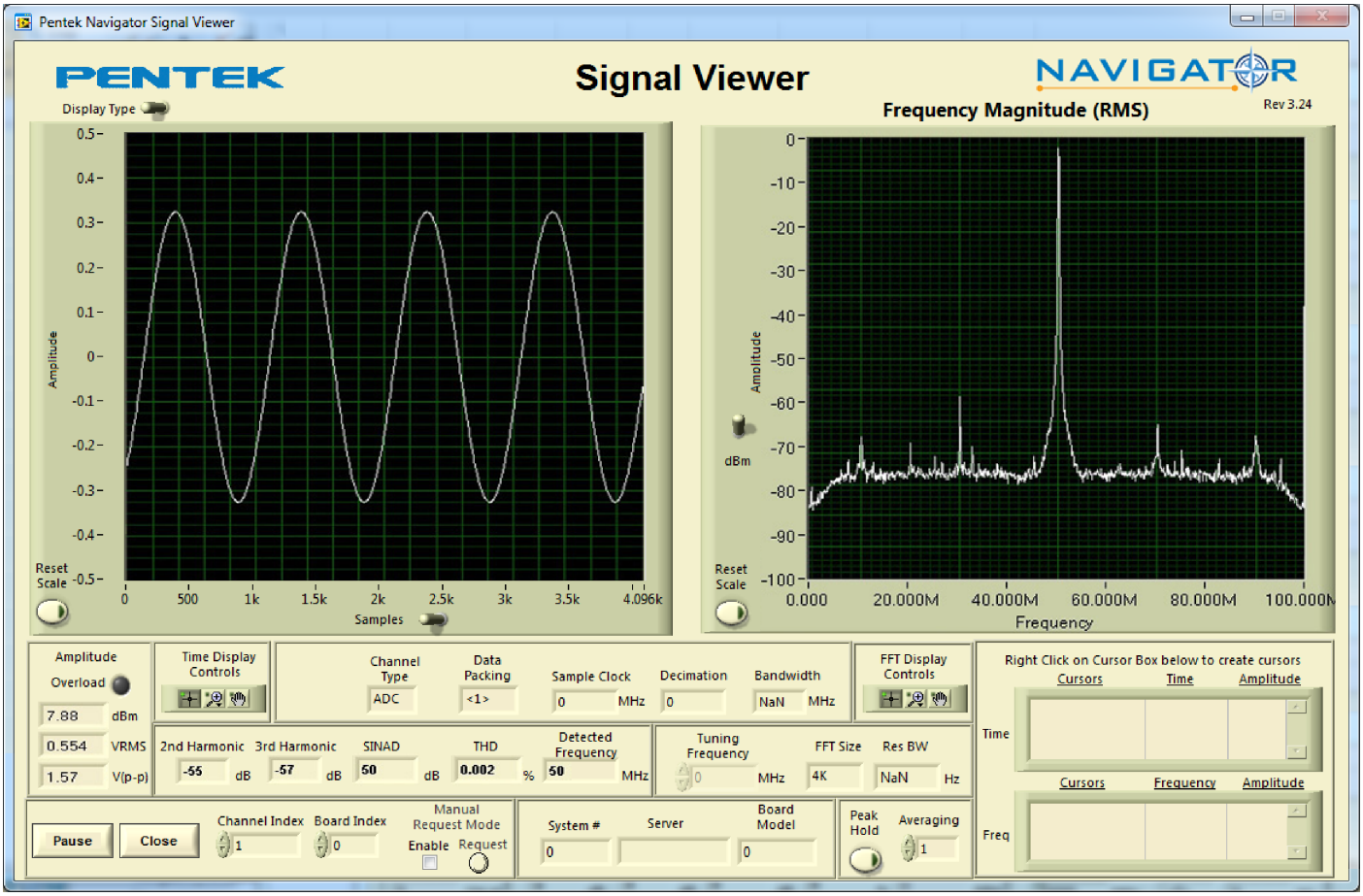
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



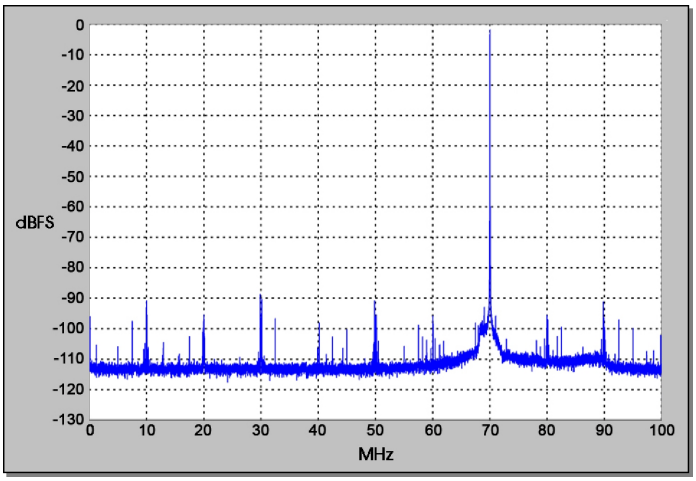
Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



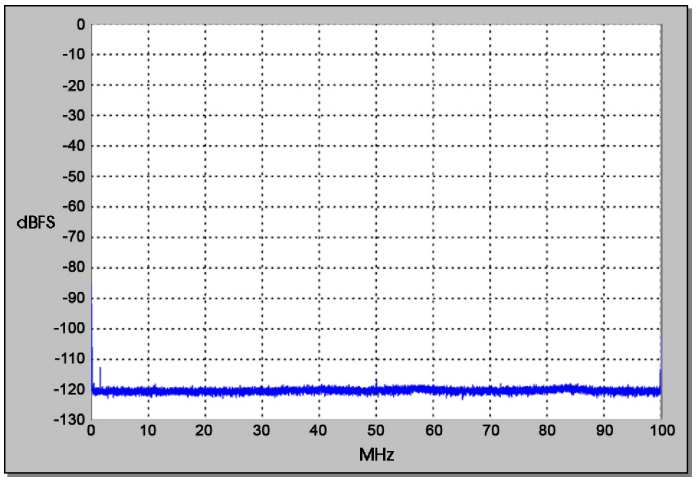
A/D Performance

Spurious Free Dynamic Range



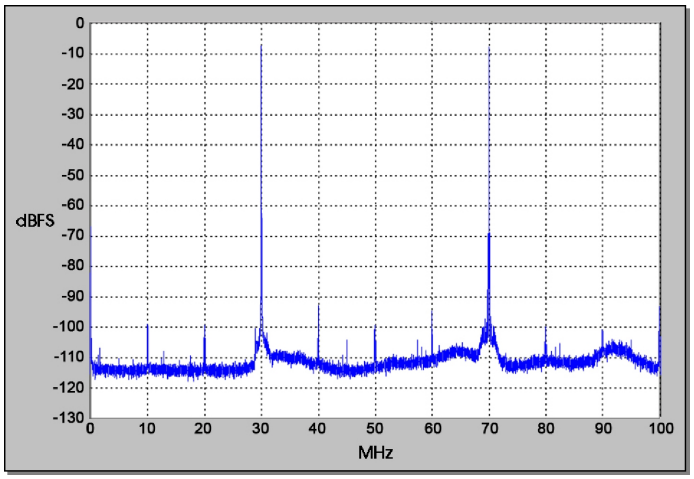
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



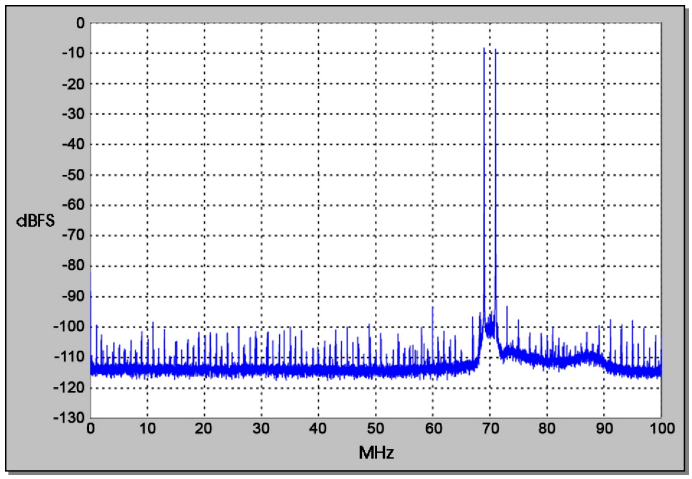
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



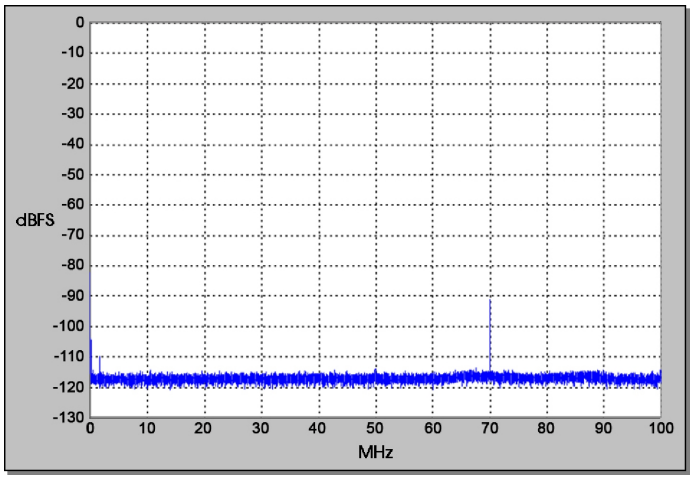
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



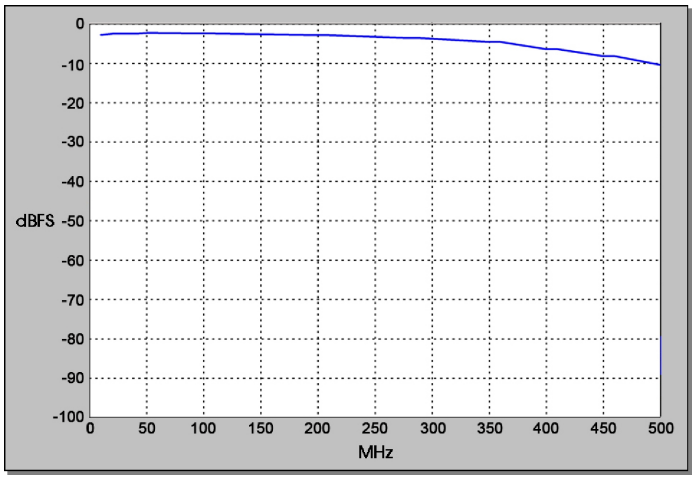
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk



f_{in} Ch2 = 70 MHz, f_s = 200 MHz, Ch 1 shown

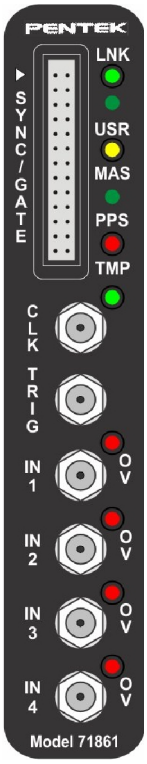
Input Frequency Response



f_s = 200 MHz, Internal Clock

Front Panel Connections

The front panel includes six SSMC coaxial connectors for clock, trigger, and analog input signals, and a 26-pin Sync Bus input/output connector. The front panel also includes ten LED indicators.



- **Sync Bus Connector:** The 26-pin µSync front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this Model 71861 is the Sync Bus Master. When only a single 71861 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the Model 71861 PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Input Connectors:** Four SSMC coaxial connectors, labeled **IN 1**, **IN 2**, **IN 3**, and **IN 4**: one for each ADS5485 input channel.
- **A/D Overload LEDs:** There are four red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5485, or an A/D FIFO overrun.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Four channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_S
LO SFDR: >108 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources

On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

26-pin connector LVPECL bus includes, clock-/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
Option -105: provides an 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory

Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air-cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: PCIe card
Depth: 181.10 mm (7.13 in)
Height: 111.25 mm (4.38 in)
Weight: Approximately 14 oz (400 grams)

Ordering Information

Model	Description
78861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through serial connector
-702	Air-cooled, Level 2

Contact Pentek for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Pentek for the latest information.

Accessory Products

Model	Description
2171	Cable Kit: SSMC to SMA
7893	System Synchronizer and Distribution Board – PCIe

SPARK Development Systems

The Pentek SPARK® systems are fully-integrated development systems for Pentek software radio, data acquisition, and I/O boards. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

The following SPARK systems are available for Pentek's Cobalt®, Onyx®, and Jade® boards: PCIe (Model 8266), 3U OpenVPX (Model 8267) and 6U OpenVPX (Model 8264). For Flexor boards, SPARK systems are available in PCIe (Model 8266) and 3U VPX (Model 8267).

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

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Lifetime Applications Support

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