New!

Models 7252, 7252D and 7352

32 or 64-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - cPCI

Model 7352 *Model 7252D*

Features

- 32 or 64-channel DDC with four or eight banks of 8 channels
- Four or eight 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths: 20 kHz to 10 MHz
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 7252 and 7352 are high-speed software radio cPCI boards. They consist of one Model 7152 Quad A/D digitizer with a factory-installed high-performance 32-channel DDC IP Core mounted on a cPCI carrier board. The Model 7252 is a 6U cPCI board, while the Model 7352 is a 3U cPCI board. Model 7252D is the same as the Model 7252, except it contains two 7152's rather than one.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

These Models employ an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 32 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

ReadyFlow Board Support Package

Decimation and Filtering

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

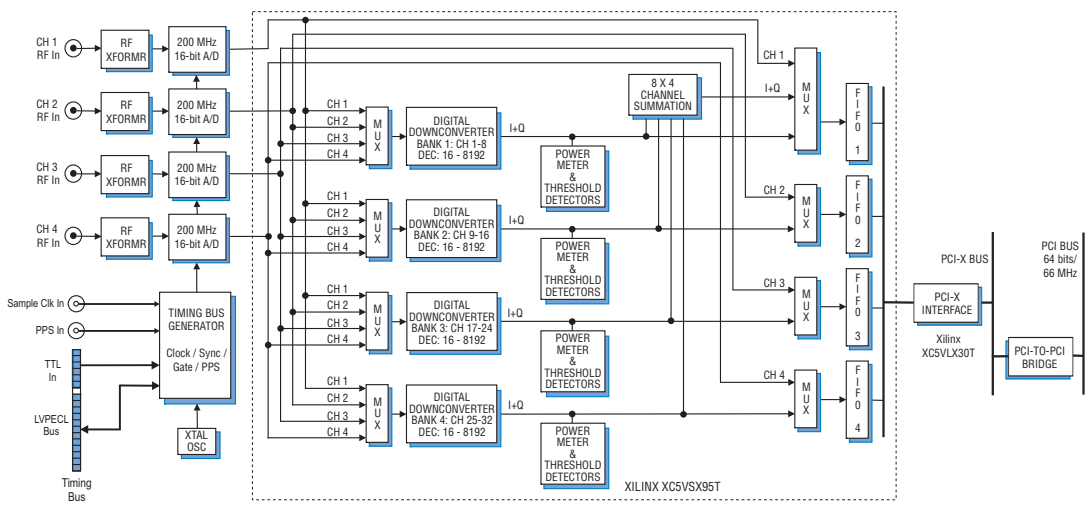
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

These models feature 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤

Model 7252 and 7352 Block Diagram Model 7252D doubles all resources except the PCI Bridge



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32 or 64-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - cPCI

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7252Ds or three slave 7352s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Interface

Both models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the boards.

Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

Specifications

Model 7252 or 7352: 4 A/Ds, 32-channel DDC
Model 7252D: 8 A/Ds, 64-channel DDC
Model 7252D shown in the Specifications

Front Panel Analog Signal Inputs (8)
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8)
Type: Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks (4)
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array (4)
- **Processing FPGA:** Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T
- **Interface FPGA:** One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface
- **PCI Bus:** 32 or 64 bits at 66 MHz and 32 or 64 bits at 33 MHz
- **DMA:** 8 channel demand-mode and chaining controller
- **Local Bus:** 64 bits at 33, 66 and 100 MHz

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7252	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 6U cPCI
7252D	64-Channel DDC with eight 200 MHz, 16-bit A/Ds - 6U cPCI
7352	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U cPCI
Options:	
-730	Two-slot heat sink

Contact Pentek for available options.

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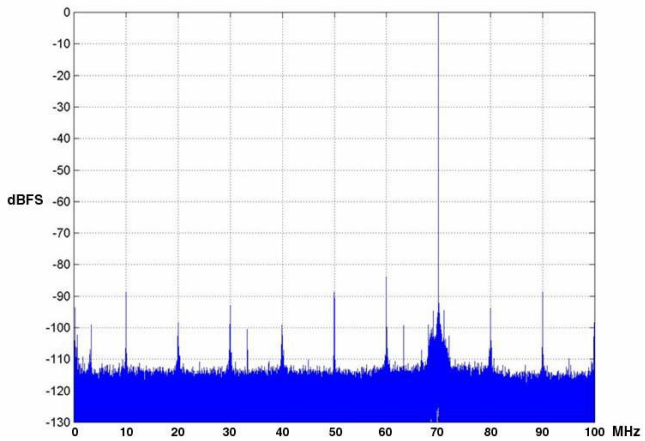
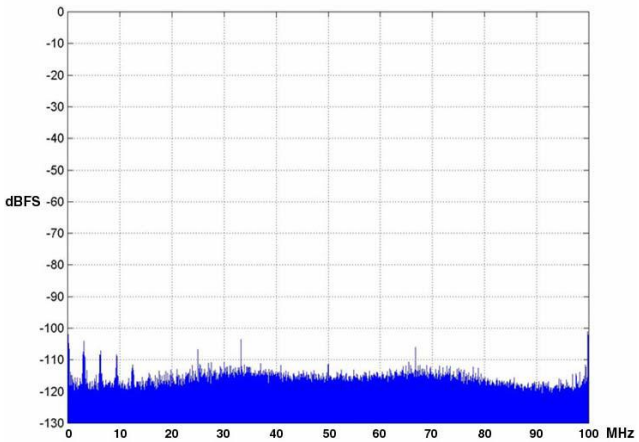
A/D Performance

Spurious-Free Dynamic Range



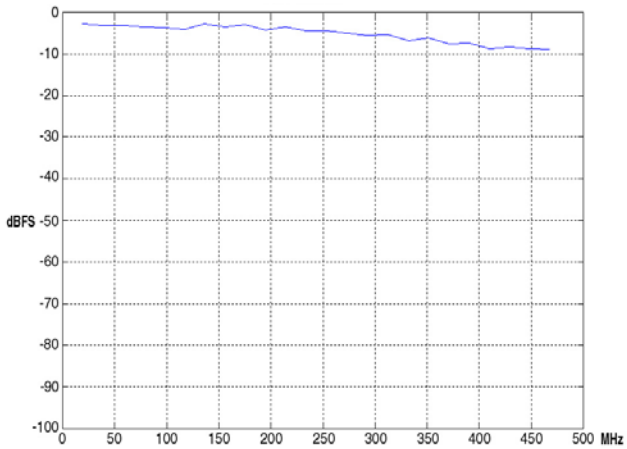
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



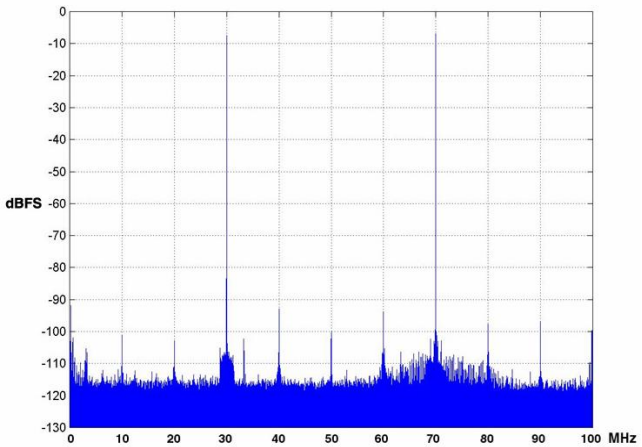
f_s= 200 MHz, Internal Clock

Input Frequency Response



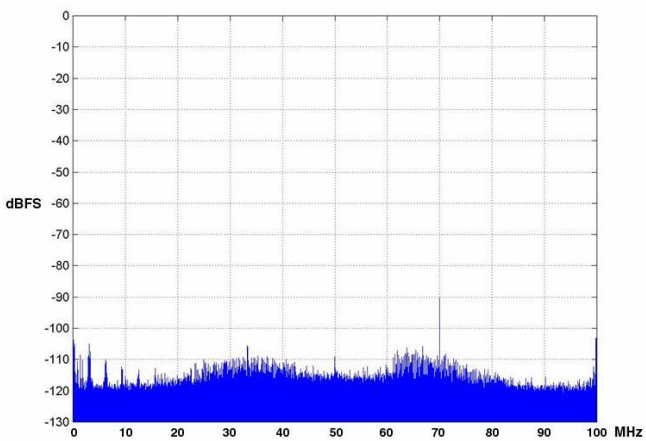
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



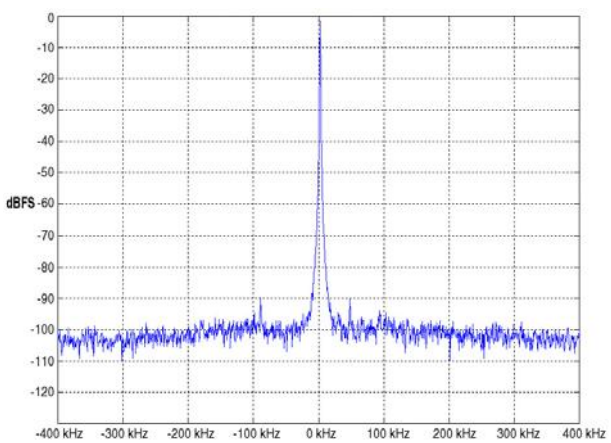
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock