New!

General Information

The JadeFX™ Model 5983 is a high-performance 3U OpenVPX board based on the Xilinx Kintex UltraScale FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5983 includes a VITA-57.4 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface Flexor® FMCs to create a FlexorSet, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4connector. With the installation of a serial protocol in the FPGA, this interface enables a high-band-width connection between 5983s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Jade family of Kintex UltraScale products, the JadeFX 5983 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions that include data

multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.
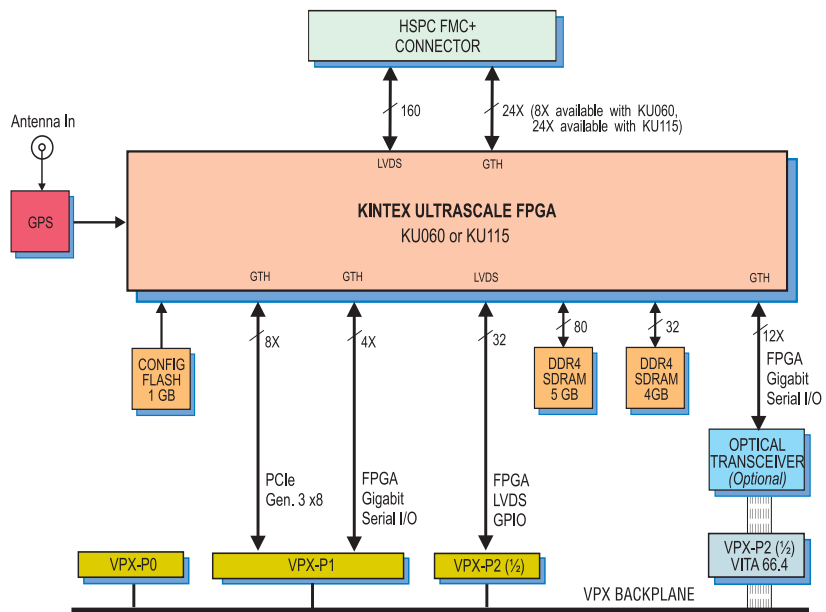
When integrated with a Pentek FMC, the 5983 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A wave-form generation engines for simplifying data capture and playback.

Data tagging and metadata packet genera-tion, in conjunction with powerful linked- list DMA engines, provide a streamlined inter-face for moving data on and off the board and identifying data packets with chan-nel timing and sample-count information.

IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchro-nization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own cus-tom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block dia-gram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core docu-mentation is included. Developers can ➤

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGAs
- 9 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Kintex UltraScale FPGA for custom I/O
- Optional optical Interface for backplane gigabit serial interboard communication
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

JADEfx

Flexor

NAVIGATOR
Design Suite

Block diagram showing the KINTEX ULTRASCALE FPGA (KU060 or KU115) connected to HSPC FMC+ CONNECTOR (160 LVDS, 24X GTH — 8X available with KU060, 24X available with KU115), GPS (Antenna In), CONFIG FLASH 1 GB, PCIe Gen. 3 x8 (8X GTH), FPGA Gigabit Serial I/O (4X GTH), FPGA LVDS GPIO (32 LVDS), DDR4 SDRAM 5 GB (80), DDR4 SDRAM 4GB (32), FPGA Gigabit Serial I/O (12X GTH), OPTICAL TRANSCEIVER (Optional), VPX-P0, VPX-P1, VPX-P2 (½), VPX-P2 (½) VITA 66.4, VPX BACKPLANE.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx, OnyxFx and JadeFX 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK
Development Systems

FlexorSet Product Combinations

If you wish to purchase this FMC Carrier in combination with an FMC module, please see:

- **FlexorSet Model 5983-313**
- **FlexorSet Model 5983-317**
- **FlexorSet Model 5983-320**
- **FlexorSet Model 5983-324**

Ordering Information

Model	Description
5983	3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Options:

-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5983 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

I/O Module Interface: VITA-57.4, High Serial Pin-Count FMC site

Field Programmable Gate Array
    Standard: Xilinx Kintex UltraScale XCKU060-2
    Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
    Serial : 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
    Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
    Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
    Type: DDR4 SDRAM
    Size: Two banks, one 4 GB and one 5 GB
    Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
    PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
    Standard: L0 (air cooled)
        Operating Temp: 0° to 50° C
        Storage Temp: –20° to 90° C
        Relative Humidity: 0 to 95%, non-condensing
    Option -702: L2 (air cooled)
        Operating Temp: –20° to 65° C
        Storage Temp: –40° to 100° C
        Relative Humidity: 0 to 95%, non-condensing
    Option -763: L3 (conduction cooled)
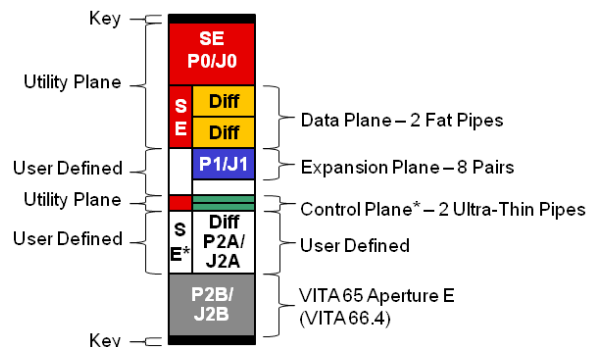   **Operating Temp:** –40° to 70° C
        Storage Temp: –50° to 100° C
        Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983 is compatibile with the following module profile, as defined by the VITA 65 OpenVPX Specification:
    SLT3-PAY-2F1F2U1E-14.6.6-1

* not connected on board