## Features

- Incorporates Xilinx® Zynq® UltraScale+™ Gen 3 RFSoC
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- LVDS connections to the RFSoC for custom I/O
- Optional VITA-66.4 optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA 66.4, VITA-57.4 and VITA-65 (OpenVPX^{TM} System Specification)
- Ruggedized and conduction-cooled versions available
- Unique QuartzXM eXpress Module enables migration to other form factors
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- 3U VPX development chassis available
- Free lifetime applications support

Applications

- High-bandwidth data streaming
- Waveform signal generator
- Multimode data acquisition system
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Remote monitoring
- Sensor interfaces

Strategies for Deploying Xilinx's RFSoC
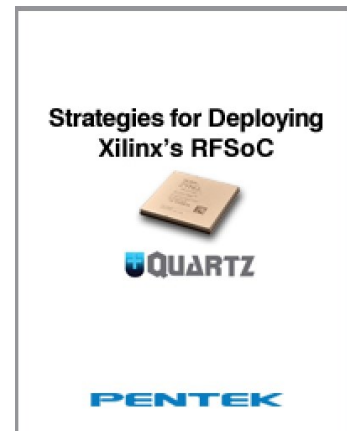
General Information

The Quartz® Model 5953 is a high-performance 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC FPGA. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The Model 5953 brings RFSoC performance to 3U VPX with a complete system on a board.

Complementing the RFSoC's on-chip resources are the 5953's sophisticated clocking section for single board and multiboard synchronization, a low-noise front end for RF input and output, up to 16 GB of DDR4, a PCIe interface, a gigabit serial optical interface capable of supporting dual 100 GigE connections, and general-purpose serial and parallel signal paths to the FPGA.

Board Architecture

The 5953 board design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Pentek-developed IP and software functions utilize this architecture to provide data capture, timing, and interface solutions for many of the most common application requirements.
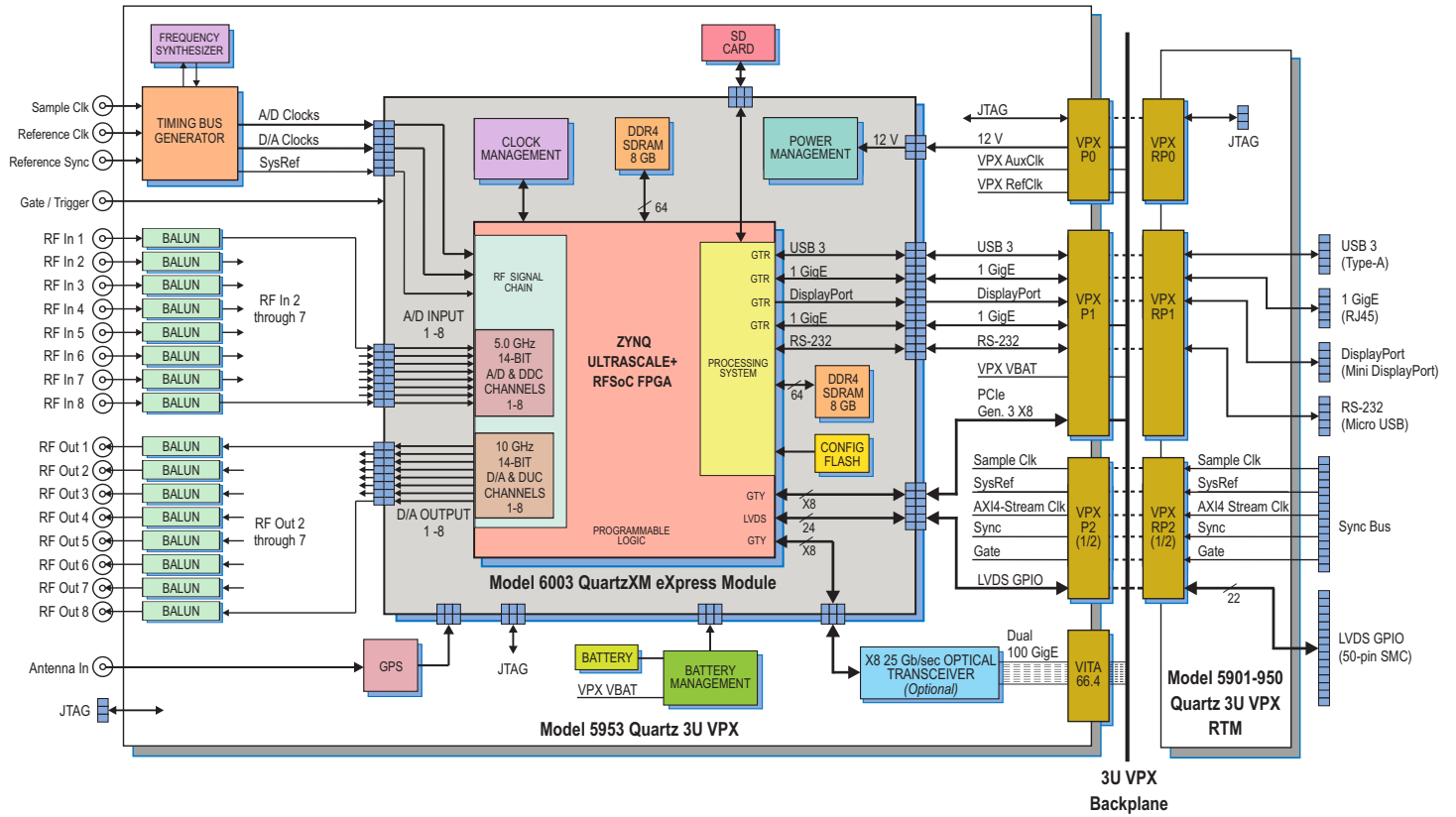
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5953's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 5953 either from applications running locally or on the ARMs, or using the Navigator API, control and command from remote system computers.

5953 Block Diagram

Model 5953 Quartz 3U VPX

Model 6003 QuartzXM eXpress Module

Model 5901-950 Quartz 3U VPX RTM

3U VPX Backplane

A/D Converter Stage

The 5953 accepts analog IF or RF inputs on eight front panel coax connectors. These inputs are transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 5 GSPS, 14-bit A/D converters. Each converter has built-in digital down-converters with programmable 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, or 40x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A Converter Stage

The RFSoC's eight D/A converters accept base-band real or complex data streams from the FPGA's programmable logic. Each 10 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, or 40x. Each D/A output is transformer coupled to a coax connection located on the front panel.

Clocking and Synchronization

The 5953 front panel includes inputs for sample clock, reference clock, reference sync, and gate/trigger. In addition to the front panel, Sync Bus signals are available on the VPX P2 connector for use with the Model 9103 High- Speed System Synchronization and Distribution Amplifier for synchronizing up to 8 5953s in larger, multi-channel systems with single sample accuracy across all channels.

The on-board timing bus generator uses these signals, in addition to a frequency synthesizer, to create the required A/D and D/A clocks and a SysRef for operation of the data converters. The timing bus generator supports an internal clock mode where the sample clock is driven by the programmable frequency synthesizer and no additional clock needs to be provided. In an alternate mode, the on-board sample clock can be synchronized to a 10 MHz reference clock received through a front panel connector.

The Model 5953 can also accept an external sample clock through a front panel connector. This mode bypasses the on-board sample clock. A multifunction gate/trigger input is available on the front panel for external control of data acquisition and playback.

Memory Resources

The 5953 architecture supports 8 GB bank of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, along with the Pentek-supplied DDR4 controller core within the FPGA, can take advantage of the memory for custom applications.

An 8 GB bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

PCI Express Interface

The Model 5953 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

GPS

A GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and 10 MHz reference clock to the FPGA.

Expandable I/O

The Model 5953 supports the VITA-66.4 standard providing eight 25 Gb/sec full duplex optical lanes to the backplane. With the built-in 100 GigE UDP interface or installation of user-provided serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

Eleven pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O.

Rear Transition Module

The Model 5901 RTM complements the 5953 by providing rear backplane access to standard interfaces including: JTAG, USB 3, 1 GigE, DisplayPort, and RS-232. The RTM also includes a multisignal Sync Bus connector for synchronizing multiple 5953s with the Model 5903 Quartz® Synchronization 3U VPX board, and a general-purpose FPGA I/O connector is also provided for access to 11 LVDS pairs from the FPGA.

RTM Panel Connections

The picture below shows the Model 5901-950 Rear Transition Module panel.
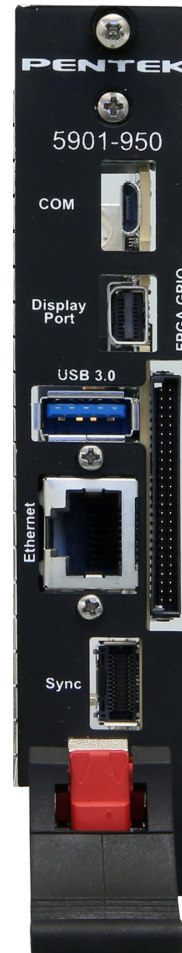

- **COM:** RS-232 interface the processor over Micro USB connector
- **DisplayPort:** Mini DisplayPort connection to processor (*currently not supported*)
- **USB 3.0:** Type-A USB 3.0 interface to the processor.
- **Ethernet:** RJ45 1GigE interface to the processor
- **Sync:** Multi-pin, high-speed connector for multiboard synchronization
- **FPGA GPIO:** 11 pairs of LVDS connections to the programmable fabric for custom I/O

Optimized IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Pentek helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications.
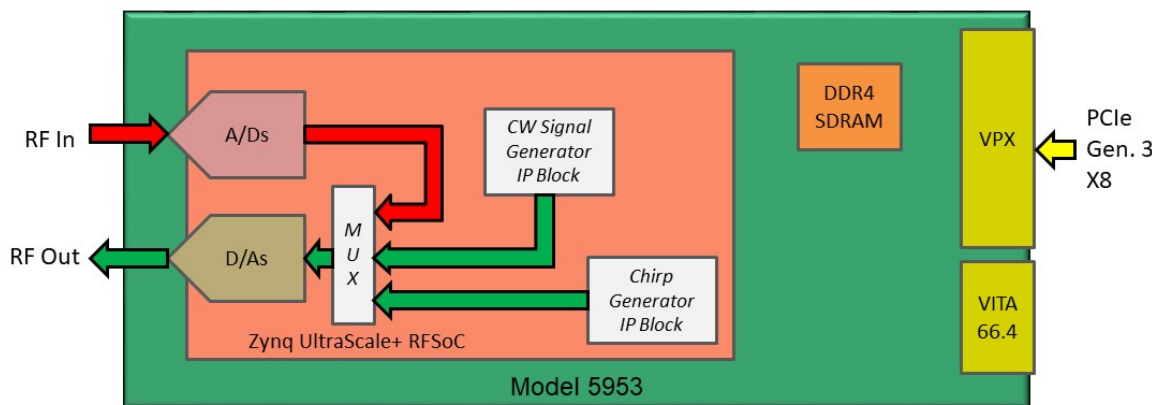
Example Application 1 - High Bandwidth Data Streaming

The RFSoC's eight A/Ds are capable of producing an aggregate data rate of 80 GB/sec when all channels are enabled. While capturing and storing this much raw data is not feasible, the A/Ds built-in digital down-converters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system. In some applications capturing the raw, full bandwidth data is crucial. The 5953's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board. Along with the built-in data acquisition IP, the 5953 can stream raw data from two A/D channels running at 4 GSPS over optical cable to a downstream storage or processing subsystem.
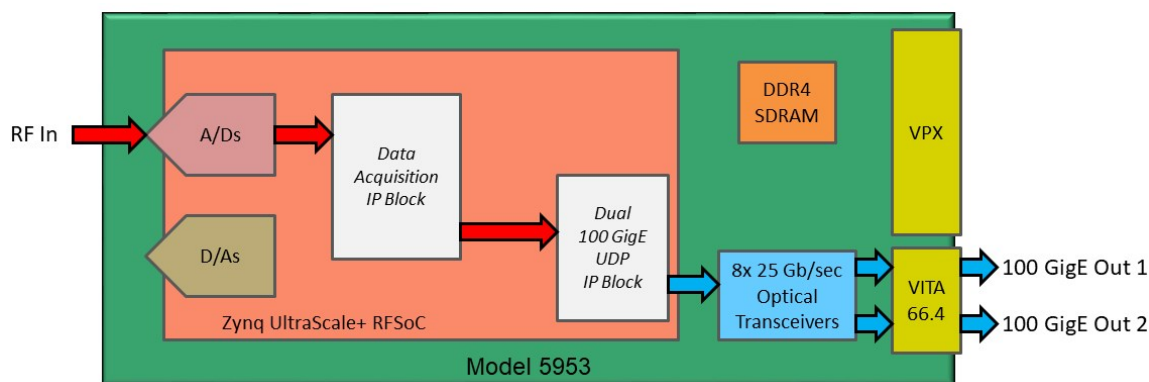
Example Application 2 - Waveform Generator

The 5953's IP supports multiple D/A signal source options. A simple loopback path allows samples received by the A/Ds to be output through the D/As. A CW signal generator produces a sine output with programmable frequency. A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset, and length. The generators also include flexible trigger options with both internal and external triggering.

Example Application 3 - Multimode Data Acquisition System

In some applications multiple data acquisition modes may need to be operated at the same time. A required dataflow could be full bandwidth streaming of a single A/D channel over 100 GigE to a data recorder while another channel of A/D data is stored as snapshots in the board's DDR4 SDRAM and read by the ARM processor while yet other A/D channels are down converted using the A/Ds' built-in DDCs and streamed over PCIe. The 5953 provides these modes with built-in IP supporting complex data streaming scenarios without the need for creating custom IP.
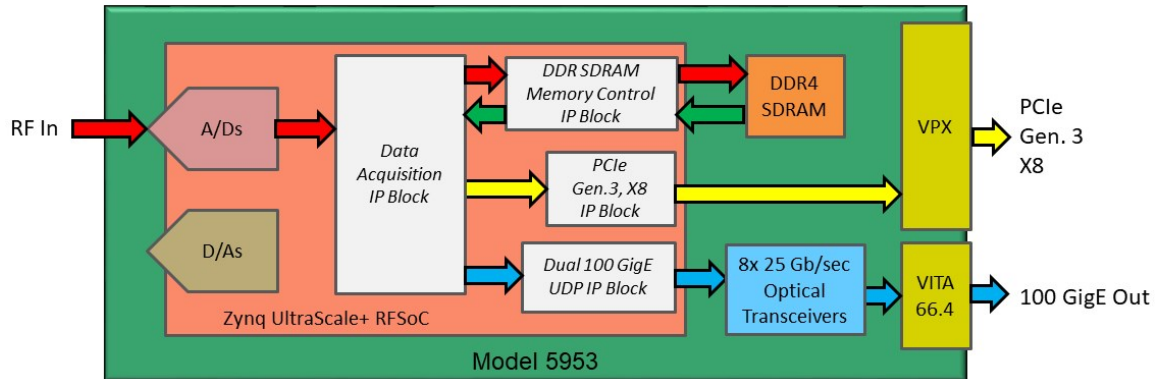
Flexible Modular Design

While Pentek's 5953 follows the form factor of a standard 3U OpenVPX board, the unique modular design of Pentek's Model 6003 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC FPGA, DDR4 SDRAM, and power and clock management.

In the case of Model 5953, the QuartzXM is mounted on a 3U OpenVPX carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver, and an 8x 25 Gbps optical transceiver. As a module and carrier board set, the 5953 becomes a complete, ready-to-deploy 3U OpenVPX solution available for a range of operating environments from commercial to rugged and conduction-cooled.

The Model 6003 QuartzXM can also be mounted on other carriers available from Pentek to support standard form factors, or for applications that require a non-standard footprint, Pentek supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application-specific carrier design.
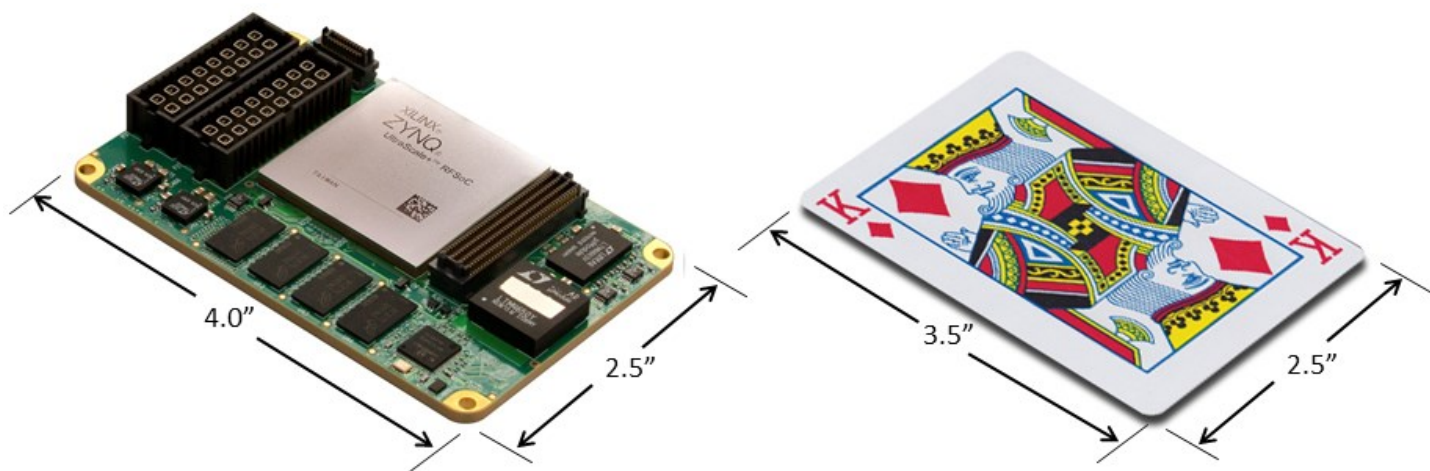

Model 6003 QuartzXM eXpress Module

Navigator Design Suite

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. Multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

Navigator IP FPGA Design Viewed in IP Integrator
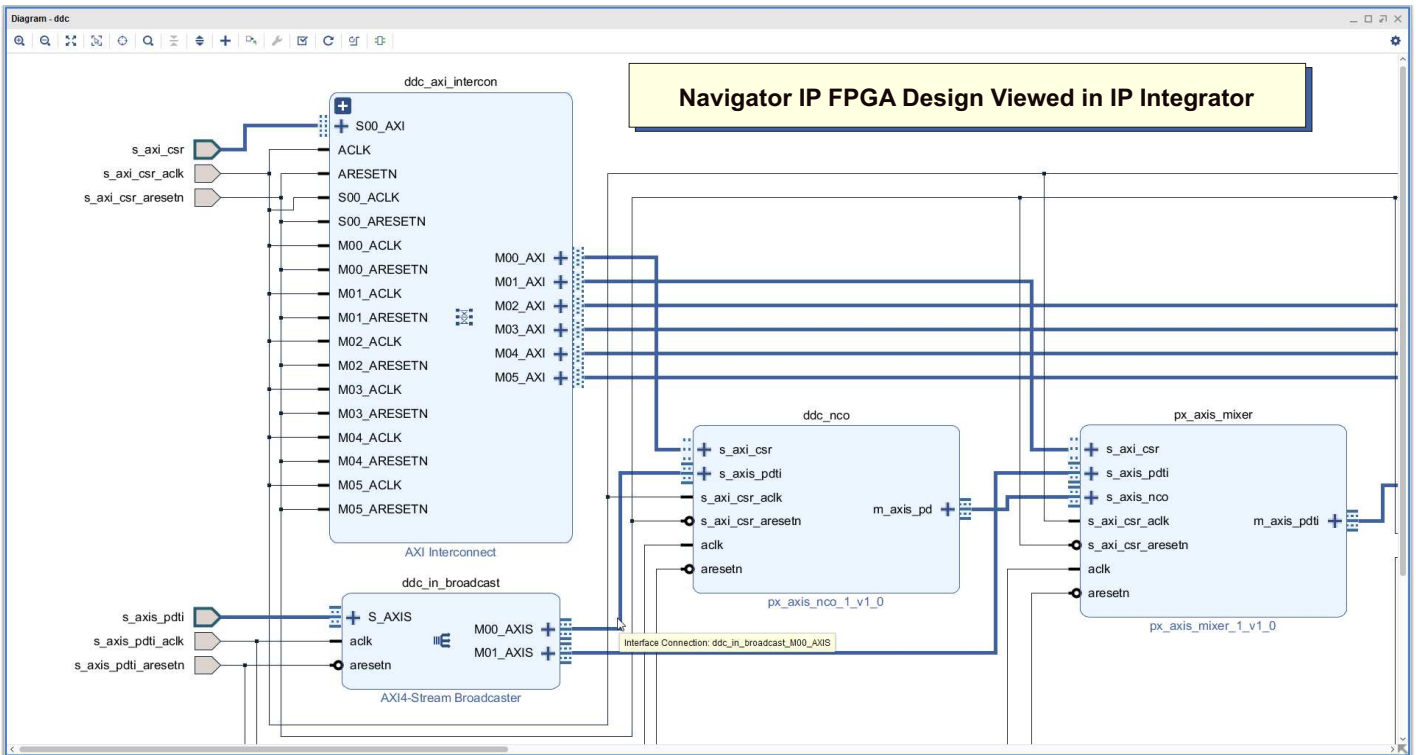
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP's structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.

| NAVIGATOR Board Support Package		NAVIGATOR FPGA Design Kit
Data I/O BSP Module	⟷	Data I/O IP Modules
DSP BSP Module	⟷	DSP IP Modules
Data Acquisition BSP Module	⟷	Data Acquisition IP Modules
Waveform Generation BSP Module	⟷	Waveform Generation IP Module
DMA BSP Module	⟷	DMA IP Module
PCIe & DDR4 SDRAM BSP Module	⟷	PCIe & DDR4 SDRAM IP Module
Utility BSP Module	⟷	Utility IP Module

Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP's extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.
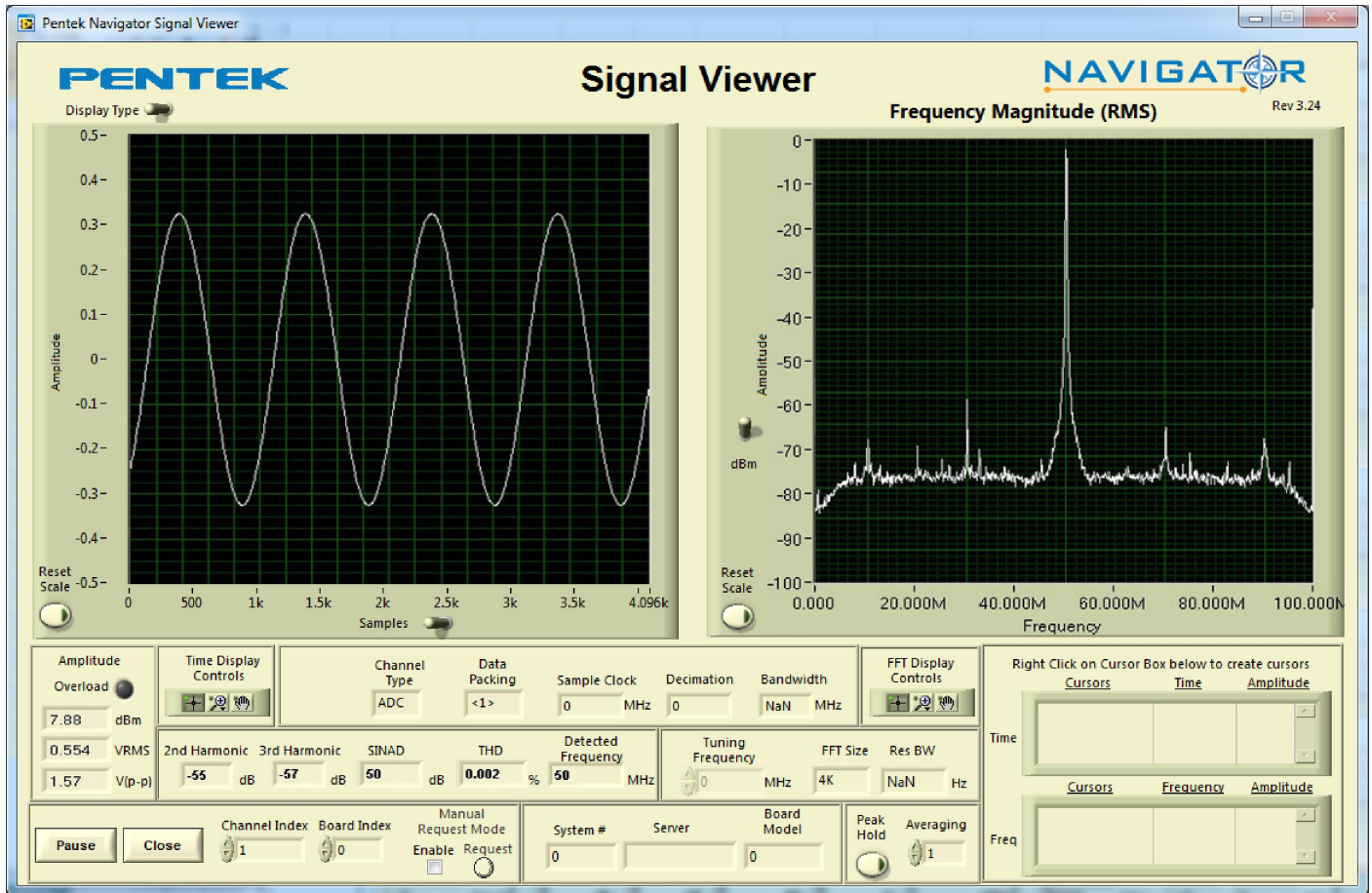
Front Panel Connections

The 5953 is available in air- and conduction-cooled configurations. The picture below shows the front panel of the air-cooled 5953.
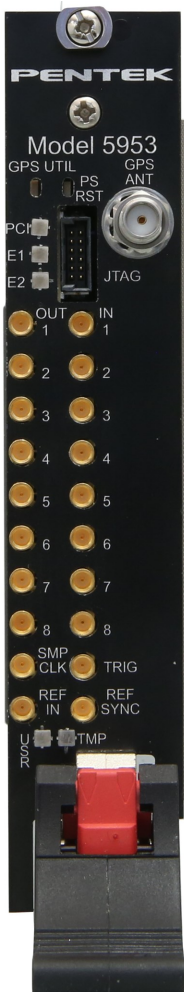
- **GPS Safeboot Power Up Button (Factory Use Only):** The white button, labeled **GPS UTIL**, provides a reset and safe reboot of the onboard GPS receiver.

- **Front Panel Reset Button:** The white button, labeled **PS RST**, provides a reset of the ARM processors.

- **GPS Antenna Connector:** the front panel has a connector, labeled **GPS ANT**, for input of an antenna RF signal for the onboard GPS receiver.

- **PCIe Link Up LED:** The green **PCI** LED illuminates when a valid PCIe link has been established over the VPX interface.

- **Link 1 LED:** The green **E1** LED illuminates when a link is established on 100G Ethernet link #1.

- **Link 2 LED:** The green **E2** LED illuminates when a link is established on 100G Ethernet link #2.

- **JTAG Connector:** The 5953 includes a **JTAG** connector on the front panel. This is used to download to the FPGA and program QSPI configuration memory.

- **8 A/D Input Connectors:** The 8 MMCX connectors labeled **IN 1-8** provide A/D input to the A/D Converters on the 5953.

- **8 D/A Output Connectors:** The 8 MMCX connectors labeled **OUT 1-8** provide D/A output from D/A Converters on the 5953.

- **Sample Clock Connector:** The MMCX connector labeled **SMP CLK** provides an input for an external sample clock when external sample clock mode is selected.

- **Trigger Connector:** The MMCX connector labeled **TRIG** provides a trigger input. This trigger input is DC coupled and compatible with the LVTTL levels, but is 5V tolerant. This trigger, being an LVTTL signal, is not meant for high accuracy in relation to the sample clock as its rise time is on the order of nanoseconds.

- **Reference Clock In Connector:** The MMCX connector labeled **REF IN** provides an input for an external 10 MHz reference. This signal can be used to lock the on-board sample clock synthesizer to an external reference. It is optimally a sinewave signal.

- **Reference Clock Sync Connector:** The MMCX connector labeled **REF SYNC** provides an input for reference clock synchronization.

- **User LED:** The yellow **USR** LED is available for user applications.

- **Over Temperature LED:** The red **TMP** LED illuminates when an over−temperature or over−voltage condition is indicated by the temperature/voltage sensors on the 5953.

Specifications

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU47DR
   Option -048: RFSoC XCZU48DR
Speed: (standard) -1 speed grade
   Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs
   Quantity: 8
   Connectors: MMCX
   Location: Front panel
   Input Type: Transformer-coupled
   Transformer Type: Mini-Circuits TCM1-83X+
   Full Scale Input: +8 dBm into 50 ohms
A/D Converters
   Quantity: 8
   Sampling Rate: 5.0 GHz
   Resolution: 14 bits
Digital Downconverters
   Quantity: 1 per A/D
   Decimation Range: 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, and 40x (not all decimations are supported by default IP)
   LO Tuning Freq. Resolution: 48 bits, 0 to f_s
   Filter: 80% passband, 89 dB stop-band attenuation

Analog Outputs
  Quantity: 8
  Connectors: MMCX
  Location: Front panel
  Input Type: Transformer-coupled
  Transformer Type: Mini-Circuits TCM1-83X+
  Full Scale Output: +0 dBm into 50 ohms
D/A Converters
  Quantity: 8
  Sampling Rate: 10 GHz
  Resolution: 14 bits
Digital Upconverters
  Quantity: 1 per D/A
  Interpolation Range: 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, and 40x (not all interpolations are supported by default IP)
  LO Tuning Freq. Resolution: 48 bits
  Filter: 80% pass band, 89 dB stop-band attenuation
Sample Clock
  Source: On-board programmable clock source or external clock source
  Location: Front panel (*for external source*)
  Connector Type: MMCX
  Level: -10 dBm to +10 dBm front panel
Reference Clock
  Source: On-board oscillator, on-board GPS, or external source
  Location: Front panel (*for external source*)
  Connector Type: MMCX
  Level: -10 dBm to +24 dBm
Reference Sync
  Source: Programmable through software or external source
  Location: Front panel (*for external source*)
  Connector Type: MMCX
  Level: TTL
Gate/Trigger
  Source: Programmable through software or external source
  Location: Front panel (*for external source*)
  Connector Type: MMCX
  Level: TTL
GPS
  Source: On-board
  Antenna Connector Location: Front panel
  Connector Type: SMA
Sync Bus
  Signals: Sample Clock, Reference Clock, Reference Sync, Gate/Trigger
  Location: VPX-P2 or RTM
  Connector Type: Multi-pin, high-speed differential (*on RTM*)

RFSoC Processing System
ARM Cortex-A53:
  Quantity: 4
  Speed: 1.5 GHz
ARM Cortex-R5:
  Quantity: 2
  Speed: 600 MHz
Processor I/O:
  Interface: USB 3.0
    Location: VPX-P1 or RTM
    Connector Type: USB Type-A (*on RTM*)
  Interface: 1 GigE
    Location: VPX-P1 or RTM
    Connector Type: RJ45 (*on RTM*)
  Interface: RS-232
    Location: VPX-P1 or RTM
    Connector Type: Micro USB (*on RTM*)
  Interface: DisplayPort (not currently supported)
    Location: VPX-P1 or RTM
    Connector Type: Mini DisplayPort (*on RTM*)

FPGA I/O
  Interface: GPIO
    Quantity: 11 Pairs
    Type: LVDS Location: VPX-P2 or RTM
    Connector Type: 50-pin SMC (*on RTM*)
  Interface: Optical (Option -110)
    Quantity: 8 full duplex lanes
    Speed: 25 Gb/sec
    Laser: 850 nm
    Location: Lower 1/2 of VPX-P2
    Connector Type: VITA 66.4
    Protocol: Factory-installed dual 100 GigE UDP IP cores provides greater than 24 GB/sec data transfers, other protocols supported with user-installed IP

JTAG
  Location: Front panel and VPX-P0 or RTM
  Connector Type: Standard 14-pin header (*on front panel and RTM*)

Memory
Processing System:
  Type: DDR4 SDRAM
  Size: 8 GB
  Speed: 1200 MHz (2400 MHz DDR)
Programmable Logic:
  Type: DDR4 SDRAM
  Size: 8 GB
  Speed: 1200 MHz (2400 MHz DDR)
 FPGA Configuration FLASH
  Type: QSPI NOR Flash
  Size: 2 x 1 Gbit

PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)
   Operating Temp: 0° to 50° C
   Storage Temp: −20° to 90° C
   Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air-cooled)
   Operating Temp: −20° to 65° C
   Storage Temp: −40° to 100° C
   Relative Humidity: 0 to 95%, non-condensing
Option -763: L3 (conduction-cooled)
   Operating Temp: −40° to 70° C
   Storage Temp: −50° to 100° C
   Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board
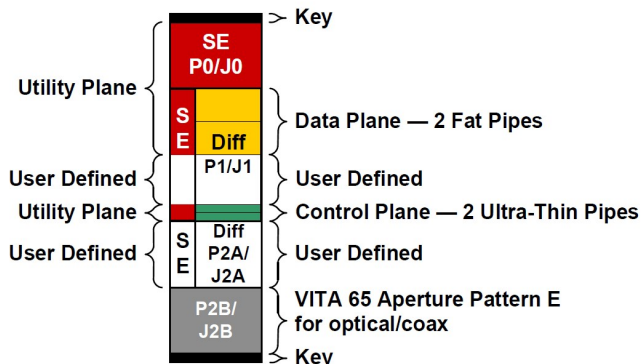   **Depth:** 170.61 mm (6.717 in)
   Height: 100 mm (3.937 in)
Weight: 22 oz (624 grams)

OpenVPX Compatibility

The Model 5953 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:
  SLT3-PAY-2F2U1E-14.6.10-n

Ordering Information

Model	Description
5953	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX

Options	Description
-002	-2 FPGA speed grade, -1 standard
-048	XCZU48DR FPGA (XCZU47DR is standard)
-110	VITA-66.4 8X optical interface
-702	Air cooled, Level L2
-763	Conduction cooled, Level L3
Contact Pentek for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Storage and general options may change, so be sure to contact Pentek for the latest information.	

Accessory Products

Model	Description
5901	Rear Transition Module - 3U VPX

Option	Description
-950	Support for Model 5953

Model	Description
8257	3U VPX Development Chassis

Model 8257

The Model 8257 is a 3U VPX chassis ideal for application development. Offered as a convenient, low cost solution for hosting the 5953, it includes power and cooling to match the 5953's requirements in a portable desktop package.

Model 8257

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458 USA
Tel: +1 (201) 818-5900
Email: sales@pentek.com

Lifetime Applications Support

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