Model 57891 & 58891	Dual L-Band RF Tuner, 4-Channel 400 MHz A/D	Kintex UltraScale FPGA	6U VPX Board

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNAs handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two or four 400 MHz 14-bit A/Ds digitize IF or I+Q signals synchronously
- Two or four FPGA-based multiband DDCs (digital downconverters)
- Xilinx® Kintex® UltraScale™ FPGAs
- Five or ten GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Clock/sync bus for multimodule synchronization
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- SPARK® fully-integrated development system
- Free lifetime applications support

Applications

- Complete radar and software radio interface solution
- Communication receiver
- Radar receiver
- Analog I/O for digital recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The Jade Architecture

Evolved from the proven designs of Pentek's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 57891 & 58891 factory-installed functions include A/D acquisition modules for simplifying data capture and tagging, DDCs (digital downconverters), an RF tuner controller, and specialized DMA engines for efficient data transfers between the board and a host computer.

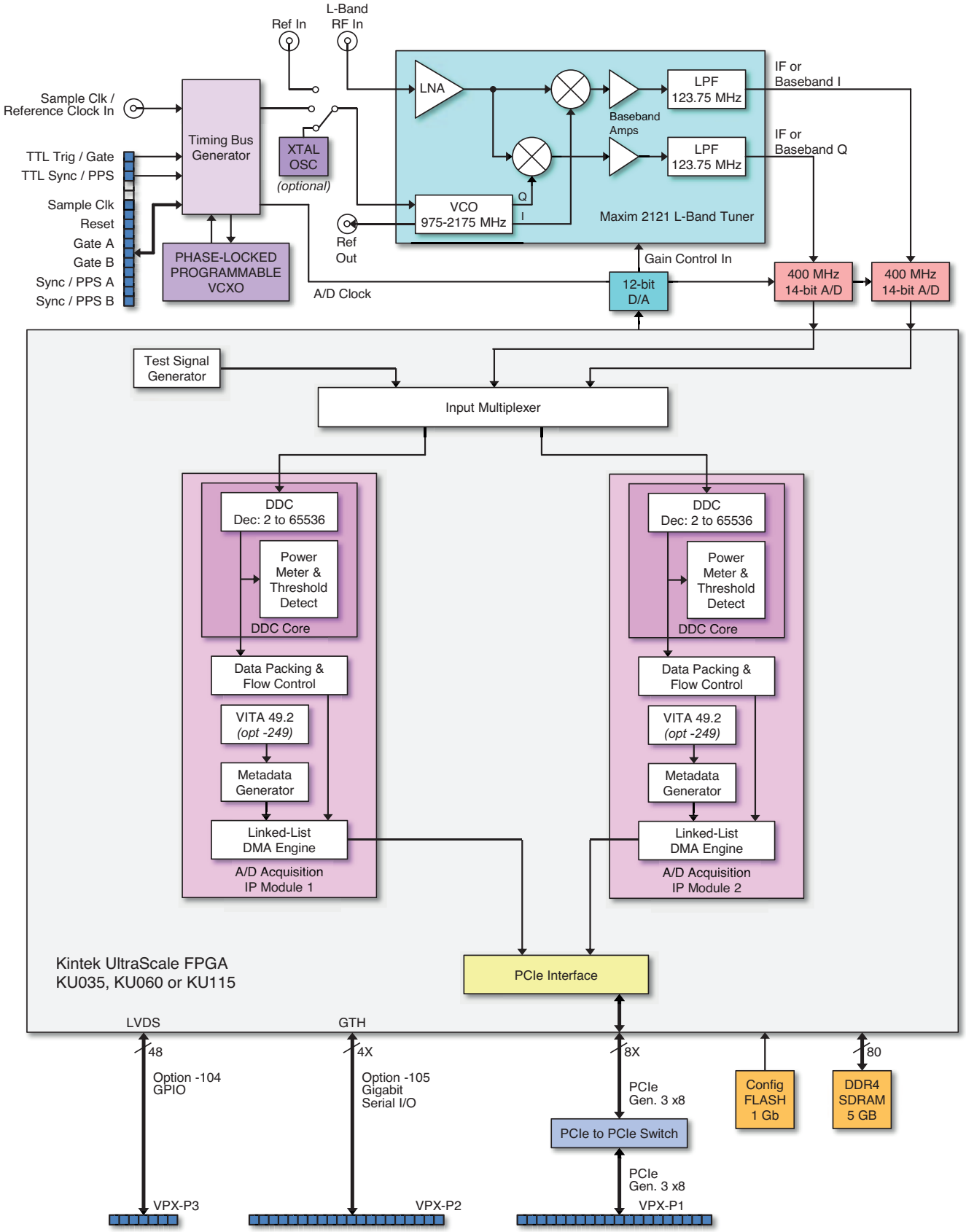
Additional IP includes: an IP module for DDR4 SDRAM memory control; a clock and synchronization generator; a test signal generator, and a PCIe interface. These factory-installed applications enable the 57891 & 58891 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Xilinx Kintex UltraScale FPGAs

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

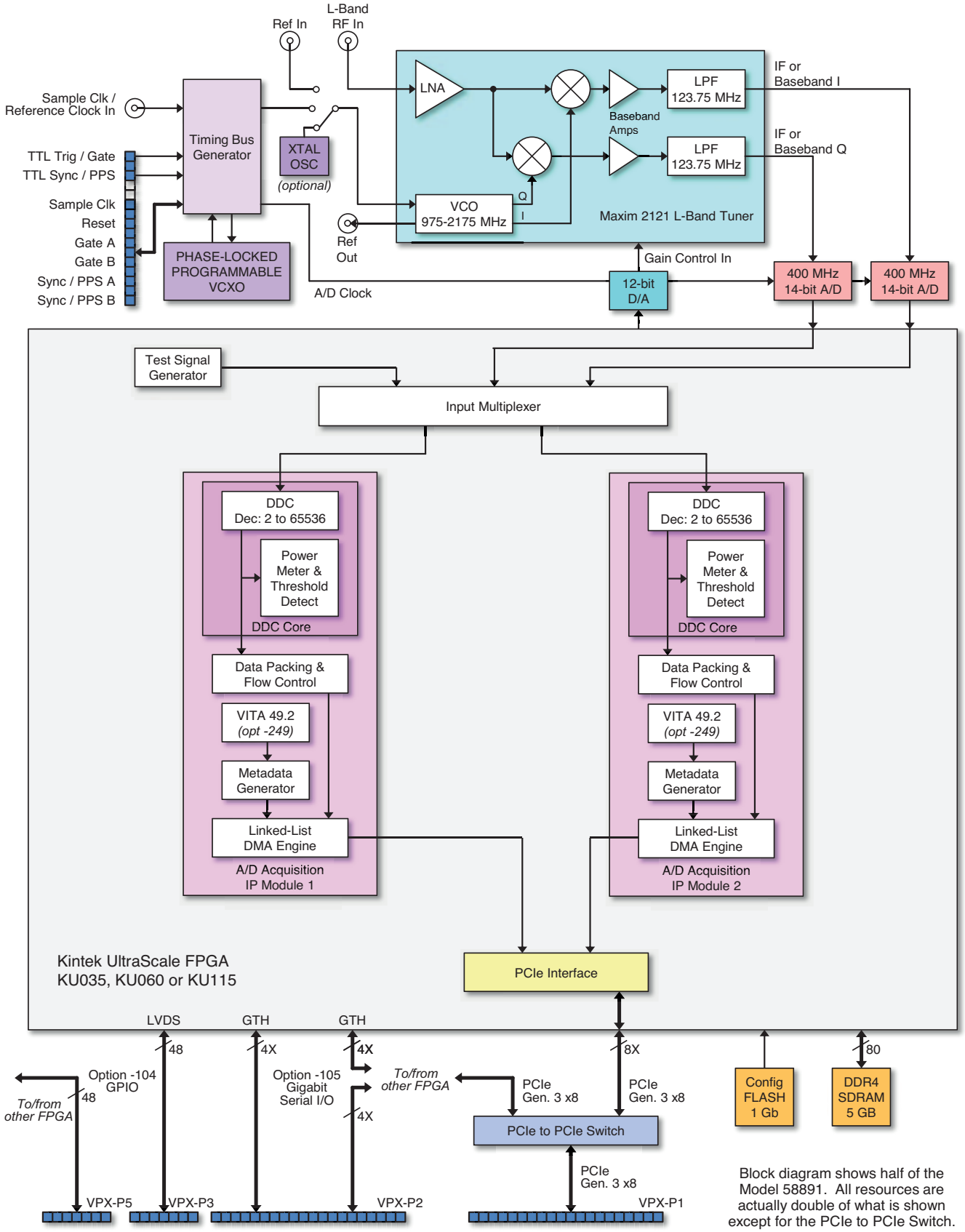
57891 Block Diagram

Click on a block for more information.



58891 Block Diagram

Click on a block for more information.



Block diagram shows half of the Model 58891. All resources are actually double of what is shown except for the PCIe to PCIe Switch.

Board Configuration and Resources

The Models 57891 and 58891 consist of one or two Model 71891 XMC modules mounted on a 6U VPX carrier board. Model 57891 is a 6U board with one Model 71891 XMC module. Model 58821 is a 6U board with two XMC modules.

The descriptions below represent the resources for the Model 57891, a single 71891 XMC module mounted on the 6U VPX carrier. For the Model 58891 with two XMCs mounted, all resources are doubled.

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5474 400 MHz 14-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Acquisition IP Modules

The 57891 & 58891 feature A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator. Each acquisition module has a DMA engine for efficiently moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 65,536 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_S/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_S/N.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/ trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 57891 & 58891 architecture includes a 5 and 10 GB bank of DDR4 SDRAM memory. This resource is used by the board's built-in functions for data storage and buffering, but can also be used for custom applications. The Navigator FDK provides a memory controller as well as guidance on the most efficient use of the memory when creating IP functions.

PCI Express Interface

The 57891 & 58891include industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

6U VPX Interface

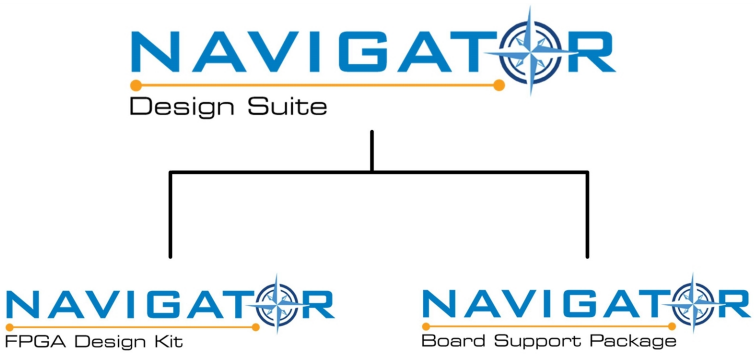
The 57891 & 58891 comply with the VITA 65.0 6U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds additional gigabit serial lanes for supporting user-installed protocols. On the 57891 option -105 installs four lanes from the FPGA to the P2 connector. On the 58891 the option installs four lanes from each of the FPGAs to the P2 connector and an additional four lanes between the FPGAs.

The 57891 & 58891 offer flexible interface options for the VPX-P3 and -P5 to meet system-specific requirements.

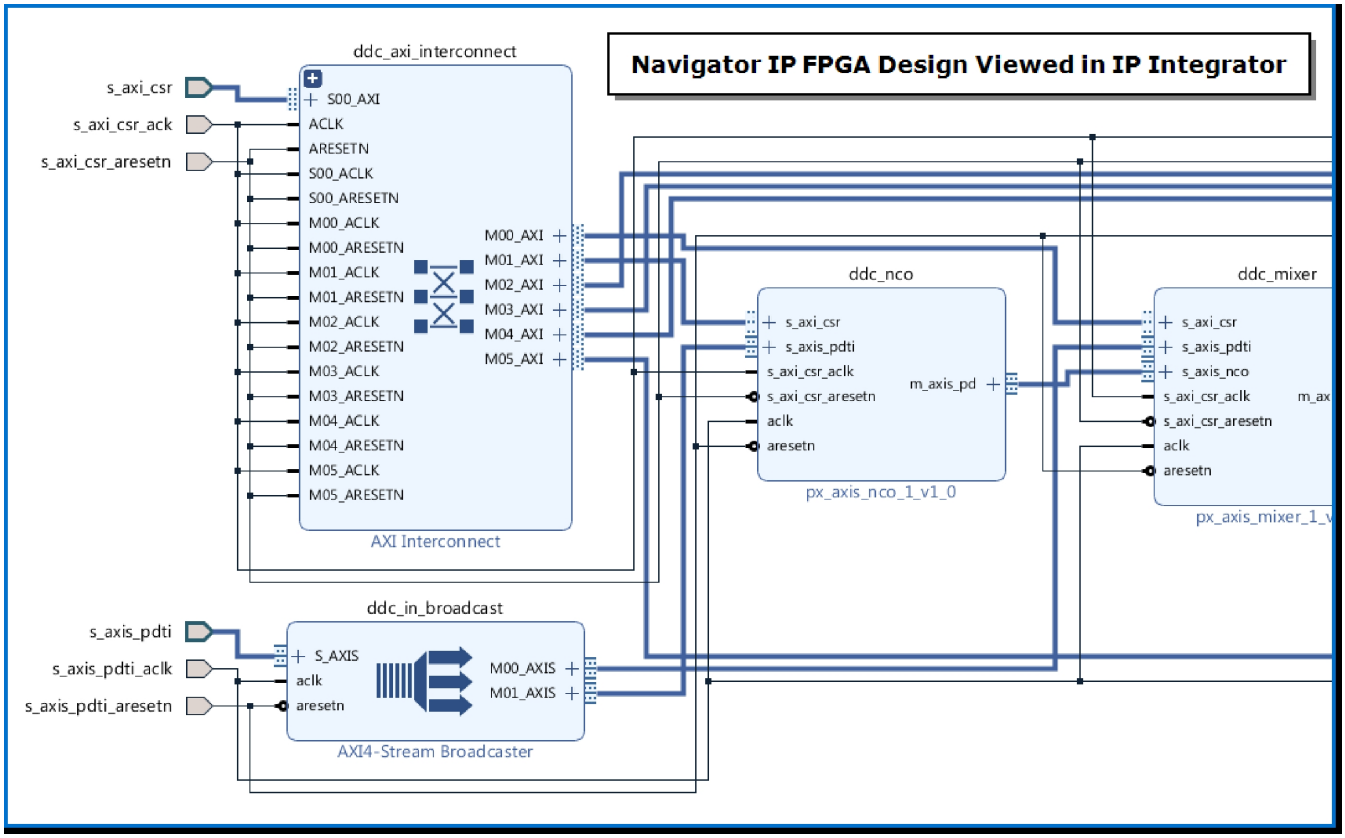
On the 57891 option -104 installs 24 pairs of LVDS connections between the first FPGA to the P3 connector. On the 58891 the option installs an addition 24 pairs between the second FPGAs and the P5 connector.

Navigator Design Suite

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

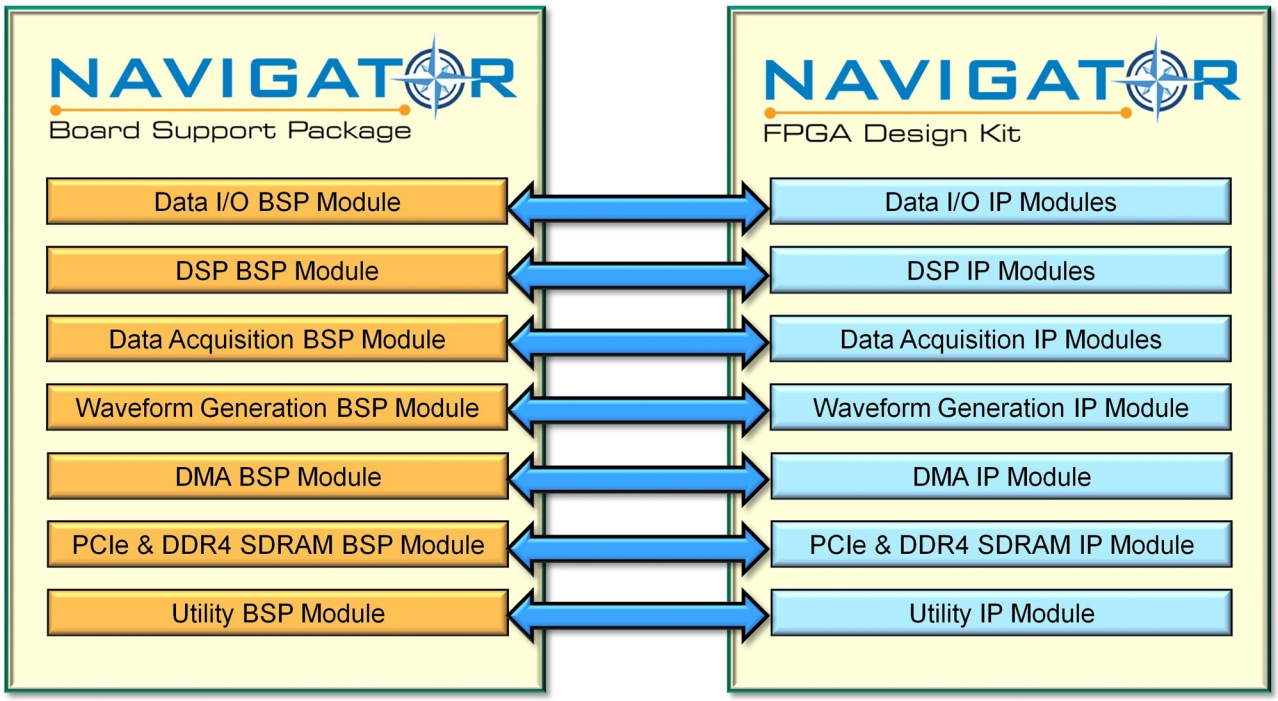


The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.



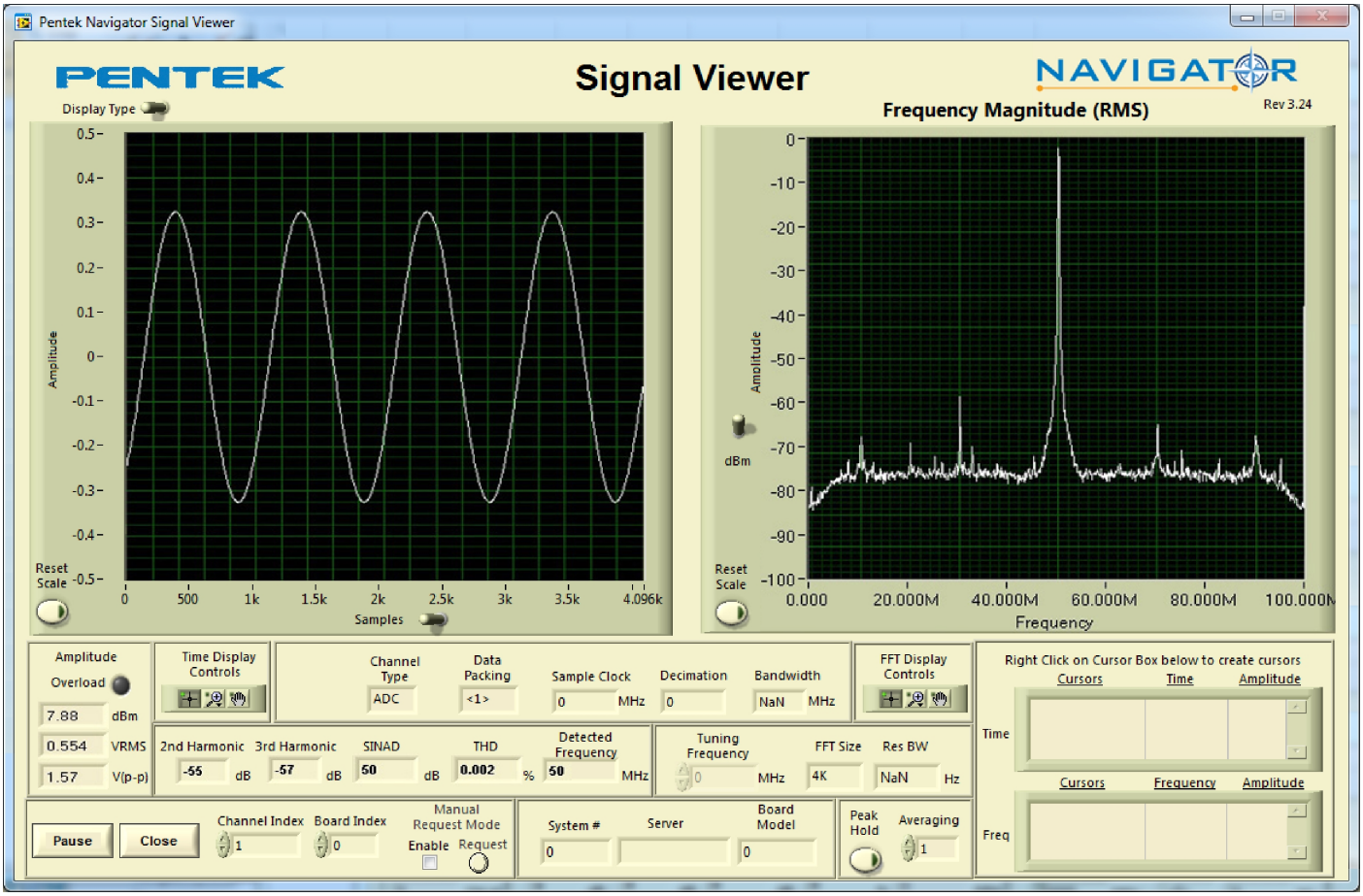
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



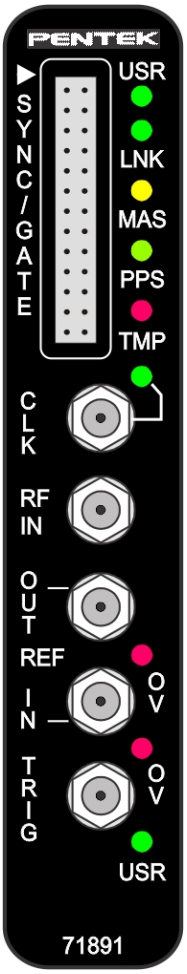
Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



Front Panel Connections

The XMC front panel includes five SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of clock, trigger and analog signals. The front panel also includes nine LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **User LED:** The green **USR** LED is for user applications.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **MAS LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected.
- **Reference Clock Input Connector:** One SSMC coaxial connector for a RF analog signal input, labeled **RF IN.**
- **Reference Clock Output Connector:** One SSMC coaxial connector for a tuner reference clock output, labeled **REF OUT.**
- **Analog Signal Input Connector:** One SSMC coaxial connector, labeled **REF IN**, is for a tuner reference clock input.
- **ADC Overload LEDs:** Two red **OV** (overload) LEDs for each A/D channel.
- **Trigger Input Connector:** The SSMC coaxial connector labeled **TRIG** is for input of an external trigger or gate signal. The signal must be a LVTTL signal.
- **User LED:** One green **USR** LED for user applications.

Specifications

Front Panel Analog Signal Inputs

Connector: Front panel female SSMC
Quantity: 57891 one, 58891 two
Impedance: 50 ohms

L-Band Tuner
Type: Maxim MAX2121
Quantity: 57891 one, 58891 two
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: freqVCO = (N.F.) x $freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters
Type: Texas Instruments ADS5474
Quantity: 57891 two, 58891 four
Sampling Rate: 10 MHz to 400 MHz
Resolution: 14 bits

Sample Clock Sources
On-board timing generator/synthesizer

A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Timing Generator External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus

26-pin front panel connector LVPECL bus includes, clock/ sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/ PPS inputs

External Trigger Input

Quantity: 2
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: provides 24 or 48 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O
Option -105: provides an 4X gigabit link between the each FPGA and the VPX P2 connector to support serial protocols, on the Model 58891 a 4X link is provided between FPGAs

Memory

Processing System:
Type: DDR4 SDRAM
Size: 5 or 10 GB each
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: PCI Express Bus: Gen. 1, 2 or 3: x8

Environmental

Standard: L0 (air-cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 3U VPX board
Depth:
Height:
Weight:

Ordering Information

Model	Description
57891 & 58891	Dual L-Band RF Tuner with 4-Channel 400 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

Options	Description
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through VPX P3 and P5
-105	Gigabit serial FPGA I/O through VPX P2
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3
Contact Pentek for compatible option combinations, complete specifications of rugged and conduction-cooled versions. Storage and general options may change, contact Pentek for the latest information.	

Accessory Products

Model	Description
2171	Cable Kit: SSMC to SMA
9193	System Synchronization and Distribution Amplifier

SPARK Development Systems

The Pentek SPARK® systems are fully-integrated development systems for Pentek software radio, data acquisition, and I/O boards. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

The following SPARK systems are available for Pentek's Cobalt®, Onyx®, and Jade® boards: PCIe (Model 8266), 3U OpenVPX (Model 8267) and 6U OpenVPX (Model 8264). For Flexor boards, SPARK systems are available in PCIe (Model 8266) and 3U VPX (Model 8267).

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

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