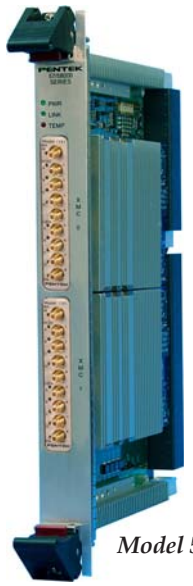
New!

Models 5791 & 5891

Programmable Multifrequency Clock Synthesizer - 6U VPX



Model 5890

Features

- Simultaneous synthesis of up to five or 10 different clocks
- Eight or 16mSMC clock outputs
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to100 MHz
- Four or eight progammable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

ReadyFlow Board Support Package

Ordering Information

Model	Description
5791	Programmable Multifrequency Clock Synthesizer - 3U VPX Single Density
5891	Programmable Multifrequency Clock Synthesizer - 3U VPX Double Density

General Information

Models 5791 and 5891 generate up to eight or 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

These models use four or eight Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These models can be programmed to route any of these frequencies to the board's five or 10 output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or 10 different clocks to various outputs.

With four or eight independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than 10 different clock outputs are required simultaneously, multiple 5891's can be used and phase-locked with a 5 to 100 MHz system reference.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Model 5791: Four
  Model 5891: eight
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

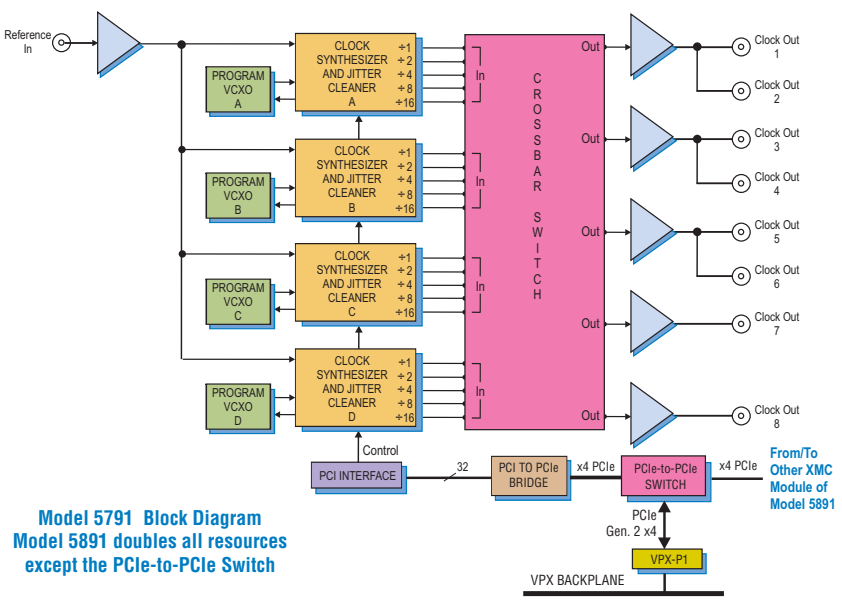
Programmable VCXOs (Four or eight)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Eight or 16)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2: x4, control and status

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)



Model 5791 Block Diagram
Model 5891 doubles all resources except the PCIe-to-PCIe Switch

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