New!

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz, 12-bit A/Ds, with Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX

Model 58841

JADE

NAVIGATOR
Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex Ultra-Scale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57841 and 58841 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, ➤
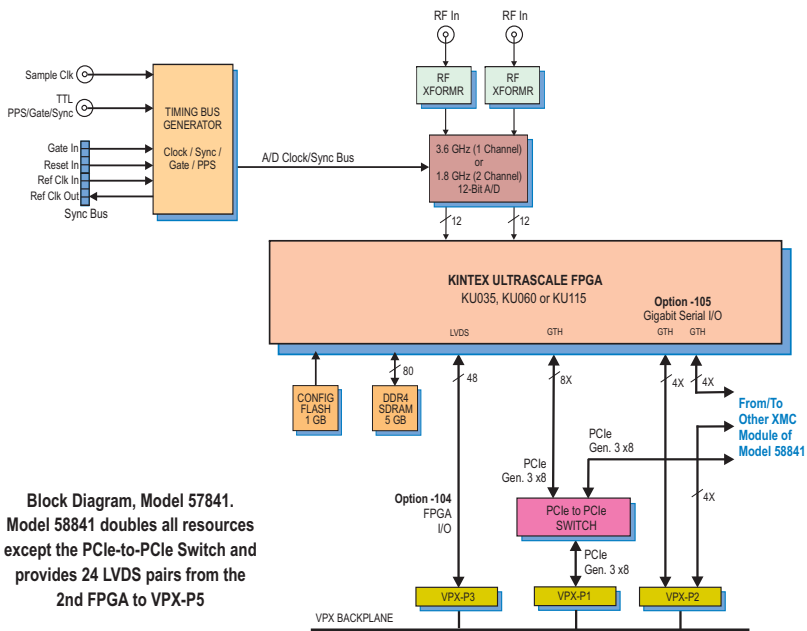
Block Diagram, Model 57841. Model 58841 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.
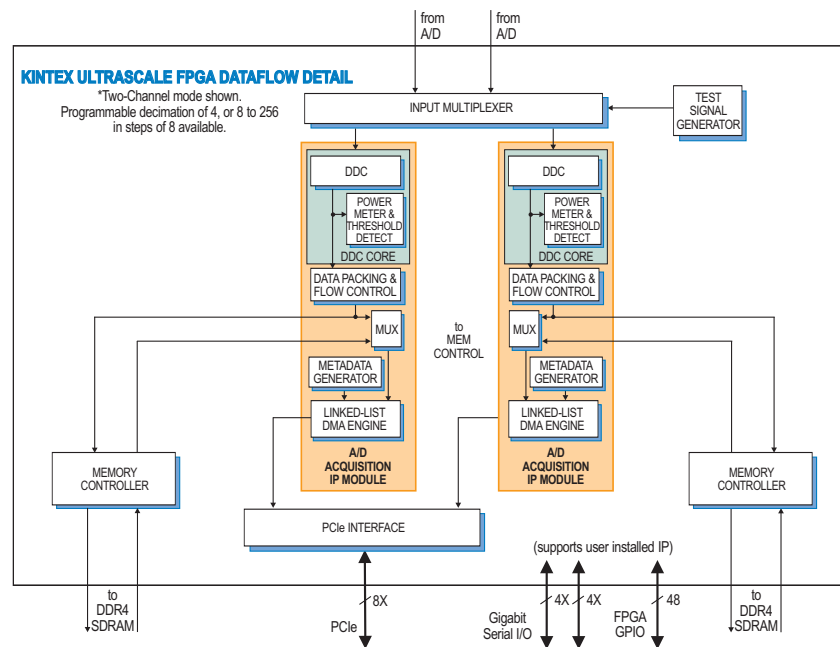
The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel μSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The μSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high-speed sync module to drive the sync bus. ➤

KINTEX ULTRASCALE FPGA DATAFLOW DETAIL

*Two-Channel mode shown.
Programmable decimation of 4, or 8 to 256 in steps of 8 available.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

⬤SPARK
Development Systems

Ordering Information

Model	Description
57841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX
58841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2, Model 57861; P2 and P5 Model 58861
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Memory Resources

The architecture supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Specifications

Model 57861: One A/D
Model 58861: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
  Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
  Type: Texas Instruments ADC12D1800
  Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  Resolution: 12 bits
  Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer
Digital Downconverters (2 or 4)
  Modes: One or two channels, programmable
  Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
  Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
  Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
  Either mode: the DDC can be bypassed completely
  LO Tuning Freq. Resolution: 32 bits, 0 to f_s
  LO SFDR: >120 dB

  Phase Offset Resolution: 32 bits, 0 to 360 degrees
  FIR Filter: User-programmable 18-bit coefficients
  Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: (1 or 2)
  Front panel SSMC connectors
Timing Bus: (1 or 2)
  19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
  Type: Front panel female SSMC connector, LVTTL
  Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
  Standard: Xilinx Kintex UltraScale XCKU035-2
  Option -084: Xilinx Kintex UltraScale XCKU060-2
  Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
  Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57861; and P5 connector, Model 58861 for custom I/O
  Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory
  Type: DDR4 SDRAM
  Size: 5 GB Model 57841; 10 GB Model 58841
  Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
  Standard: L0 (air cooled)
    Operating Temp: 0° to 50° C
    Storage Temp: –20° to 90° C
    Relative Humidity: 0 to 95%, non-condensing
  Option -702: L2 (air cooled)
    Operating Temp: –20° to 65° C
    Storage Temp: –40° to 100° C
    Relative Humidity: 0 to 95%, non-condensing
  Option -713: L3 (conduction cooled)
    Operating Temp: –40° to 70° C
    Storage Temp: –50° to 100° C
    Relative Humidity: 0 to 95%, non-condensing
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)