New!

Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

Model 58690

Cobalt
GateFlow
ReadyFlow Board Support Package

Features

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57690 and 58690 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a VPX carrier board.

Model 57690 is a 6U board with one Model 71690 module while the Model 58690 is a 6U board with two XMC modules rather than one.

These models include one ot two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

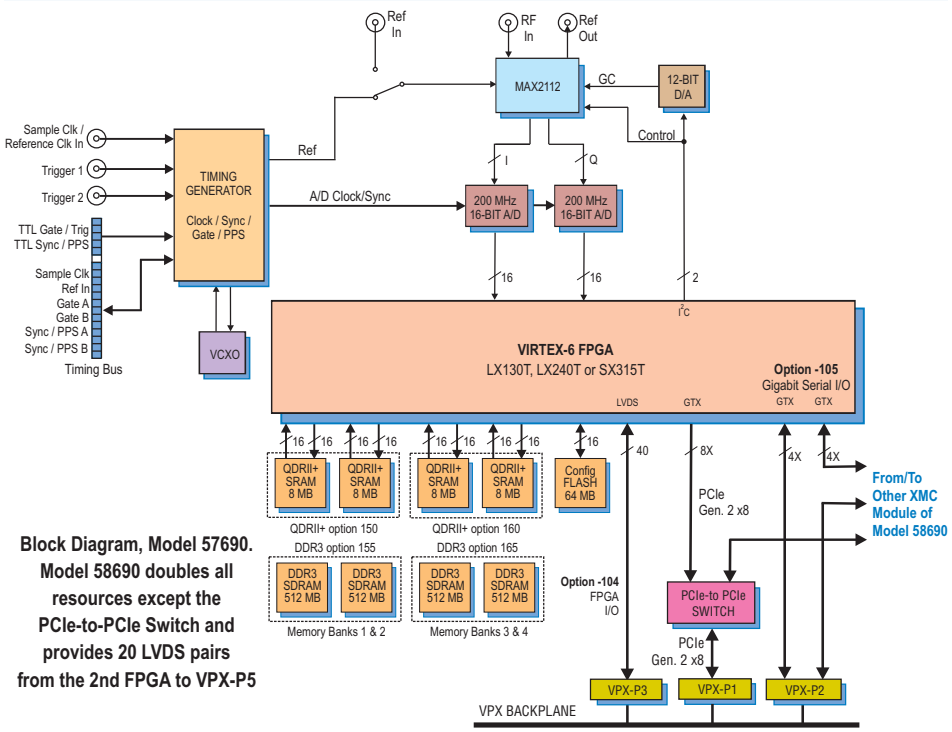
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690. ➤



Block Diagram, Model 57690. Model 58690 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

➤ RF Tuner Stages

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LNBs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNAs offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stages

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the bosrd. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave bosrds, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

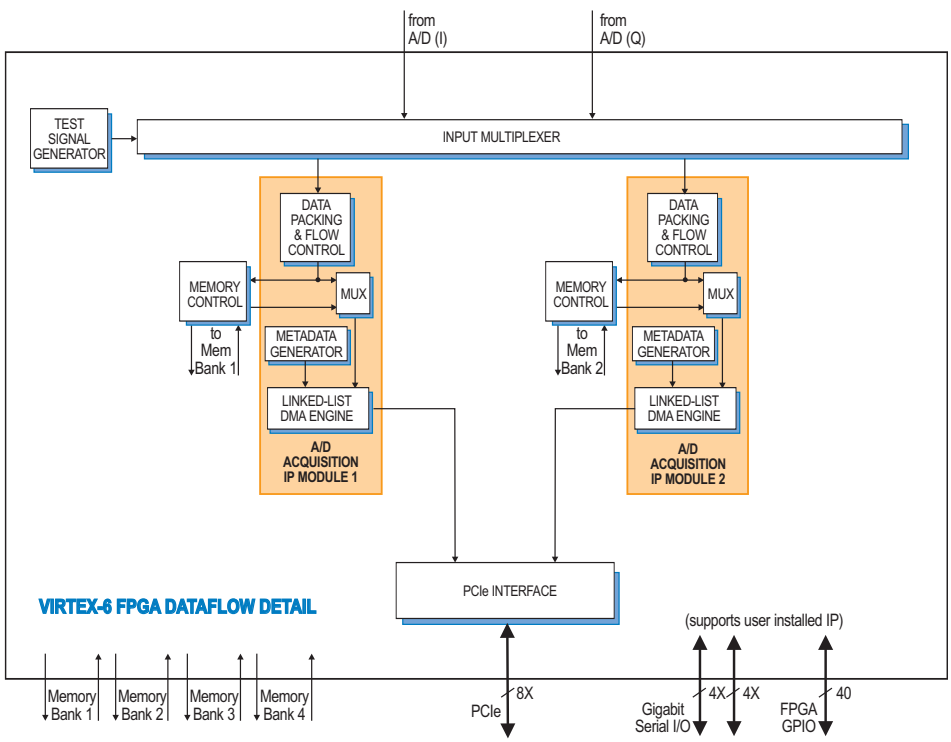
The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

Ordering Information

Model	Description
57690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX
58690	Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57690; P3 and P5 connectors, Model 58690
-105	Gigabit link between the FPGA and P2 connector, Model 57690; gigabit links from each FPGA to P2 connector, Model 58690
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57690: One RF tuner, two A/Ds
Model 58690: Two RF tuners, four A/Ds
Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuners (1 or 2)
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters (2 or 4)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer
A/D Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Inputs (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (2 or 4)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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