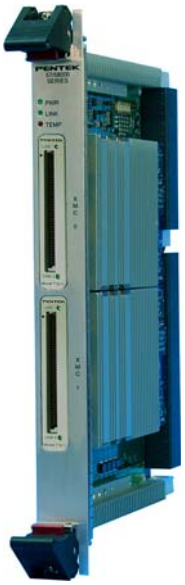
New!

Models 57610 and 58610

Single or Dual LVDS Digital I/O with Virtex-6 FPGA - 6U OpenVPX



Model 58610

General Information

Models 57610 and 58610 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71610 XMC modules mounted on a VPX carrier board.

Model 57610 is a 6U board with one Model 71610 module while the Model 58610 is a 6U board with two XMC modules rather than one.

These models include one or two general-purpose connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The factory-installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, controllers for all data clocking, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

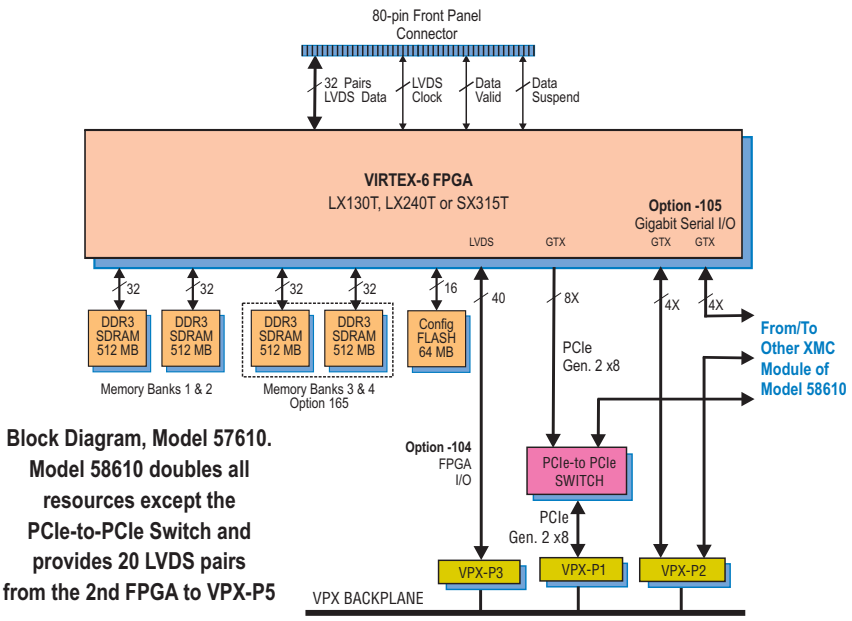
The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58610. ➤

Features

- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57610. Model 58610 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

PENTEK

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Models 57610 and 58610

Single or Dual LVDS Digital I/O with Virtex-6 FPGA - 6U OpenVPX

Ordering Information

Model Description

57610	Single LVDS Digital I/O with Virtex-6 FPGA - 6U VPX
58610	Dual LVDS Digital I/O with two Virtex-6 FPGAs - 6U VPX

Options:

-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57610; P3 and P5 connectors, Model 58610
-105	Gigabit link between the FPGA and P2 connector, Model 57610; gigabit links from each FPGA to P2 connector, Model 78610
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

➤ Acquisition IP Modules

These models can be configured for digital input mode by the setting of one or two jumpers. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that these models are no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Modules

These models can be configured for digital output mode by the setting of one or two jumpers. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

One or two linked-list controllers allow users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 or 128 individual link entries can be chained together to create complex output patterns with minimum programming.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The hardware architecture supports up to four or eight independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 4 GB.

Specifications

Model 57610: Single LVDS Digital I/O
Model 58610: Dual LVDS Digital I/O
Front Panel Input/Output (1 or 2)
Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
Clock: One LVDS differential pair, 2.5 V compliant
Data Valid: One LVDS differential pair, 2.5 V compliant
Data Suspend: One LVDS differential pair, 2.5 V compliant
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58610
Memory Banks (1 or 2)
Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR
PCI Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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