Model 54141A	1-Channel 6.4 GHz A/D or 2-Channel 3.2 GHz A/D, 2-Channel 6.4 GHz D/A	Kintex UltraScale FPGA	3U VPX Board

Features

- Exceptional dynamic range and analog signal integrity
- Xilinx® Kintex® UltraScale™ FPGA
- Compatible with several VITA standards including: VITA 66.5 and VITA 67.3C
- Supports VITA-49.2 VITA Radio Transport standard
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of 2400 MHz DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- SPARK® fully-integrated development system
- Free lifetime applications support

JADE

Applications

- Complete radar and software radio interface solution
- Communication receiver and transmitter
- Radar receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Analog I/O for digital recording and playback
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The Jade Architecture

Evolved from the proven designs of Pentek's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

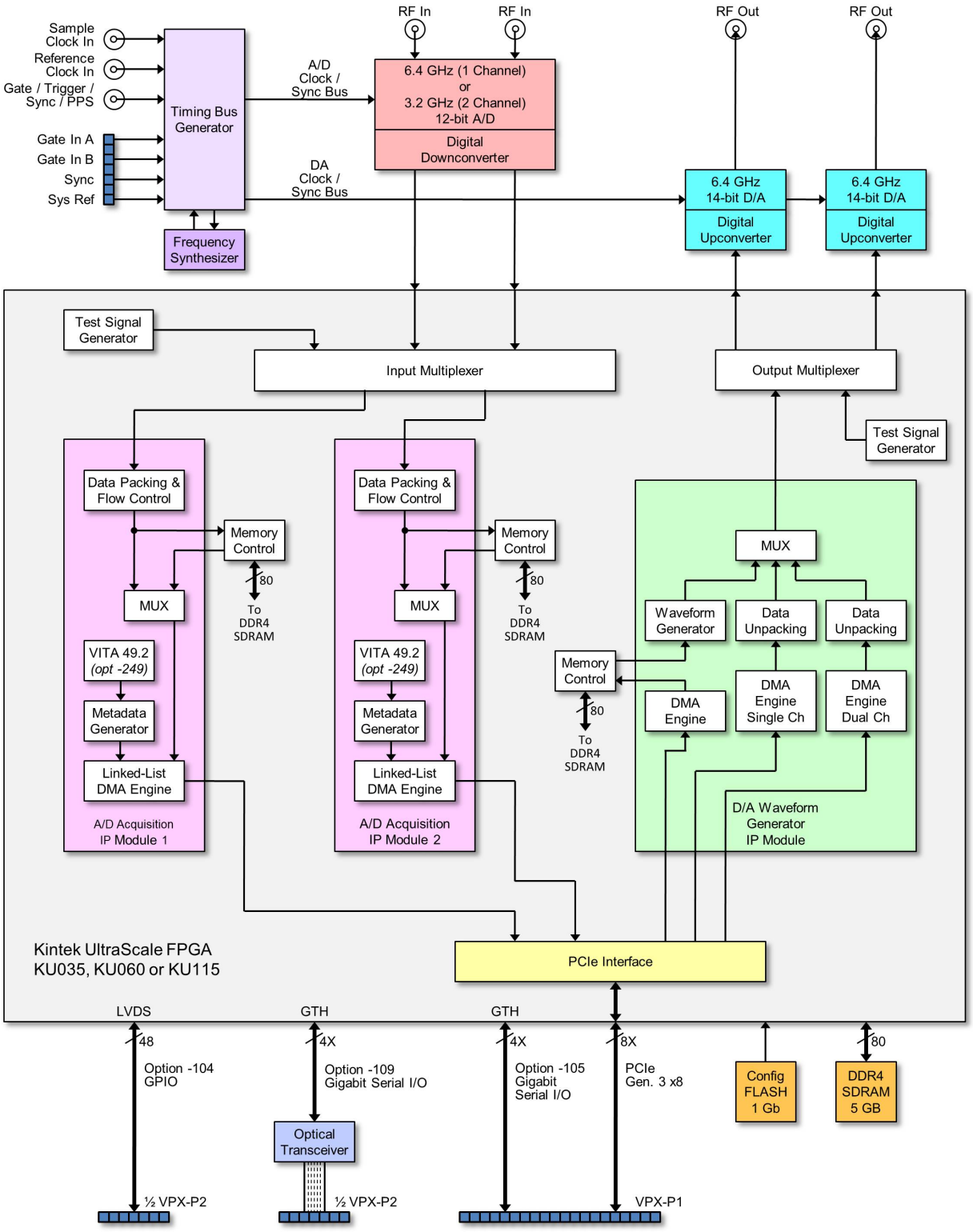
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 54141A factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 54141A to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGAs

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

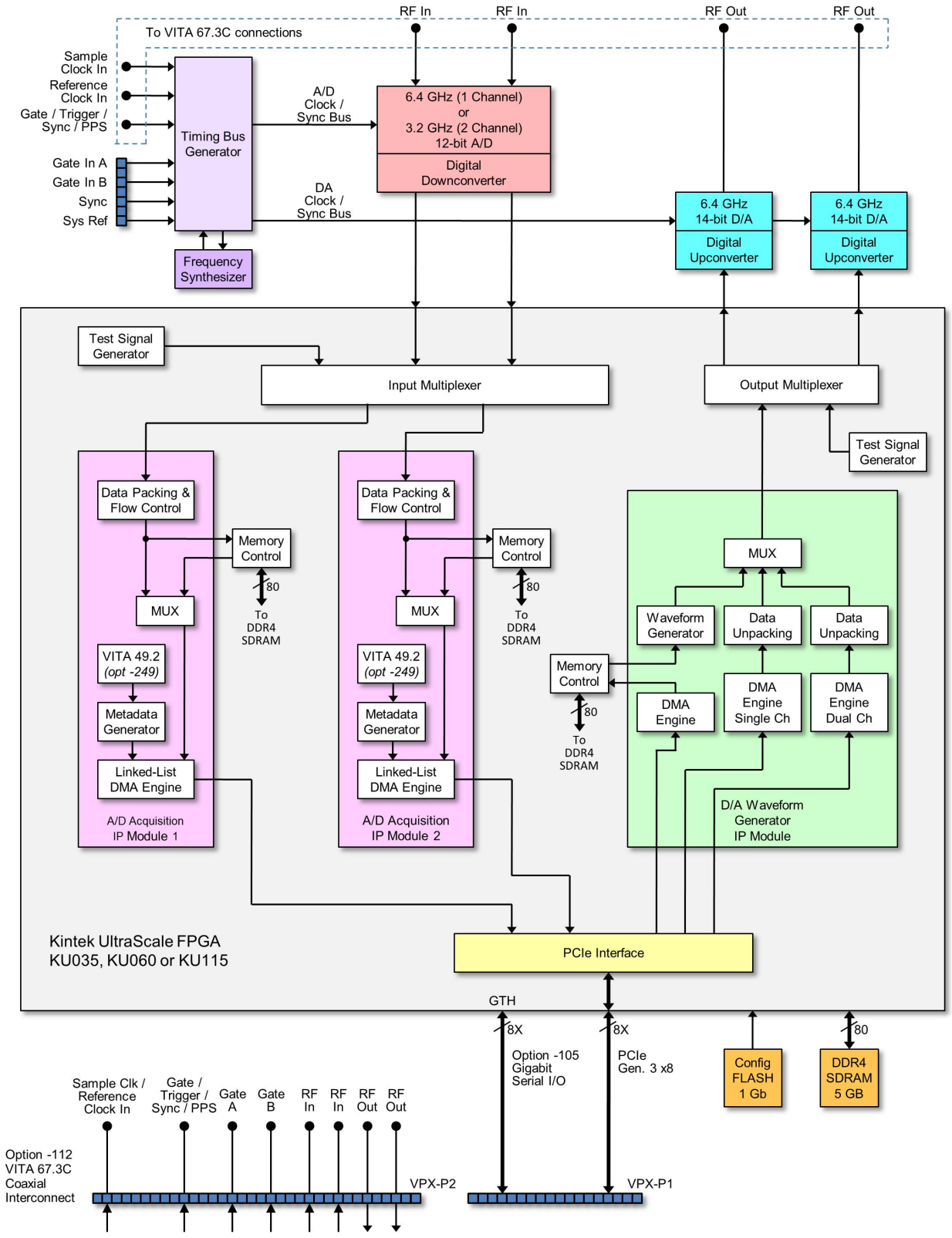
54141 Block Diagram (Standard configuration and option 109 shown.)

Click on a block for more information.



54141 Block Diagram (Option -112 shown.)

Click on a block for more information.



A/D and Digital Downconverter Stage

The board's analog interface accepts analog HF or IF inputs either through a pair of front panel SSMC connectors or the VITA 67.3C connector with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters (DDCs) support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

A/D Acquisition IP Modules

The 54141A features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

VITA 49.2 Radio Transport Standard

VITA 49.2 is a data transport protocol for conveying digitized signal information among signal acquisition/generation and processing elements in a communication, radar or similar system. The 54141A implements the VITA 49 packet format for the ADC/DDC data being transferred to the host memory via DMA.

VITA 49.2 packet elements always supported are:

- Signal Data Packet Type
- Stream Identifier
- Integer Seconds Timestamp
- Fractions Seconds Timestamp
- Trailer

Programmable elements are:

- Packet Size
- Stream Identifier
- Trailer

The Timestamp is automatically inserted from the metadata engine. After initialization an externally applied 1 PPS pulse will increment the Integer Seconds Timestamp. A division of the sample clock will increment the fractional seconds timestamp and this count is reset by the 1 PPS pulse.

VITA 49 packets sent via DMA to the DAC/DUC for output will have the header, stream ID, timestamp and trailer removed leaving only the signal data to be transmitted.

D/A Waveform Generator IP Module

The Model 54141A factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/ As waveforms stored in either on-board memory or off-board host memory.

Digital Upconverter and D/A Stage

A Texas Instruments DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is either through a pair of front panel SSMC connectors or the VITA 67.3C connector.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Clocking and Synchronization

The 54141A accepts a half-rate sample clock via a front panel SSMC connector. In an alternate mode, the sample clock can be sourced from an on-board programmable frequency synthesizer. In this mode, the front panel SSMC connector can be used to provide a reference clock for synchronizing the internal oscillator. A third front panel SSMC connector accepts a TTL signal that can function as a Gate, Trigger Sync or PPS. The clocking and synchronization inputs can also be accepted on the VITA 67.3C connector.

For systems requiring high-channel counts, Model 5292 System Synchronization and Distribution board can synchronize up to four 54141As.

Memory Resources

The 54141A architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The 54141A includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

3U VPX Interface

The 54141A complies with the VITA 65.0 3U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds up to 8 more gigabit serial lanes connected directly to the FPGA for supporting user-installed protocols.

The 54141A offers flexible analog and digital interface options for the VPX-P2 to meet system-specific requirements.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. This option cannot be combined with option -111 or -112.

When purchased with option -109, the 54141A supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high-bandwidth communications between boards or chassis independent of the PCIe interface.

Options -111 and -112 provides analog signal routing through the VPX backplane. Both options replace front panel connectors for RF In, RF Out, Sample Clock/Reference Clock In and Gate/Trigger/Sync/PPS In with coax signals that pass through the backplane for connections to other boards or chassis. Option -111 is compatible with VITA 67.2. Option -112 is compatible with VITA 67.3C.

See Specifications for the OpenVPX Profile.

Navigator Design Suite

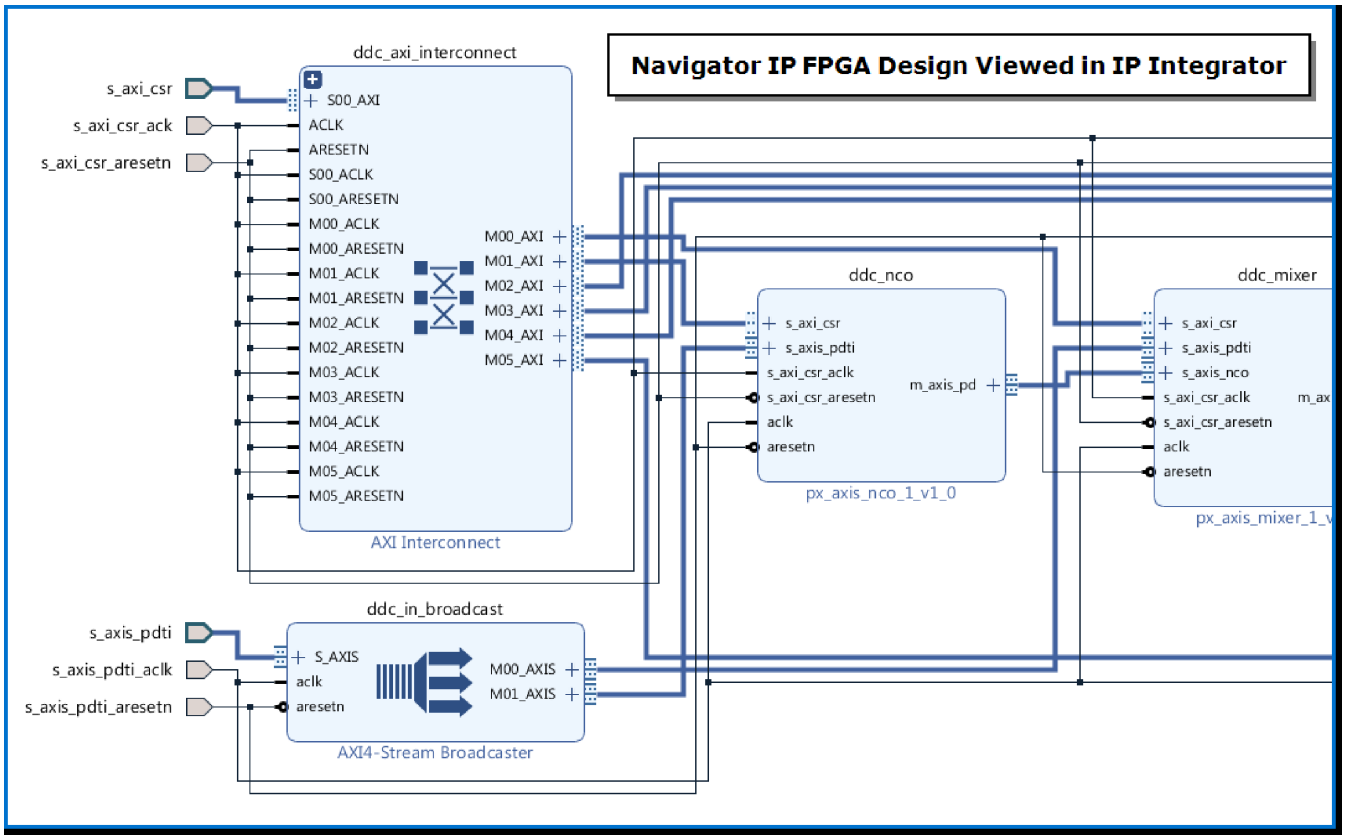
For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

NAVIGATOR Design Suite

NAVIGATOR FPGA Design Kit

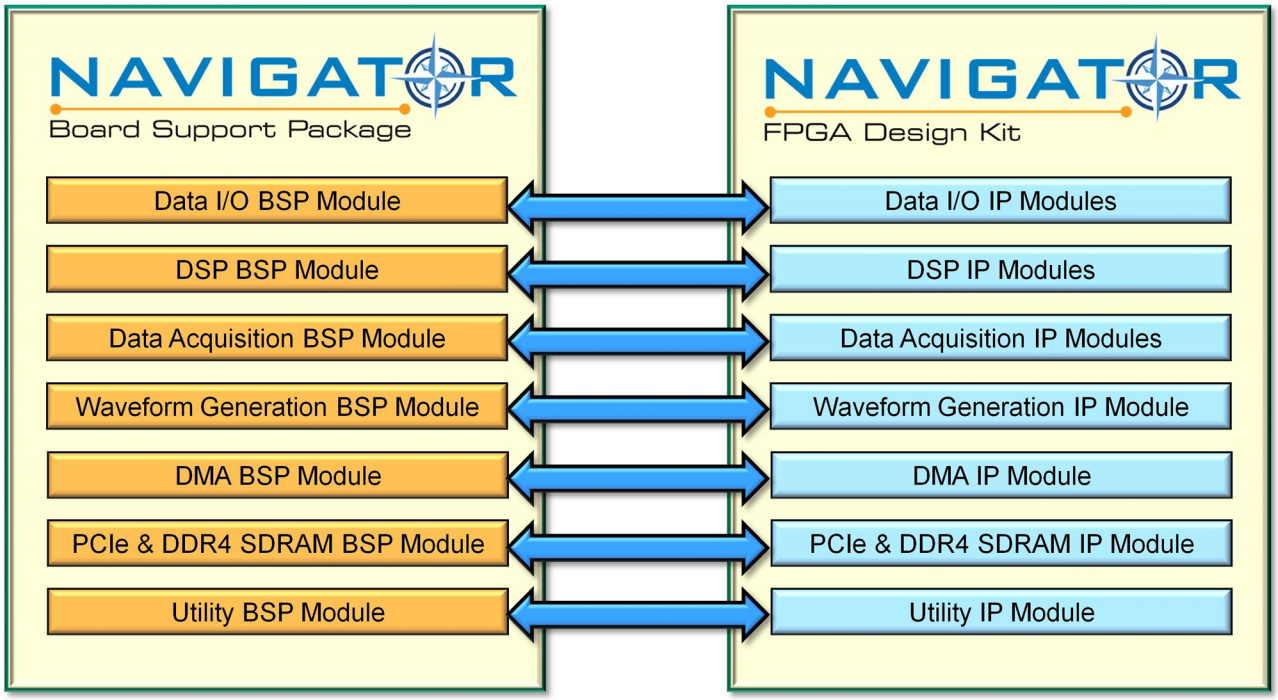
NAVIGATOR Board Support Package

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.



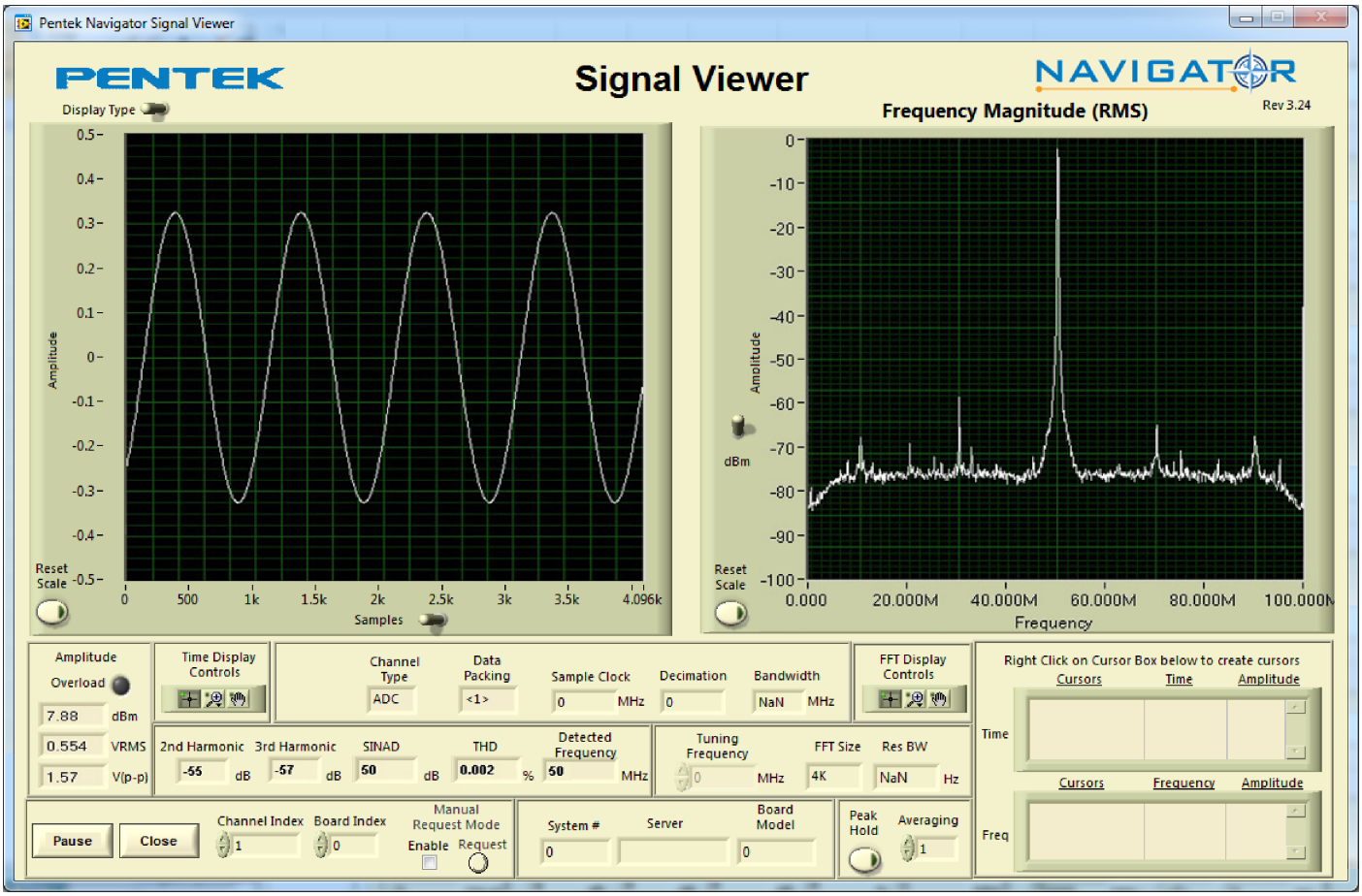
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



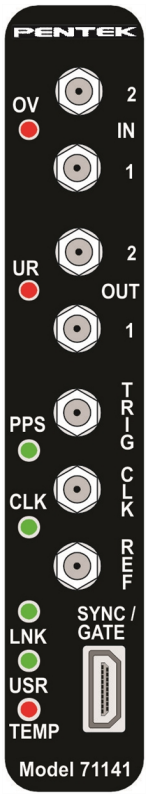
Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



Front Panel Connections

The front panel includes seven SSMC coaxial connectors for input/output of analog RF, clock, and trigger, signals, and a 12-pin Sync Bus input connector. The front panel also includes seven LED indicators.



- **ADC Overload LED:** There is one red **OV** (overload) LED for all ADC inputs. This LED indicates either an overload detection in one of the ADC12DJ3200s, or an ADC FIFO overrun.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **In 1** and **IN 2**: one for each ADC input channel.
- **DAC Underrun LED:** One red underrun **UR** LED for both DAC outputs. This LED illuminates when the DAC38RF82 FIFO is out of data.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and**OUT 2**: one for each DAC38RF82 output channel.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Reference Clock Input Connector:** The SSMC coaxial connector, labeled **REF**, for input of an external reference clock.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **Sync Bus Connector:** The 19-pin µSync front panel connector, labeled **SYNC/GATE**, provides sync and gate input signals for A/D and D/A Processing.
- **User LED:** The green **USR** LED is for user applications.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.

Specifications

Analog Signal Inputs

Input Type:
Standard: Two front panel SSMC connectors
Option -112: Two signals in VITA 67.3C connector
Full Scale Input: +1.0 dBm into 50 ohms
Maximum Power Input: 12 dBm
Input Impedance: 50Ω
Coupling: Transformer coupled
Transformer Type:
Standard: Marki Microwave BALH-0006SMG
Option -201: Marki Microwave BALH-0003SMG
3dB Passband: 0.5 MHz to 6000 MHz (standard)
0.5 MHz to 3000 MHz (Option -201)

Analog to Digital Converter

Type: Texas Instruments ADC12DJ3200 A/D converter
Sampling Rate, Resolution, Decimation: See Configuration Modes table below.
Input Bandwidth: Single-channel mode: 7.9 GHz
Dual-channel mode: 8.1 GHz
Output Interface: JESD204B to FPGA
Clock Source: Sample clock source can be selected from onboard frequency synthesizer or from External Sample Clock Input

Analog Signal Outputs

Output Type:
Standard: Two front panel SSMC connectors
Option -112: Two signals in VITA 67.3C connector
Full Scale Output: +7.5 dBm into 50 ohms
Output Impedance: 50Ω
Coupling: Transformer coupled
Transformer Type: Mini-Circuits TCM3-452X-1+
3dB Passband: 20 MHz to 4000 MHz

Digital to Analog Converters

Type: Texas Instruments DAC38RF82 D/A converter
Sampling Rate, Interpolation: See Configuration Modes table below.
Resolution: 14 bits
Input Interface: JESD204B from FPGA
Clock Source: Sample clock source can be selected from onboard frequency synthesizer or from External Sample Clock Input

Sync Bus Inputs/Outputs

Connector: Front panel 19-pin µSync connector
Gate A In: 2 pins (CML pair)
Sync A In: 2 pins (CML pair)
Gate B In: 2 pins (CML pair)
Sync B In: 2 pins (CML pair)
TWSI Bus: 2 pins

External Gate / Trigger / Sync / PPS Input

Connector Type:
Standard: One front panel SSMC connector
Option -112: One signal in VITA 67.3C connector
Signal Type: LVTTL
Functions: Programmable - trigger, gate, sync, PPS (see below)

Internal Sample Clock Generator

Device: Texas Instruments LMX2594 Fractional-N frequency synthesizer
Reference Source: Selectable from external or internal reference
External Reference: (see External Reference Clock Input below)
Standard: One front panel SSMC connector (shared with External Sample Clock Input)
Option -112: One signal in VITA 67.3C connector (shared with External Sample Clock Input)
Internal Reference: Internal Programmable Frequency Reference
Synchronization: Frequency Synthesizer can be locked to an external 1 to 300 MHz PLL system reference, typically 10 MHz. An on-board internal reference source is also available (see below)
Maximum Synthesizer Output Frequency: 3255 MHz

External Sample Clock Input

Connector:
Standard: One front panel SSMC connector
Option -112: One signal in VITA 67.3C connector
Signal Type: AC signal, 50% duty cycle
Frequency Range: 10 MHz - 4 GHz input clock
Voltage Range: +0 to +10 dBm
Coupling: AC coupled
Input Impedance: 50Ω

Effective Data Converter Sampling Frequency

Either 1x or 2x the internal sample clock generator or external clock, depending on data converter operating modes

External Reference Clock Input

Connector:
Standard: One front panel SSMC connector
Option -112: One signal in VITA 67.3C connector
Signal Type: AC signal, 50% duty cycle
Frequency Range: 0.6 to 300 MHz input clock
Voltage Range: -10 to +24 dBm
Coupling: AC coupled
Input Impedance: 50Ω

Internal Programmable Frequency Reference

Device: Silicon Labs Si571 Any-Rate VCXO
Frequency Range: 10-945, 970-1134, 1213-1417.5 MHz
Start-Up Freq: 100 MHz
Freq Resolution: 0.09 ppb

Gates

Quantity: Two separate gates: Gate A for A/D; Gate B for D/A
Gate Sources: Selectable from external or internal gate
External: (see External Gate / Trigger / Sync / PPS Input) or Sync Bus CML Gate
Internal: Generated from programmable register
Gate Polarity: Programmable polarity for external as well as internal gate
Triggering: Programmable trigger length

Syncs

Quantity: Two separate syncs: Sync A for A/D; Sync B for D/A
Sync Source: Selectable from external or internal sync
External: (see External Gate / Trigger / Sync / PPS Input) or Sync Bus CML Sync
Internal: Generated from programmable register
Sync Pulse Width: 2 clock cycles, minimum
Sync Pulse Edge: Programmable selection of either rising edge or falling edge

Field-Programmable Gate Arrays (FPGA)

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Configuration: IP Cores factory-programmed by Pentek

FPGA MGT Clock Generator

Device: Silicon Labs Si5341B Any-Rate Clock Generator
Type: 10 separate programmable clock outputs
Frequency Range: 100 Hz to 350 MHz

RAM memory

Size: 5 Gigabytes of DDR4 SDRAM
Speed: 1200 MHz (2400 MHz DDR)
Bus Width: 80 bits

Configuration FLASH memory

Size: 1 Gigabit
Bus Width: 16 bits

Temperature and Voltage Sensors

PCB Temperature
Quantity: Four temperature sensors
Controller: Texas Instruments LM95234
PCB Power
Quantity: Four voltage inputs (two for 3.3V, two for 12V)
Controller: Linear Technology LTC2990

PCB Voltage

Quantity: Five voltage sensors
Controller: Kintex UltraScale System Monitor

PCI Express Interface

PCI Express: Gen. 1, 2 or 3: x4 or x8

Lanes/Speed: Gen1 x8 - 2 GB/sec
Gen2 x8 - 4 GB/sec
Gen3 x8 - 8 GB/sec

OpenVPX Profile

The 54141 is compatible with multiple OpenVPX profiles. Profile for standard and Option -109 shown below, contact Pentek for other optional profiles.

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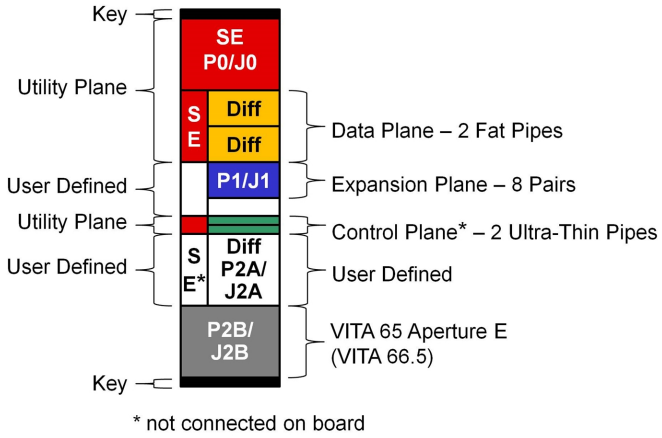

* not connected on board

Environmental

Standard: L0 (Air-cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (Air-cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Sine Vibration: 2g, 20-500 Hz
Random Vibration: 0.04g2/Hz, 20-2000 Hz
Shock: 20g, 11ms
Relative Humidity:
No conformal coating: 0% to 95% non-condensing
Conformal coating (Option -720): 0% to 100% non-condensing
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Sine Vibration: 10g, 20-2000 Hz
Random Vibration: 0.1g2, 20-2000 Hz
Shock: 30g, 11mS
Relative Humidity:
No conformal coating: 0% to 95% non-condensing
Conformal coating (Option -720): 0% to 100% non-condensing

Physical

Dimensions: 3U VPX board
Depth: 170.61 mm (6.717 in)
Height: 100 mm (3.937 in)

Weight: Approximately 14 oz (400 grams), with Option -730: 2-slot heatsink

Ordering Information

Model	Description
54141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - VPX

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-109	VITA 66.5: Optical 4X duplex lanes
-112	VITA 67.3C: RF In, RF Out and Sample Clock/Reference Clock In
-201	5-3 GHz input transformer
-249	VITA 49-2 support
-702	Air-cooled, Level L2
-763	Conduction-cooled, Level 3

Contact Pentek for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Storage and general options may change, so be sure to contact Pentek for the latest information.

Accessory Products

Model	Description
2171	Cable Kit: SSMC to SMA
5292	High-Speed System Synchronization and Distribution Amplifier - 3U VPX

SPARK Development Systems

The Pentek SPARK® systems are fully-integrated development systems for Pentek software radio, data acquisition, and I/O boards. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

The following SPARK systems are available for Pentek's Cobalt®, Onyx®, and Jade® boards: PCIe (Model 8266), 3U OpenVPX (Model 8267) and 6U OpenVPX (Model 8264). For Flexor boards, SPARK systems are available in PCIe (Model 8266) and 3U VPX (Model 8267).

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

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Upper Saddle River, NJ 07458 USA
Tel: +1 (201) 818-5900
Email: sales@pentek.com

Lifetime Applications Support

Pentek offers the worldwide military embedded computing community shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of Pentek's 30 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

54141 Configuration Modes

Pentek's Model 54141A is capable of operating in the configurations listed below. Certain sampling rate ranges during independent as well as simultaneous A/D and D/A operation are not achievable due to the clocking limitations of the JESD204B interface. The Navigator BSP automatically selects the most appropriate ADC and DAC JESD modes based on the arguments supplied to the API routines. Parameters such as clock frequency, sample width and real/complex data are used while making the decision.

ADC Standalone Operation

Resolution	Real or Complex	Number of Channels	Sample Rate	Digital Downconverter
8-bit	real	2 CH	800 to 3200 MSPS	bypass
8-bit	real	1 CH	1600 to 6400 MSPS	bypass
16-bit	real	2 CH	800 to 3200 MSPS	bypass
16-bit	real	1 CH	1600 to 6400 MSPS	bypass
16-bit	complex	2 CH	800 to 3200 MSPS	decimate by 4
16-bit	complex	2 CH	800 to 3200 MSPS	decimate by 8
16-bit	complex	2 CH	800 to 3200 MSPS	decimate by 16

DAC Standalone Operation

Resolution	Real or Complex	Number of Channels	Sample Rate	Digital Downconverter
8-bit	real	1 CH	1600 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 1 interpolate by 1
16-bit	real	2 CH	400 to 2500 MSPS 2500 to 3200 MSPS*	interpolate by 1 interpolate by 1
16-bit	real	2 CH	800 to 3200 MSPS 5240 to 6400 MSPS*	interpolate by 2 interpolate by 2
16-bit	real	2 CH	1600 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 4 interpolate by 4
16-bit	complex	1 CH	400 to 2500 MSPS 2500 to 3200 MSPS*	interpolate by 1 interpolate by 1
16-bit	complex	1 CH	800 to 3200 MSPS 5240 to 6400 MSPS*	interpolate by 2 interpolate by 2
16-bit	complex	1 CH	1600 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 4 interpolate by 4
16-bit	complex	2 CH	1200 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 6 interpolate by 6
16-bit	complex	2 CH	1600 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 8 interpolate by 8
16-bit	complex	2 CH	2000 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 10 interpolate by 10
16-bit	complex	2 CH	2400 to 3200 MSPS 5240 to 6400 MSPS	interpolate by 12 interpolate by 12
16-bit	complex	2 CH	3200 MSPS 5240 to 6400 MSPS	interpolate by 16 interpolate by 16
16-bit	complex	2 CH	5240 to 6400 MSPS	interpolate by 18
16-bit	complex	2 CH	5240 to 6400 MSPS	interpolate by 24

NOTE: *Theses modes have an input resolution of 12 bits to achieve higher sample rates.

Record/Playback Scenario, ADC and DAC Operating in Complementary Configurations (but not simultaneously)

Resolution	Real or Complex	Number of Channels	Sample Rate	Digital Downconverter
8-bit	real	1 CH	1600 to 3200 MSPS 5240 to 6400 MSPS	bypass bypass
16-bit	real	2 CH	800 to 2500 MSPS 2500 to 3200 MSPS*	bypass bypass
16-bit	complex	1 CH	1600 to 3200 MSPS	int/dec by 4
16-bit	complex	2 CH	1600 to 3200 MSPS	int/dec by 8
16-bit	complex	2 CH	3200 MSPS*	int/dec by 16

Full-Duplex Transceiver Scenario, ADC and DAC Operating Simultaneously in Complementary Configurations

Resolution	Real or Complex	Number of Channels	Sample Rate	Digital Downconverter
8-bit	real	1 CH	5240 to 6400 MSPS	bypass
16-bit	real	2 CH	800 to 1000 MSPS 1600 to 2000 MSPS 2500 to 3200 MSPS	bypass bypass bypass
16-bit	complex	1 CH	1600 to 3200 MSPS	int/dec by 4
16-bit	complex	2 CH	1600 to 3200 MSPS	int/dec by 8
16-bit	complex	2 CH	3200 MSPS	int/dec by 16
16-bit	complex	2 CH	3200 MSPS* 6400 MSPS*	dec. by 8 int by 16