

New!

# Model 53761

# 4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX



Model 53761 COTS (left) and rugged version



### Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

### General Information

Model 53761 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53761 includes an optional connection to the Virtex-7 FPGA for custom I/O.

### The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

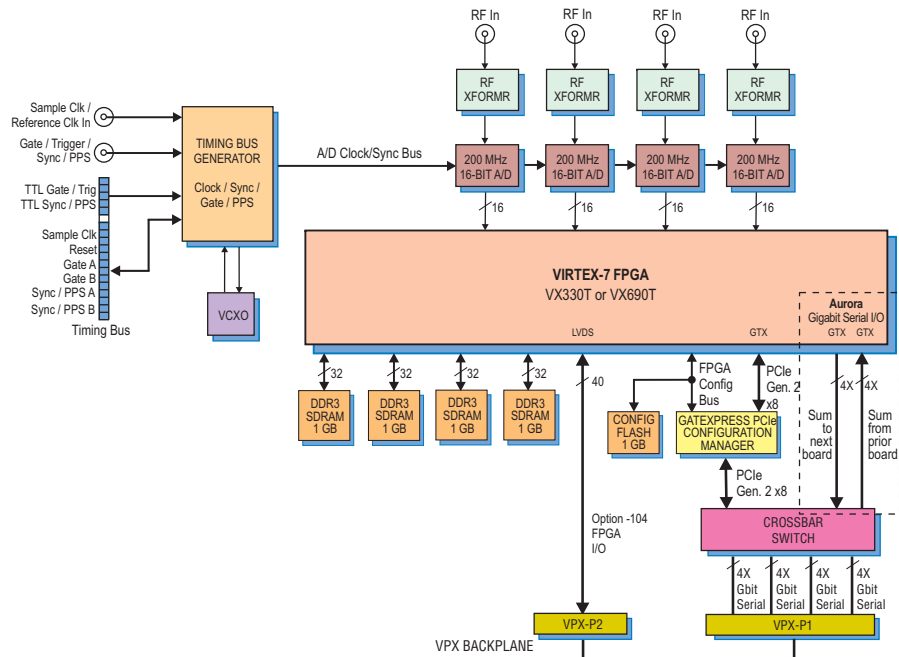
### Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



**A/D Acquisition IP Modules**

The 53761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

**Beamformer IP Core**

In addition to the DDCs, the 53761 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation

change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53761's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

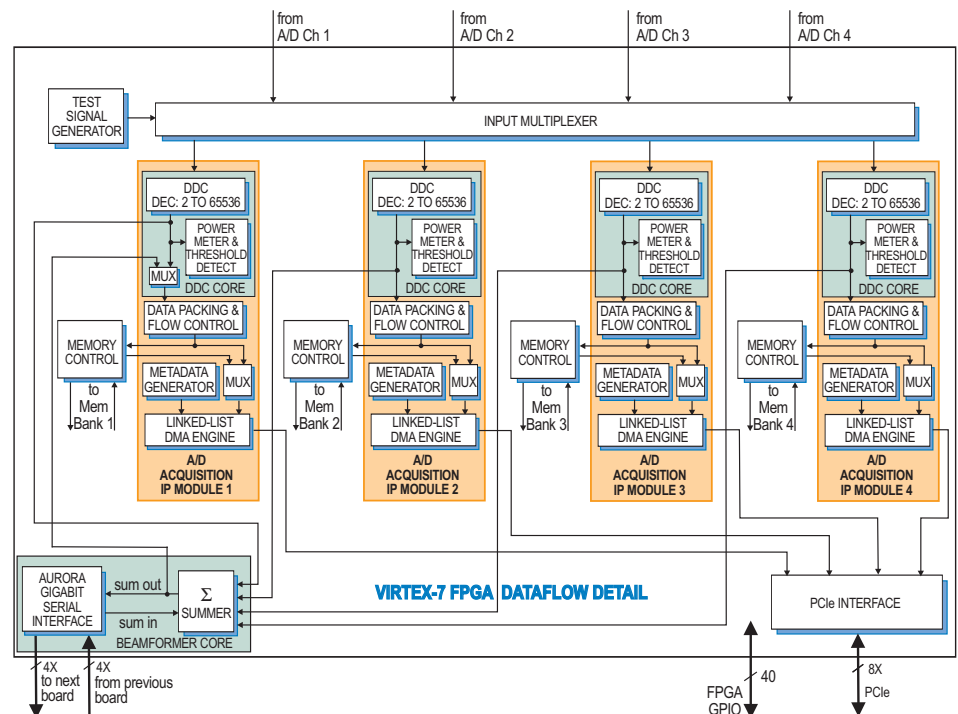
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_{sr}$  where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536



► FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

### A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

### Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous

sampling and sync functions across all connected boards.

### Memory Resources

The 53761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

### PCI Express Interface

The Model 53761 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Crossbar Switch

The 53761 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. ►

► Specifications

Front Panel Analog Signal Inputs

**Input Type:** Transformer-coupled, front panel female SSMC connectors  
**Transformer Type:** Coil Craft WBC4-6TLB  
**Full Scale Input:** +8 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

**Type:** Texas Instruments ADS5485  
**Sampling Rate:** 10 MHz to 200 MHz  
**Resolution:** 16 bits

Digital Downconverters

**Quantity:** Four channels  
**Decimation Range:** 2x to 65,536x in two stages of 2x to 256x  
**LO Tuning Freq. Resolution:** 32 bits, 0 to  $f_s$   
**LO SFDR:** >120 dB  
**Phase Offset Resolution:** 32 bits, 0 to 360 degrees

**FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients  
**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer

**Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain  
**Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol  
**Phase Shift Coefficients:** I & Q with 16-bit resolution  
**Gain Coefficients:** 16-bit resolution  
**Channel Summation:** 24-bit  
**Multiboard Summation Expansion:** 32-bit

**Sample Clock Sources:** On-board clock synthesizer

Clock Synthesizer

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus  
**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz  
**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

**Type:** Front panel female SSMC connector, LVTTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

**Standard:** Xilinx Virtex-7 XC7VX330T-2  
**Optional:** Xilinx Virtex-7 XC7VX690T-2

**Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory

**Type:** DDR3 SDRAM  
**Size:** Four banks, 1 GB each  
**Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface

**PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental

**Operating Temp:** 0° to 50° C  
**Storage Temp:** -20° to 90° C  
**Relative Humidity:** 0 to 95%, non-cond.  
**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



Ordering Information

Model	Description
53761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:

-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

VPX Families

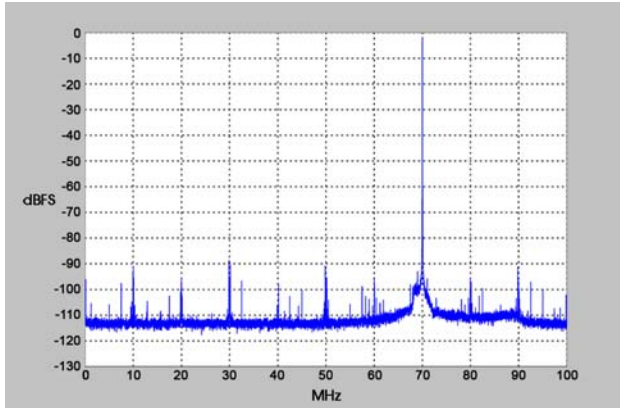
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

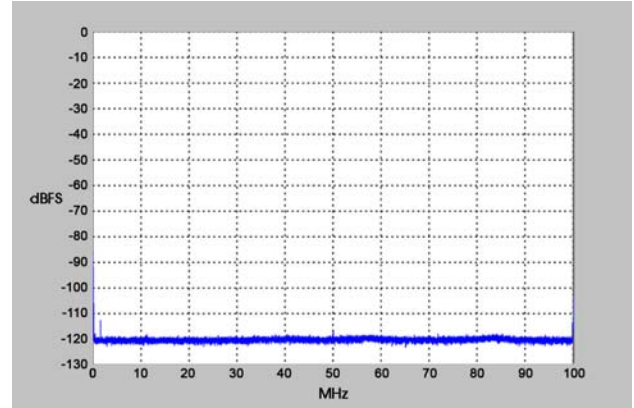
A/D Performance

Spurious Free Dynamic Range



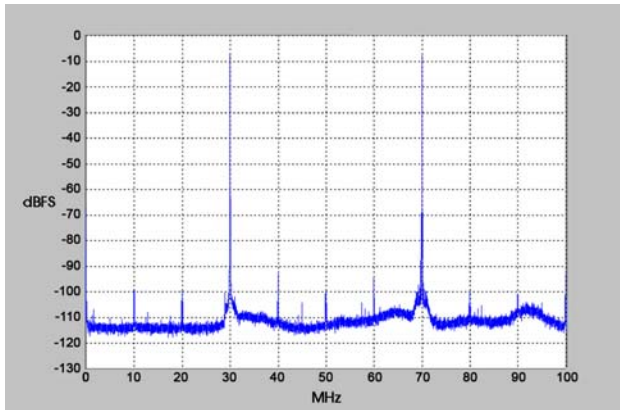
$f_{in} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Internal Clock

Spurious Pick-up



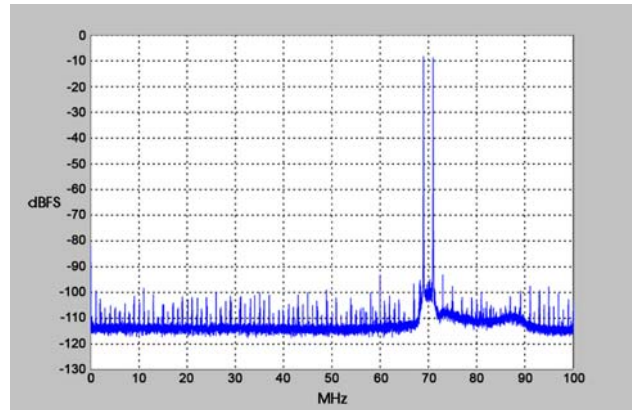
$f_s = 200 \text{ MHz}$ , Internal Clock

Two-Tone SFDR



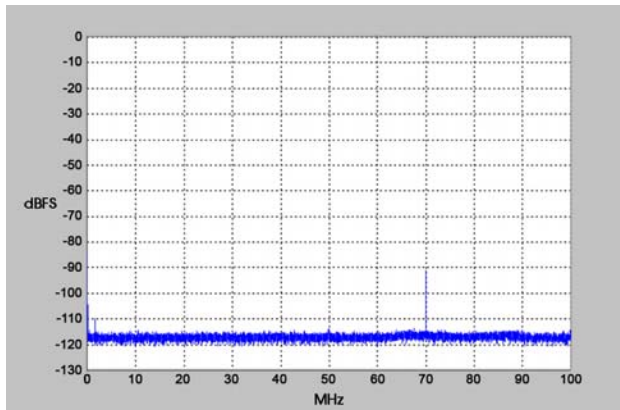
$f_1 = 30 \text{ MHz}$ ,  $f_2 = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

Two-Tone SFDR



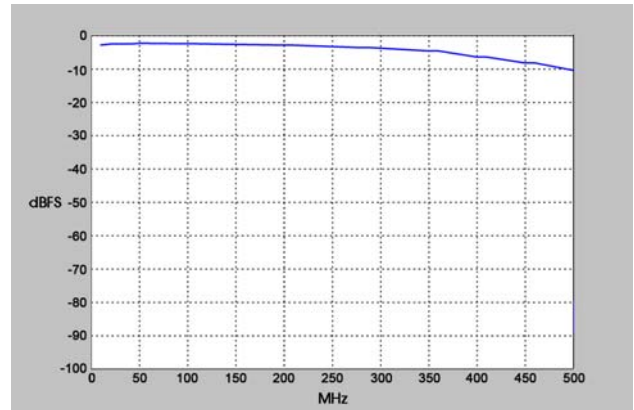
$f_1 = 69 \text{ MHz}$ ,  $f_2 = 71 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Ch 1 shown

Input Frequency Response



$f_s = 200 \text{ MHz}$ , Internal Clock