General Information

The Flexor™ Model 3320 is a multi-channel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel count-systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3320 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

Performance of the Model 3320

The true performance of the 3320 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

A/D and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual-channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the 4th page for supported modes.
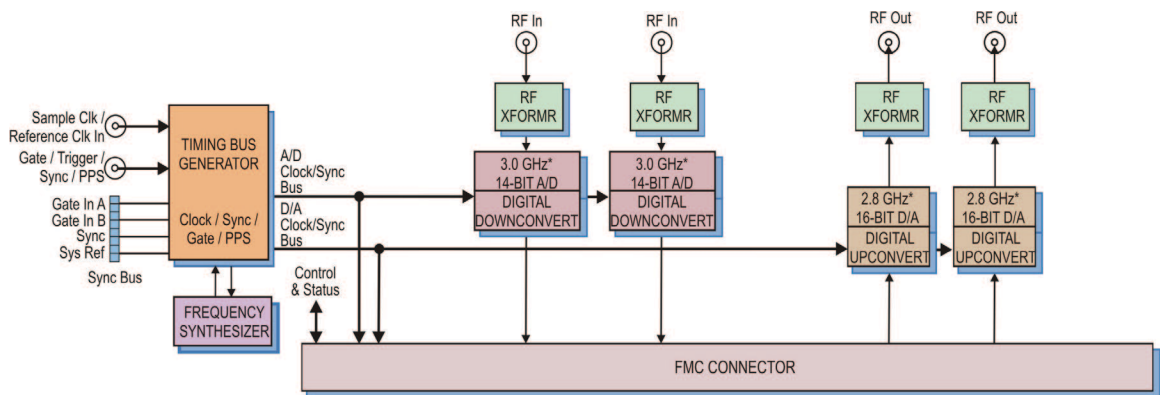
A/D Acquisition IP Modules

With the 3320 installed on a Pentek FMC carrier, the FlexorSet features two A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A wave-form generator IP modules in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data. ➤

Features

- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital upconverters
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available

* See page 4 for configuration profiles

➤ Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital up-con-verters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with Pentek's FMC carriers, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements.

Board Support Packages

Pentek's BSPs provide control of all the 3320's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a powerful, quick-start platform to create custom applications. BSPs are compatible with Windows and Linux operating systems. ReadyFlow BSP is used with OnyxFX Virtex-7 FPGA carriers and Navigator BSP is used for all new development going forward including the JadeFX Kintex Ultrascale carriers.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the development kit to completely replace the Pentek IP with their own.

GateFlow is used with OnyxFX Virtex-7 FPGA carriers and Navigator FDK is used for all new FPGA development going forward including the JadeFX Kintex UltraScale carriers.

FMC Interface

The Model 3320 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier. ➤

SPARK Development Systems

SPARK systems are fully-integrated saving engineers and system integrators the time and expense associated with building and testing a development system. SPARK systems ensure the optimum performance of Pentek boards and are available in 3U VPX **(Model 8267)** and in a PC environment **(Model 8266)**.

➤ Model 3320 Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Mini-Circuits TC1-1-13M
Full Scale Input: +6.6 dBm into 50 ohms
3 dB Passband: 4.5 to 3000 MHz

A/D Converters
Type: Texas Instruments ADC32RF45
Sampling Rate and Resolution: See table next page

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Coil Craft WBC4-14L
Full-Scale Output: +4 dBm into 50 ohms
3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
Type: Texas Instruments DAC39J84
Sampling Rate and Resolution: See table next page

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator

Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
Type: Front panel SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
3320	2-Channel 3.0 GHz A/D with DDCs and 2-Channel 2.8 GHz D/As with DUCs

Options:

3320-990	Reference design for 3320 installed on Xilinx VC707 Evaluation Kit

3U FlexorSet Description

5973-320	2-Channel 3 GHz A/D, 2-Channel 2.8 GHz D/A Virtex-7 FPGA with DUCs
5983-320	2-Channel 3 GHz A/D, 2-Channel 2.8 GHz D/A Kintex UltraScale FPGA with DUCs

PCIe FlexorSet Description

7070-320	2-Channel 3 GHz A/D, 2-Channel 2.8 GHz D/A, Virtex-7 FPGA with DUCs -x8

Contact Pentek for availability of rugged and conduction-cooled versions and other support options

➤

➤ Preconfigured Modes

When the Model 3320 is part of a FlexorSet, it is delivered with a set of six pre-configured modes. These allow users to easily select A/D and D/A settings that are commonly used in many applications. While these modes typically satisfy many applications, users can always configure the A/D and D/A settings to their specific requirements via the PCIe interface using the ReadyFlow Board Support Package.

Pre-configured Conversion Modes

mode	A/D Converter							D/A Converter					
	sample rate	DDC or bypass	output bits resolution	output bandwidth	real or complex	output data rate/chan	usable bandwidth	sample rate	DUC or bypass	input bits resolution	real or complex	input data rate/chan	usable bandwidth
1	3.0 GHz	dec = 4	16 I + 16 Q	600 MHz	complex	3.0 GB/sec	600 MHz	-	-	-	-	-	-
2	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz	2.8 GHz	int = 2	16 I + 16 Q	complex	5.6 GB/sec	1120 MHz
3	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz	2.8 GHz	int = 4	16 I + 16 Q	complex	2.8 GB/sec	560 MHz
4	2.5 GHz	bypass	12	2.5 GHz	real	5.0 GB/sec	1000 MHz	-	-	-	-	-	-
5	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz	2.0 GHz	int = 2	16 I + 16 Q	complex	4.0 GB/sec	800 MHz
6	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz	2.0 GHz	int = 2	16	real	2.0 GB/sec	400 MHz

Rationale for Each Mode

Mode 1: Maximum A/D sample rate of 3 GS/s, but the DDC must be used. D/A cannot operate at this sample rate.

Mode 2: Maximum sample rate for A/D and D/A both operating. DDC and DUC must be used, but D/A can generate twice the bandwidth of the A/D bandwidth.

Mode 3: Maximum sample rate for A/D and D/A both operating (like Mode 2), but now A/D and D/A bandwidths are the same

Mode 4: Maximum A/D useable bandwidth achieved with DDC bypass (RAW) output data and 12 bit resolution. D/A cannot operate in this mode.

Mode 5: Maximum useable signal bandwidth with A/D and D/A both operating. A/D is in bypass with 14-bit resolution. D/A uses DUC with interpolation of 2.

Mode 6. Like Mode 5 except D/A interpolates real samples instead of complex samples resulting in 400 MHz bandwidth and a simpler output anti-aliasing filter

General Notes

1. "Useable bandwidth" is equal to 80% of the Nyquist bandwidth.

2. Anti-aliasing filters are required for A/D inputs and D/A outputs to ensure elimination of unwanted out-of-band signals per Nyquist criteria.

3. Data rates shown are for the interfaces between the FMC module and the FPGA of the FMC carrier for each channel..

4. By changing board-support software, other operating modes are possible, including different decimations and interpolation.

5. The sample rates shown for each mode are the maximum rates for that mode, but lower rates are also supported with other parameters scaled appropriately.

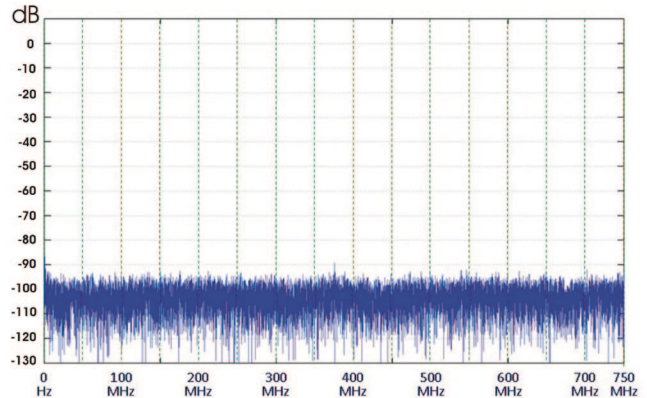6. Only one mode is allowed at a time, which defines operations for both A/D and D/A.

➤

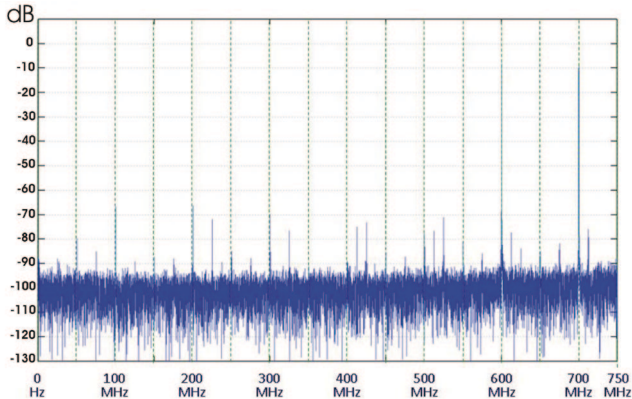## Model 3320 Typical Performance

Spurious Free Dynamic Range
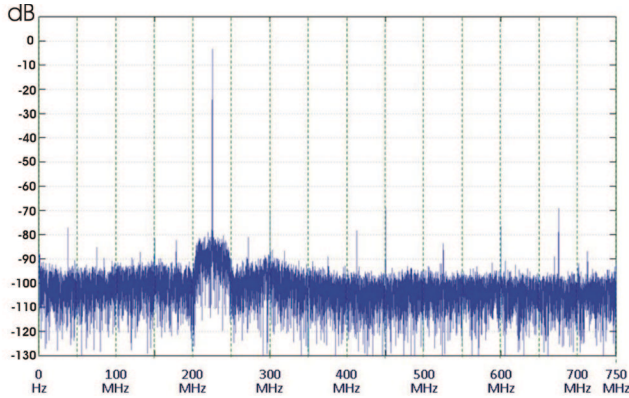
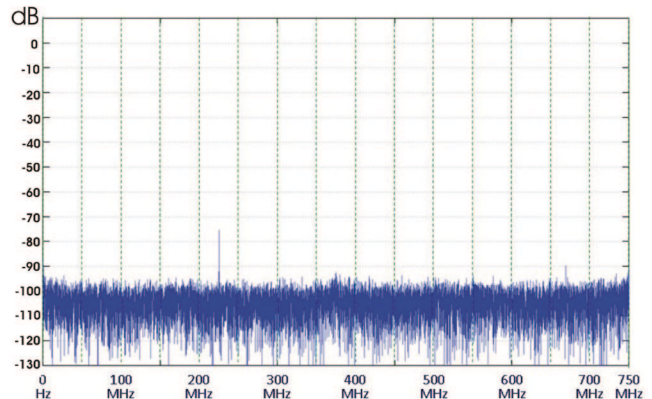

$f_s = 1.5$ GHz, $f_{in} = 225$ MHz

Spurious Pick-up

$f_s = 1.5$ GHz, Internal Clock

Two-Tone SFDR

$f_s = 1.5$ GHz, $f_1 = 800$ MHz, $f_2 = 900$ MHz

ADC Interchannel Crosstalk

$f_s = 200$ MHz, $f_1 = 225$ MHz on aggressor channel,

DDC Performance
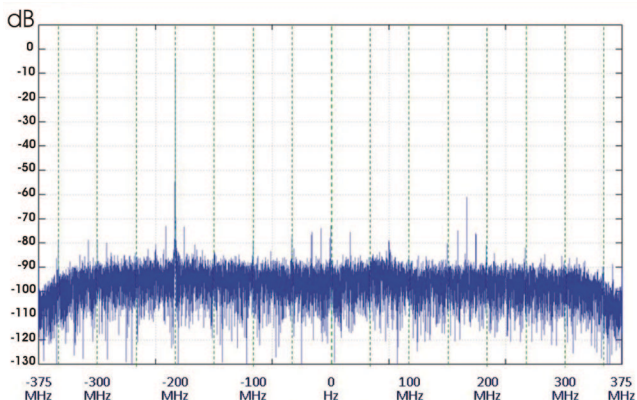
$f_s = 3.0$ GHz, $f_{tune} = 1000$ MHz, $f_{in} = 800$ MHz,
Decimation = 4

DAC SFDR
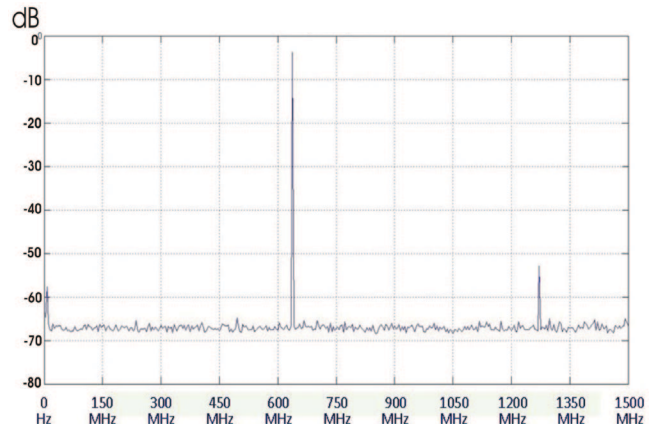
$f_s = 2.5$ GHz, $f_{out} = 629$ MHz

Pentek FlexorSet Models					
Form Factor	FPGA Type Development Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				5973-313	As above with 4 multiband DDCs & interpolation filters
			3316	5973-316	8 Ch 250 MHz 16-bit A/D
				5973-317	As above with 8 multiband DDCs
			3320	5973-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5973-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
	Kintex UltraScale Navigator BSP Navigator FDK Vivado	5983	3312	5983-313	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317	8 Ch 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5983-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
PCIe	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				7070-313	As above with 4 multiband DDCs & interpolation filters
			3316	7070-316	8 Ch 250 MHz 16-bit A/D
				7070-317	As above with 8 multiband DDCs
			3320	7070-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	7070-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A

Model 5973-320

General Information

Model 5973 is a member of the OnyxFX© family of high-performance 3U VPX base-boards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5973-320 FlexorSet™ combines the Model 5973 and the Model 3320 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.
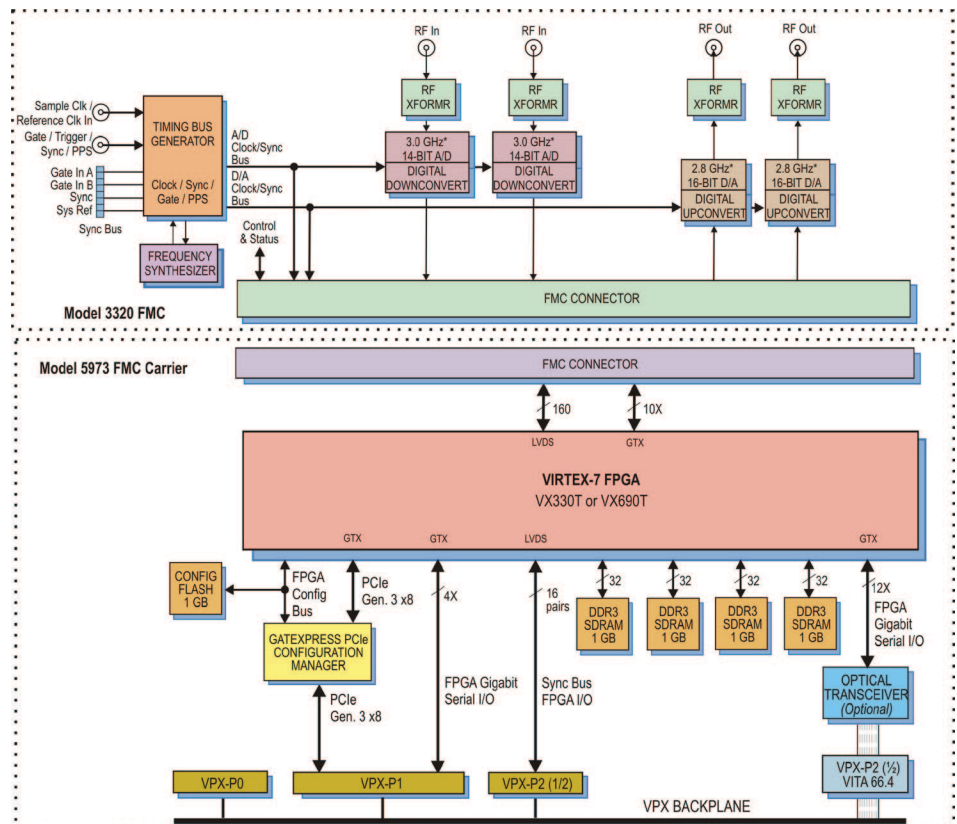
The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplex-ing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplify-ing data capture and data transfer.

Each of the acquisition IP modules contains IP for DDR3 SDRAM memories.

The 5973-320 features two sophisticated D/A waveform generator IP modules. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. In each generator module, up to 64 indi-vidual link entries can be chained together to create complex waveforms with a minimum of programming. ➤

Features

- Includes Xilinx Virtex-7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Virtex-7 FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

A/D Acquisition IP Modules

The 5973-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Modules

The 5973-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for synchronization and custom I/O.
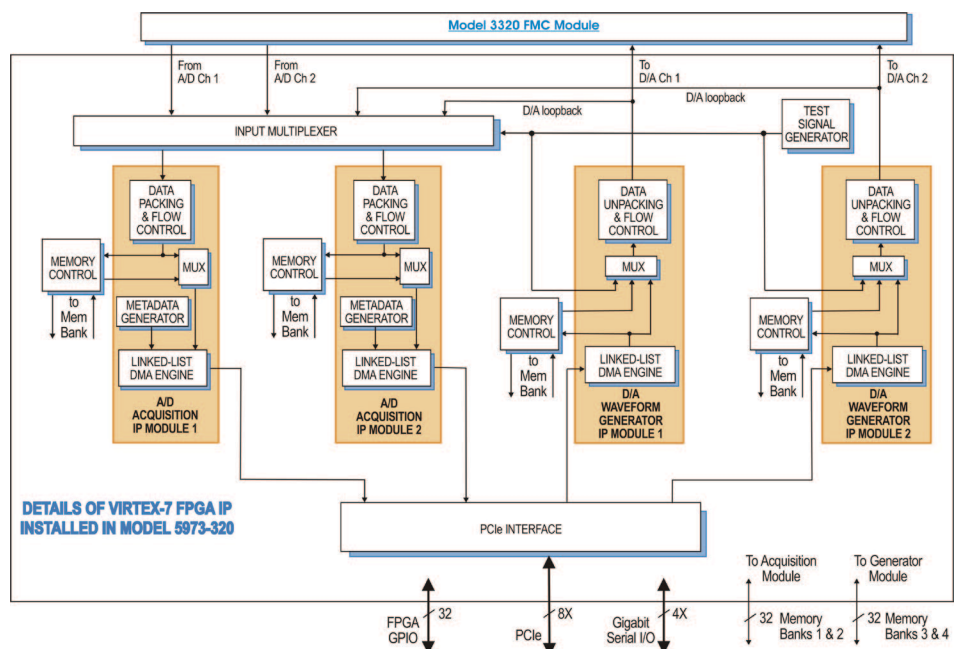
Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. ➤

DETAILS OF VIRTEX-7 FPGA IP INSTALLED IN MODEL 5973-320

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK
Development Systems

➤ The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 5973-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 5973-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Down-con-verter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The architecture includes a timing bus generator responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements. ➤

➤ Specifications

Front Panel Analog Signal Inputs
  Input Type: Transformer-coupled, front panel SSMC connectors
  Transformer Type: Mini-Circuits TC1-1-13M
  Full Scale Input: +6.6 dBm into 50 ohms
  3 dB Passband: 4.5 to 3000 MHz

A/D Converters
  Type: Texas Instruments ADC32RF45
  Sampling Rate and Resolution: See the 3320 preconfigured modes table

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Coil Craft WBC4-14L
Full-Scale Output: +4 dBm into 50 ohms
3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
  Type: Texas Instruments DAC39J84
  Sampling Rate and Resolution: See the 3320 preconfigured modes table
Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
  Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
  Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
  Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
  Type: Front panel SSMC connector
  Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
  Standard: Xilinx Virtex-7 XC7VX330T-2
  Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
  4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
  Parallel: 16 pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for synchronization and custom I/O
  Optical (Option -110): User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
  Type: DDR3 SDRAM
  Size: Four banks, 1 GB each
  Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility:
  The Model 5973-320 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification: SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

Model	Description
5973-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:

-076	XC7VX690T-2 FPGA
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

Model 5983-320

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-320 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983

FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.
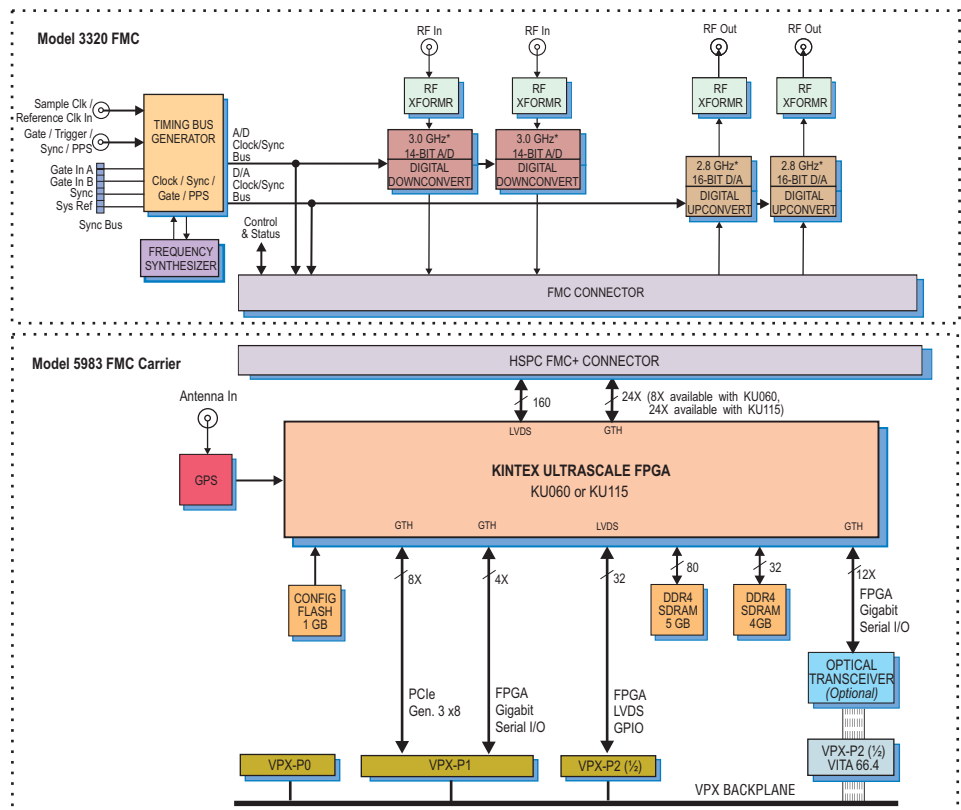
The 5983-320 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP. ➤

Features

- Supports Xilinx Kintex UltraScale FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

Model 5983-320

A/D Acquisition IP Modules

The 5983-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Modules

The 5983-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-320 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.
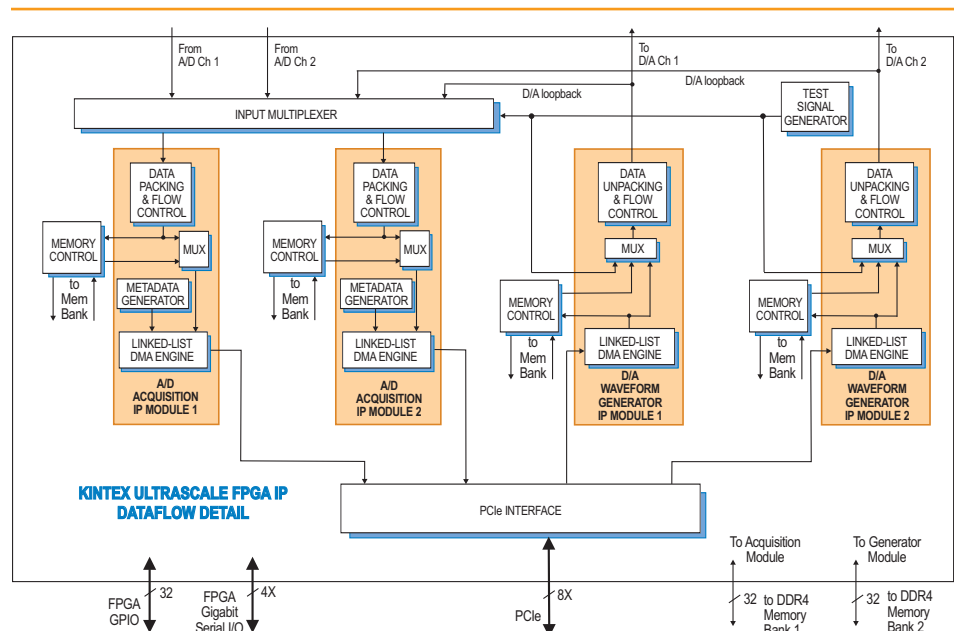
Memory Resources

The 5983-320 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Down-converter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the next page for supported modes.➤

KINTEX ULTRASCALE FPGA IP DATAFLOW DETAIL

➤ GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
   Input Type: Transformer-coupled, front panel SSMC connectors
   Transformer Type: Mini-Circuits TC1-1-13M
   Full Scale Input: +6.6 dBm into 50 ohms
   3 dB Passband: 4.5 to 3000 MHz
A/D Converters
   Type: Texas Instruments ADC32RF45
   Sampling Rate and Resolution: See the 3320 preconfigured modes table
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Coil Craft WBC4-14L
Full-Scale Output: +4 dBm into 50 ohms
3 dB Passband: 1.5 MHz to 1200 MHz
D/A Converters
   Type: Texas Instruments DAC39J84
   Sampling Rate and Resolution: See the 3320 preconfigured modes table
Sample Clock Sources: Timing bus generator provides A/D and D/A clocks
Timing Bus Generator
   Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
   Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference
External Clock
   Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
External Trigger Input
   Type: Front panel SSMC connector
   Function: Programmable functions include: trigger, gate, sync and PPS ➤

➤ **Field Programmable Gate Array**
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2
Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes
Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -763: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
OpenVPX Compatibility:
The Model 5983-320 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
5983-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:

-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options
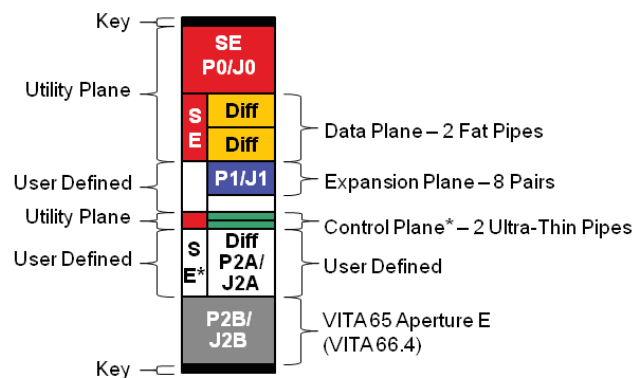
* not connected on board

General Information

Model 7070 is a member of the OnyxFX© family of high-performance PCIe baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 7070-320 FlexorSet™ combines the Model 7070 and the Model 3320 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and signal generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA- processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-320 includes optional copper and optical connections to the FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP for DDR3 SDRAM memories.

The 7070-320 features two sophisticated D/A waveform generator IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. ➤

Model 7070-320

Features

- Includes Xilinx Virtex-7 FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- LVDS connections to the Virtex-7 FPGA for custom I/O and synchronization
- Optional optical Interface for gigabit serial interboard communication
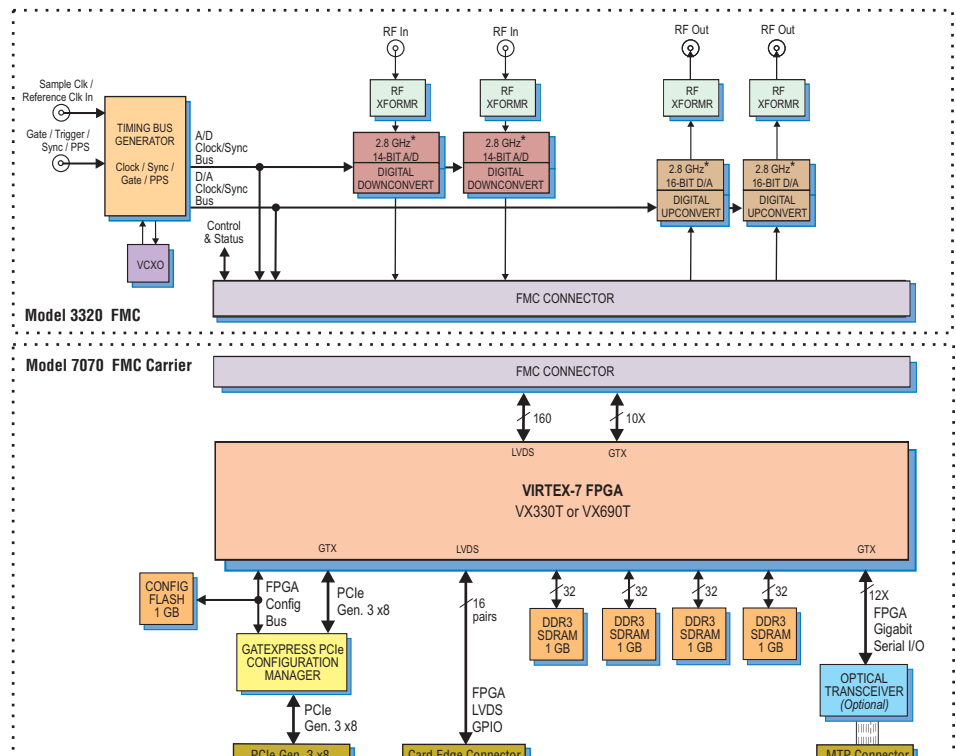
A/D Acquisition IP Modules

The 7070-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Modules

The 7070-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ In each generator module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and a card-edge connector for custom I/O.
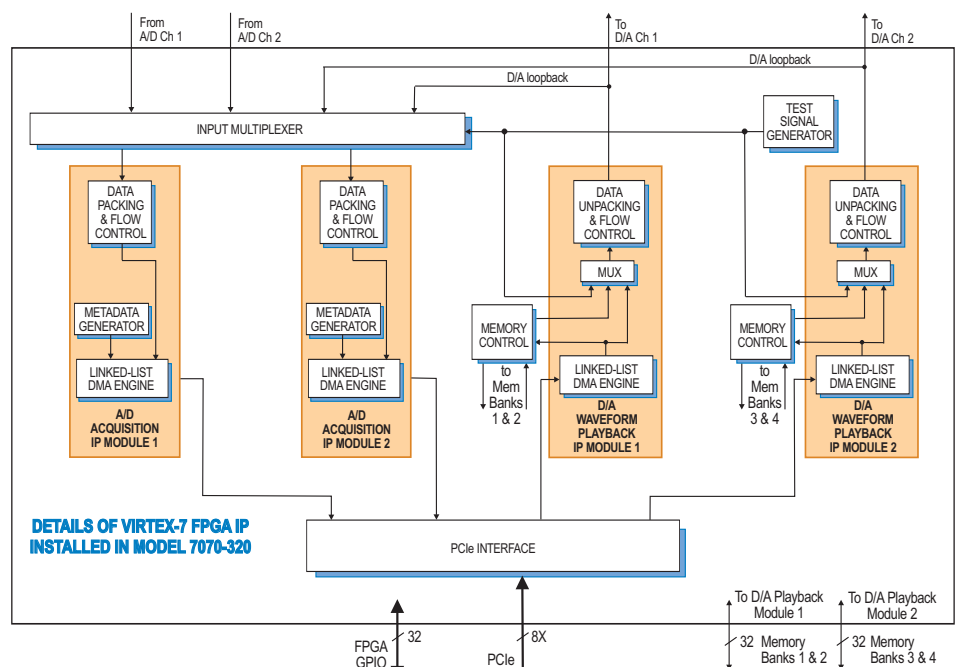
Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. ➤

DETAILS OF VIRTEX-7 FPGA IP INSTALLED IN MODEL 7070-320

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 7070-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 7070-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Down-converter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the tables on next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements. ➤

SPARK Development Systems

The Model 8266 is a fully-integrated PC development system for Pentek PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
7070-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe

Options:

-076	XC7VX690T-2 FPGA
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Mini-Circuits TC1-1-13M

Full Scale Input: +6.6 dBm into 50 ohms

3 dB Passband: 4.5 to 3000 MHz

A/D Converters

Type: Texas Instruments ADC32RF45

Sampling Rate and Resolution: See the 3320 preconfigured modes table

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters

Type: Texas Instruments DAC39J84

Sampling Rate and Resolution: See the 3320 preconfigured modes table

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator

Clock Source: Selectable from on-board frequency synthesizer or front panel external clock

Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock

Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input

Type: Front panel SSMC connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel: 16 pairs of LVDS connections are provided between the FPGA and a card-edge connector for custom I/O

Optical (Option -110): User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled

**Size:** 4.376 in. x 7.948 in (111.2 mm x 201.6 mm)

Features

- Supports the Xilinx Virtex-7 FPGA
- Complete development environment with Pentek's reference design
- Supports the Pentek Model 3320 FMC I/O Module

Pentek offers the option -990 reference design with software and IP support for the Pentek Model 3320 when installed on the Xilinx VC707 Evaluation Kit board.

The Virtex®-7 FPGA VC707 Evaluation Kit is a PCIe platform using the Virtex-7 XC7VX485T-2FFG1761C. It includes basic components of hardware, design tools, IP, and preverified reference designs.

When coupled with Pentek's option -990 reference design for the 3320, the user has a complete development environment for custom applications. The industry-standard FPGA Mezzanine Connectors (FMC) are directly compatible with the 3320.
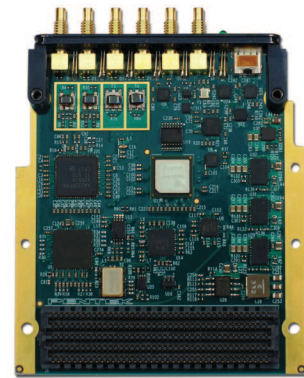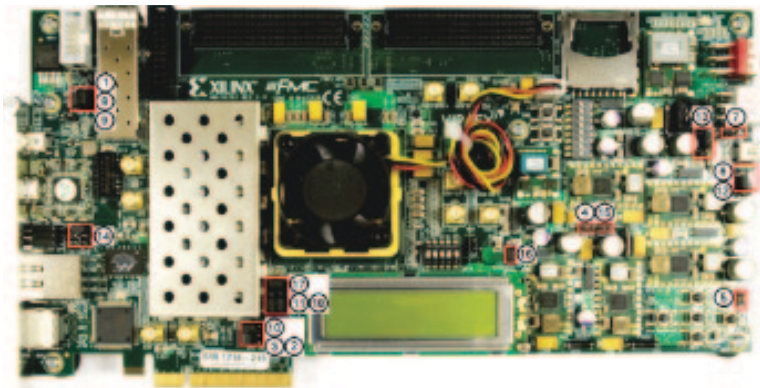
The Xilinx Virtex® -7 FPGA VC707 Evaluation Kit gives designers an easy starting point for evaluating and leveraging devices that deliver breakthrough performance, capacity, and power efficiency. Out of the box, this platform speeds time to market for the full-range of Virtex-7 FPGA-based applications including advanced systems for wired and wireless communications, aerospace and defense. The highly flexible kit combines fully integrated hardware, software, and IP with preverified reference designs that maximize productivity and let designers immediately focus on their unique project requirements.

The Flexor® Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

Ordering Information

Model	Description
3320-990	Reference Design for the Xilinx VC707 Evaluation Kit

Please purchase the Xilinx VC707 Evaluation Kit from your Xilinx authorized distributor:
https://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html