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Radar & SDR I/O

RADAR & SDR I/O - PMC/XMC

MODEL	DESCRIPTION
Cobalt 71620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC
Cobalt 71621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC
Cobalt 71624	Dual-Channel, 34-Signal Adaptive IF Relay - XMC
Cobalt 71630	1 GHz A/D and D/A, Virtex-6 FPGA - XMC
Cobalt 71640	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - XMC
Cobalt 71641	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Wideband DDC, Virtex-6 FPGA - XMC
Cobalt 71650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - XMC
Cobalt 71651	2-Chan 500 MHz A/D with DDC, DUC with 2-Chan 800 MHz D/A, Virtex-6 FPGA - XMC
Cobalt 71660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - XMC
Cobalt 71661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC
Cobalt 71662	4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - XMC
Cobalt 71663	1100-Channel GSM Channelizer with Quad A/D - XMC
Cobalt 71664	4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - XMC
Cobalt 71670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC
Cobalt 71671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC
Cobalt 71690	L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC
Onyx 71720	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - XMC
Onyx 71721	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - XMC
Onyx 71730	1 GHz A/D and D/A, Virtex-7 FPGA - XMC
Onyx 71741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC,Virtex-7 FPGA - XMC
Onyx 71751	2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - XMC
Onyx 71760	4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - XMC
Onyx 71761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - XMC
Onyx 71791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - XMC
Jade 71131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC
Jade 71132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC
Jade 71141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - XMC
Jade 71821	3-Channel 200 MHz A/D, DDC, DUC 2_Channel 800 MHz D/A, Kintex UltraScale FPGA - XMC
Jade 71841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - XMC
Jade 71851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - XMC
Jade 71861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - XMC
Jade 71862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - XMC
Jade 71800	Kintex UltraScale FPGA Coprocessor - XMC
Bandit 7120	2-Channel Analog RF Wideband Downconverter - PMC/XMC
8266	PC Development System for PCIe Cobalt, Onyx, Jade and Flexor Boards
	Customer Information

RADAR & SDR I/O - CompactPCI

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RADAR & SDR I/O - x8 PCI Express

RADAR & SDR I/O - 3U VPX - FORMAT 1

RADAR & SDR I/O - AMC

RADAR & SDR I/O - 3U VPX - FORMAT 2

RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated: March 2018

Model 71620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - XMC

General Information

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

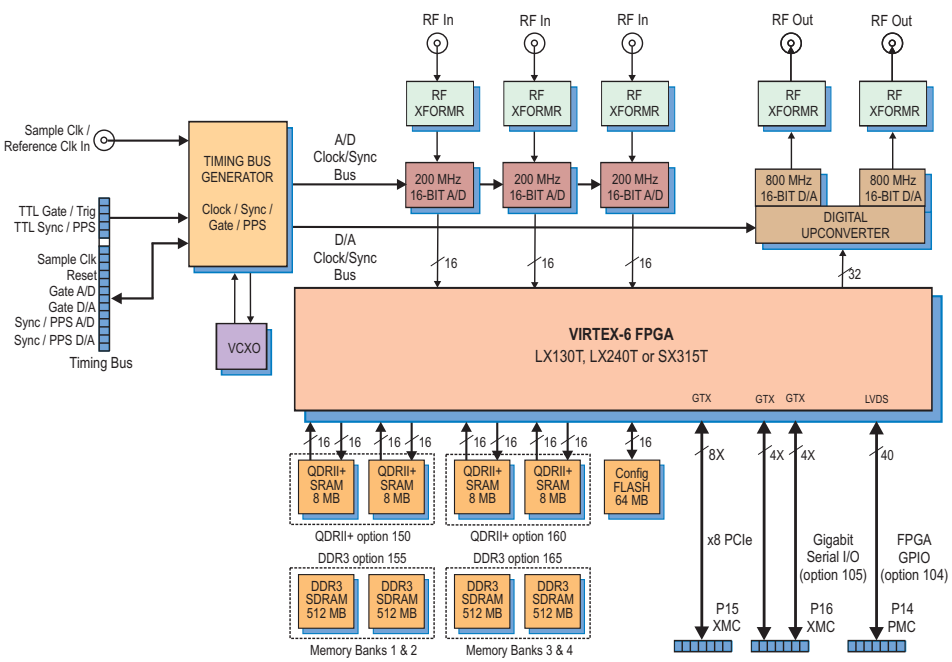
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

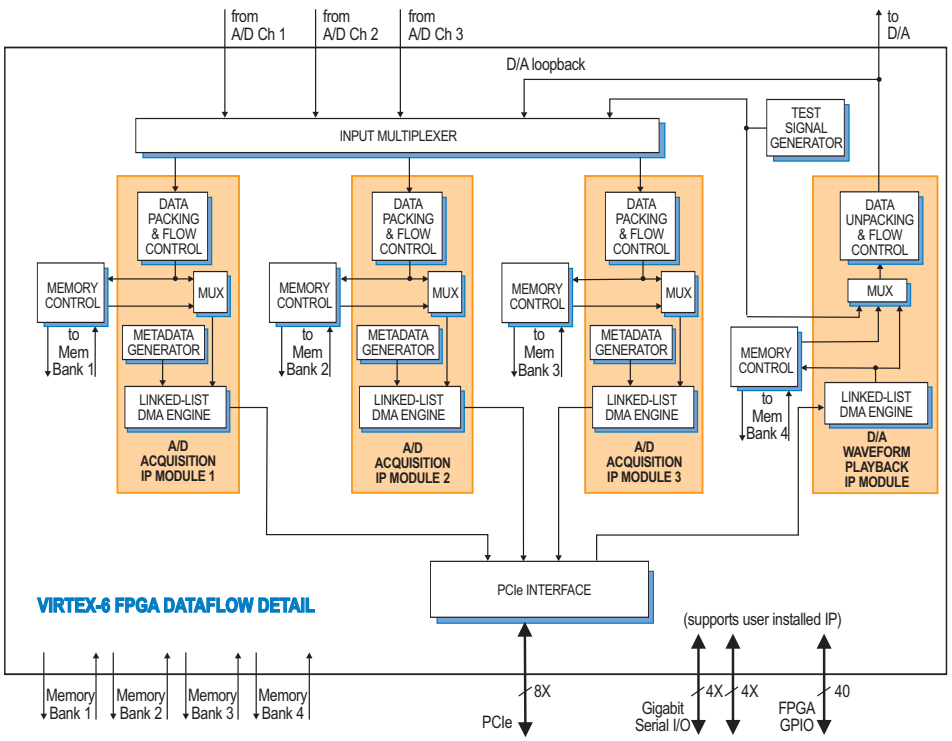
A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71620 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71620 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

General Information

Model 71621 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71621 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

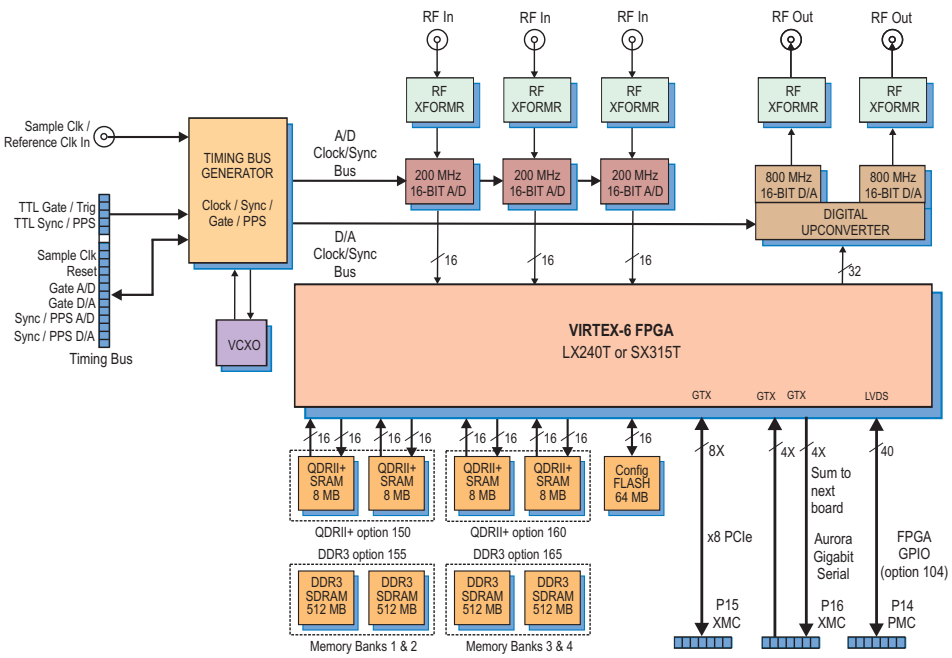
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 71621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

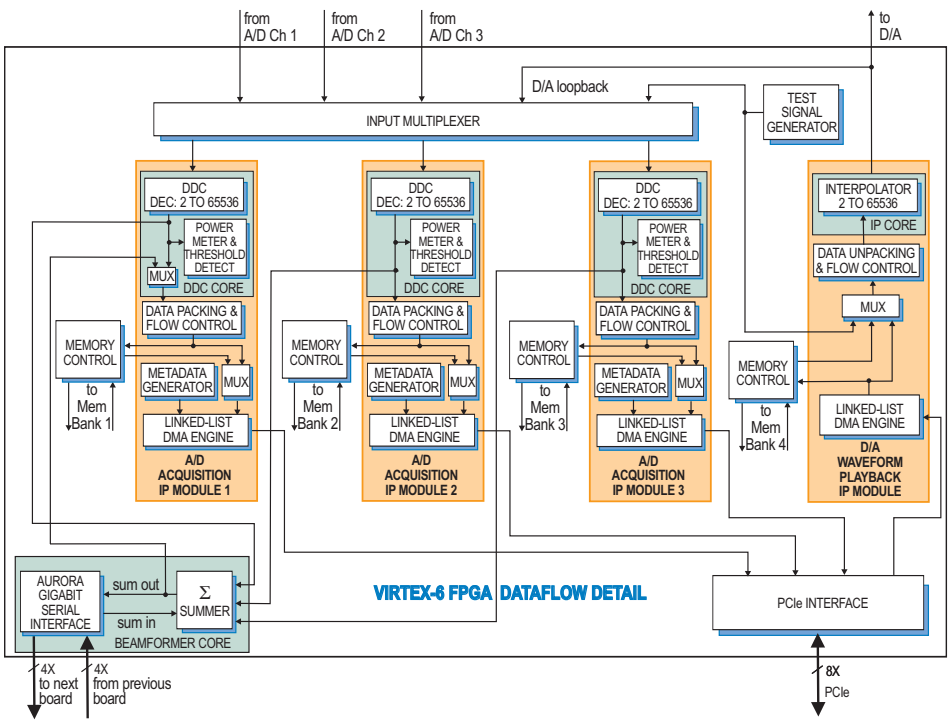
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71621 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71621 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple modules.

PCI Express Interface

The Model 71621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 71621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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New!

Model 71624

Dual-Channel, 34-Signal Adaptive IF Relay - XMC

Features

- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/As
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

General Information

Model 71624 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 71624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 71624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

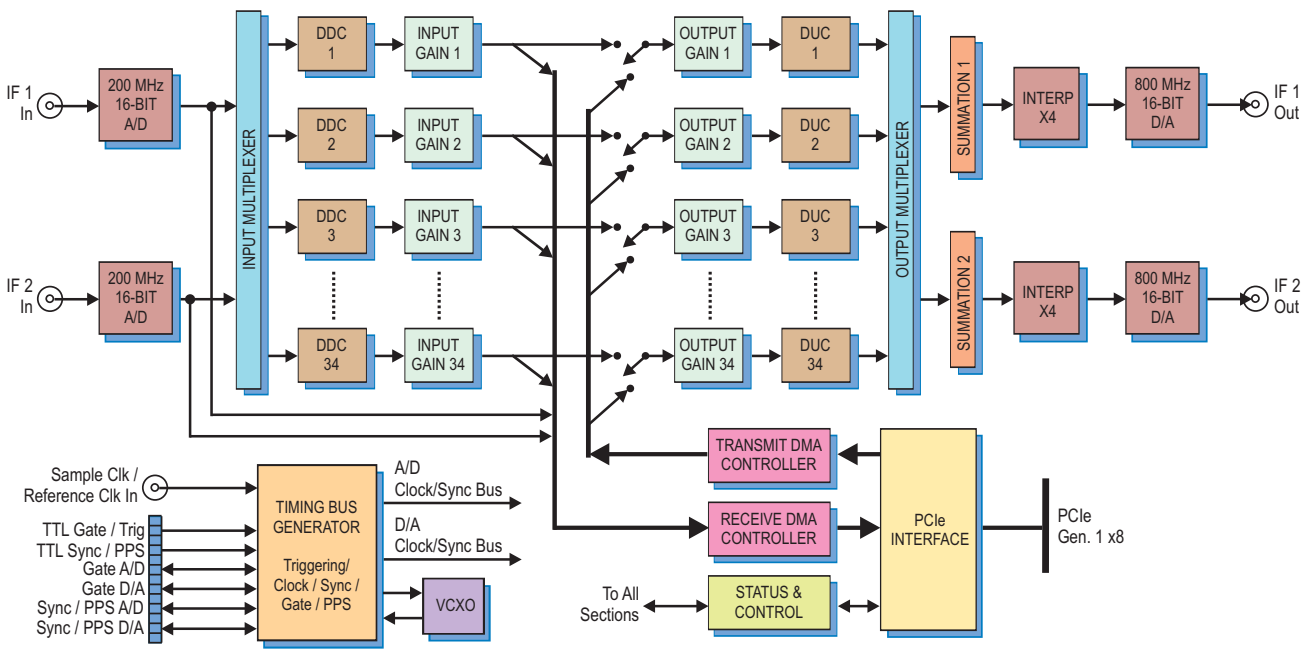
Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 71624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two summation blocks, each ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 71624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 71624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 71624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz. ➤

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71624's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

PCI Express XMC Interface

The Model 71624 complies with the VITA 42.0 XMC specification. The primary XMC connector on P15 supports an industry-standard interface fully compliant with PCIe Gen. 1 x8, bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the module.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

Model 71624 Dual-Channel, 34-Signal Adaptive IF Relay - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71624	Dual-Channel 34-Signal Adaptive IF Relay - XMC

Options:

-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
- **Quantity:** 34
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Required:** Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8;

Environmental

Standard:
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Option 702 L2 Extended Temp (air-cooled):
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-cond.

Option 712 L2 Extended Temp (conduction-cooled):
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

➤

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

General Information

Model 71630 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71630 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

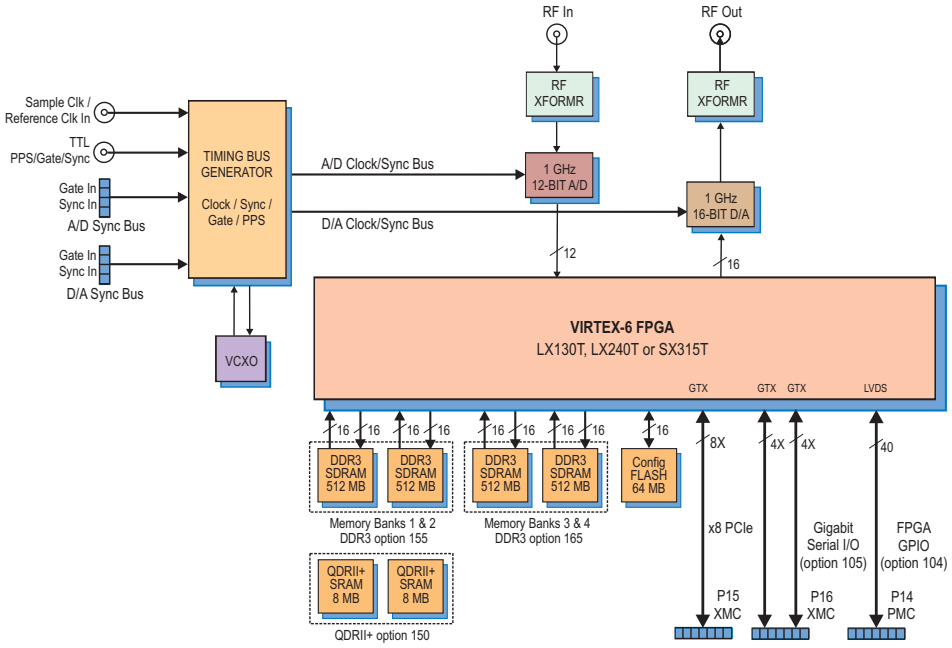
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 71630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

A/D Acquisition IP Module

The 71630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

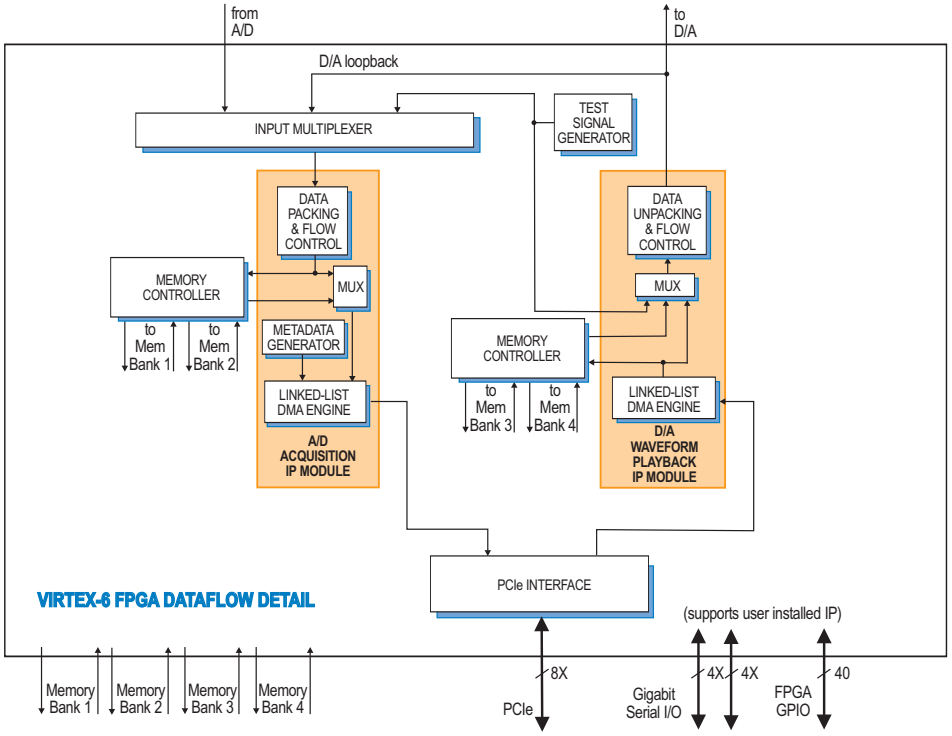
A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 71630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71630	1 GHz A/D and D/A, Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ XMC Interface

The Model 71630 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71630 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA
Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen.1: x4 or x8; Gen 2: x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC

General Information

Model 71640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71640 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

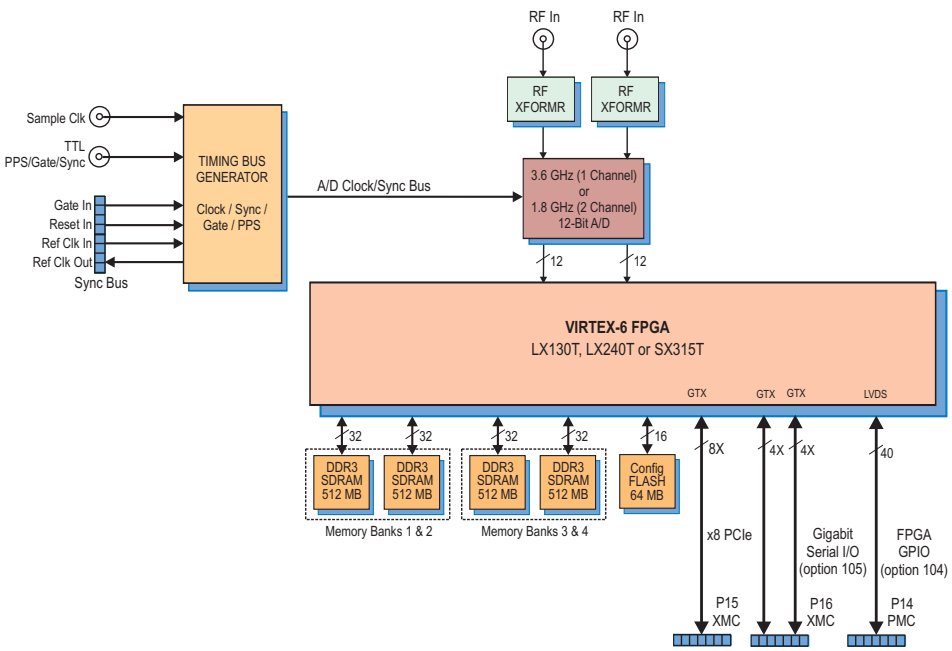
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multimodule synchronization
- PCI Express Gen. 2 interface x8 wide
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 71640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 71640s can be synchronized using the Cobalt high speed sync module to drive the sync bus.

Memory Resources

The 71640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

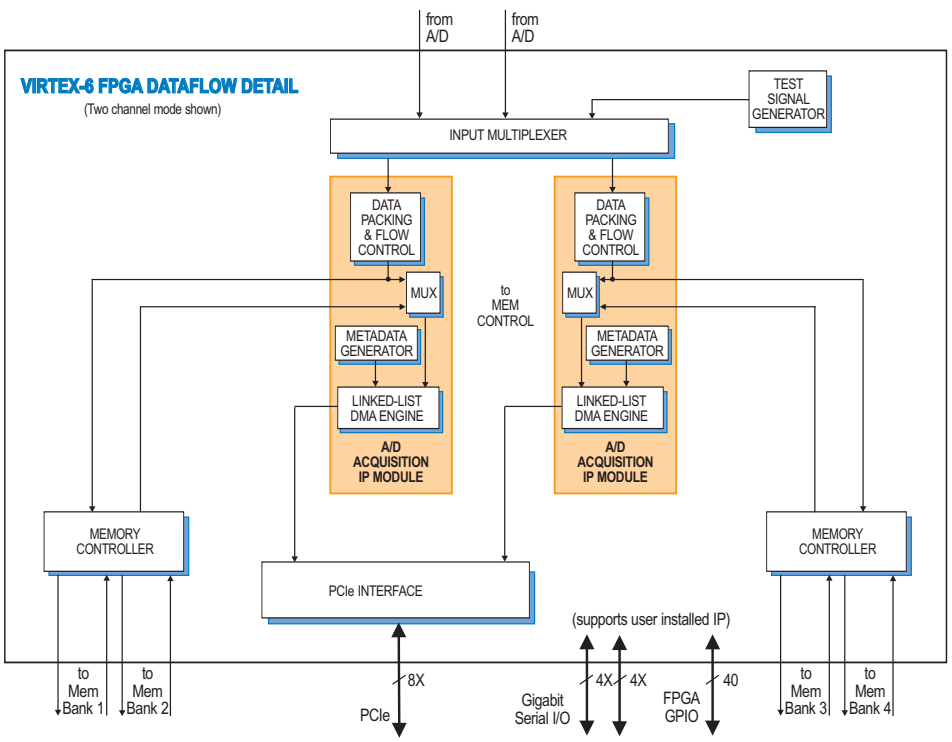
The Model 71640 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 5 GHz bit clock. With dual XMC connectors, the 71640 supports x8 PCIe on the first XMC connector leaving the optional second connector free to support user-installed transfer protocols specific to the target application. ➤

A/D Acquisition IP Module

The 71640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71640 — 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ PCI Express Interface

The Model 71640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
71640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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Model 71641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - XMC

General Information

Model 71641 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, Model 71641 includes an optional connection to the Virtex-6 FPGA for custom I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

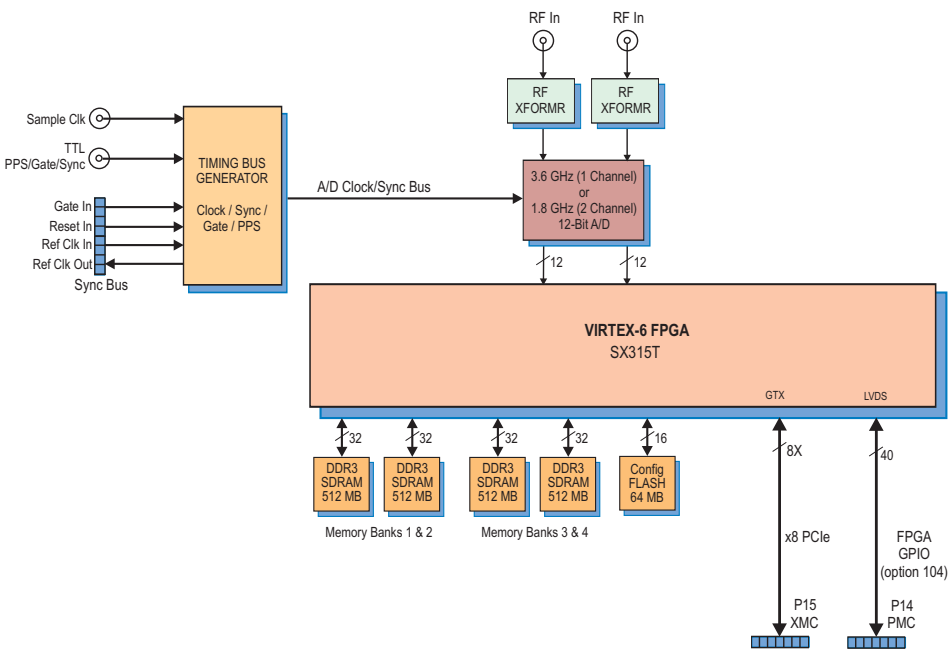
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sync bus for multimodule synchronization
- PCI Express Gen. 2 interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 71641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - XMC

A/D Acquisition IP Module

The 71641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

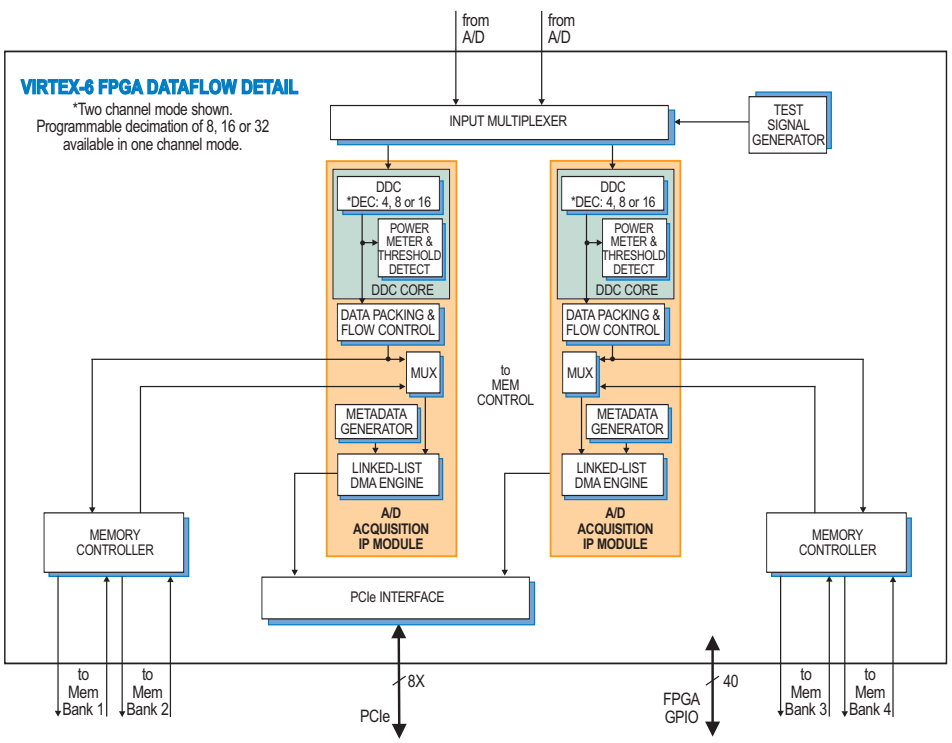
➤ Clocking and Synchronization

The 71641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 71641's can be synchronized with a simple cable. For larger systems, multiple 71641's can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

Memory Resources

The 71641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Model 71641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS FPGA I/O through P14 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ PCI Express Interface

The Model 71641 complies with the VITA 42.3 XMC specification and includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin front panel connector, includes gate, reset, and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include trigger and gate

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - XMC

General Information

Model 71650 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71650 includes optional general-purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

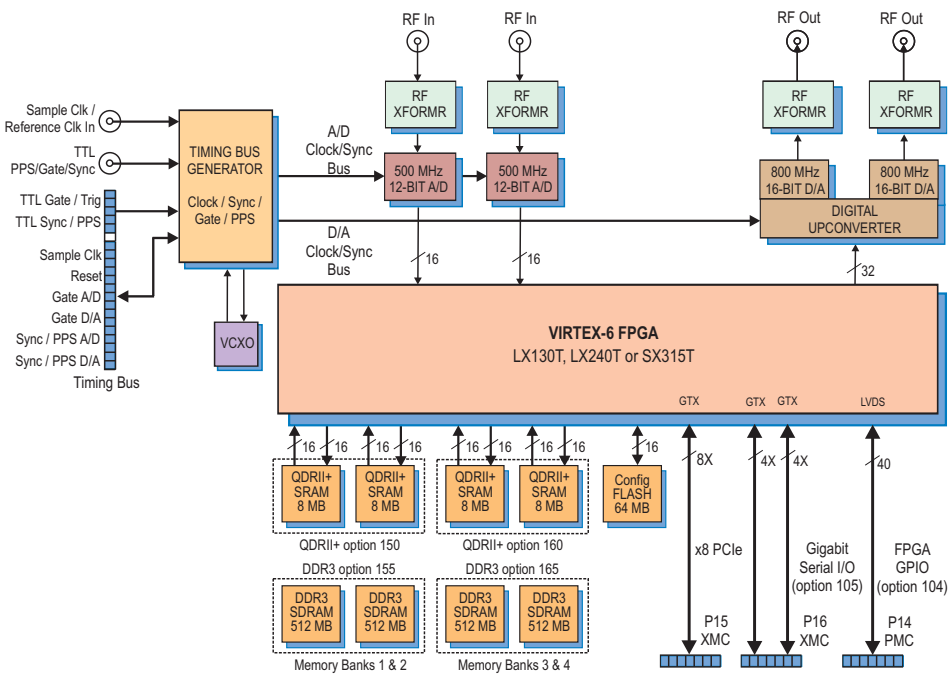
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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A/D Acquisition IP Modules

The 71650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

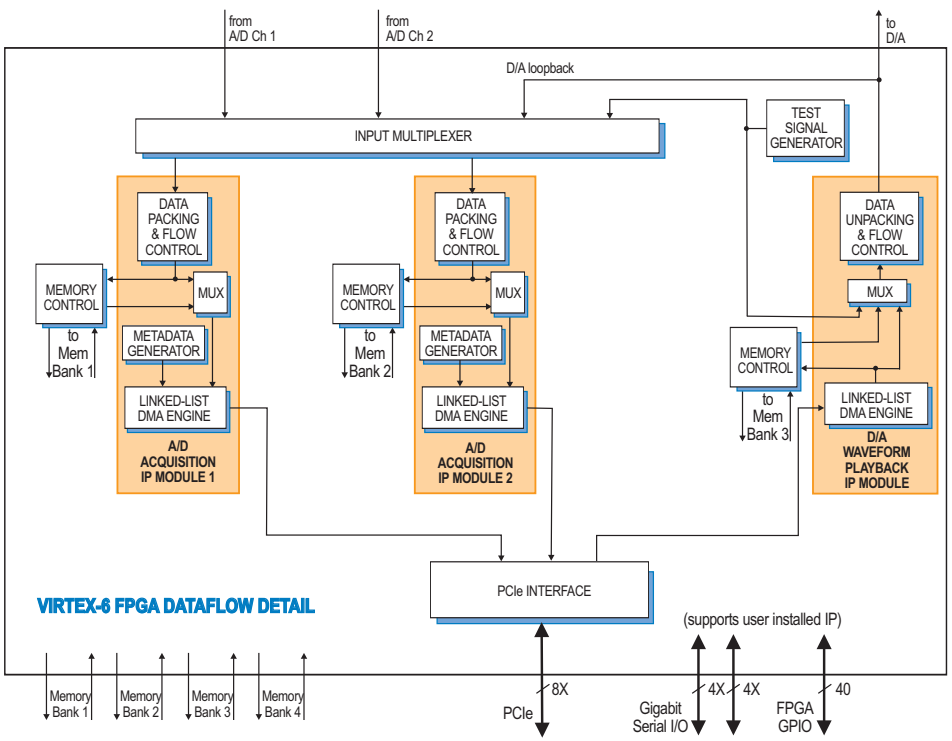
A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71650	Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240 FPGA
-064	XC6VSX315 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71650 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71650 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option 014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

General Information

Model 71651 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71651 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

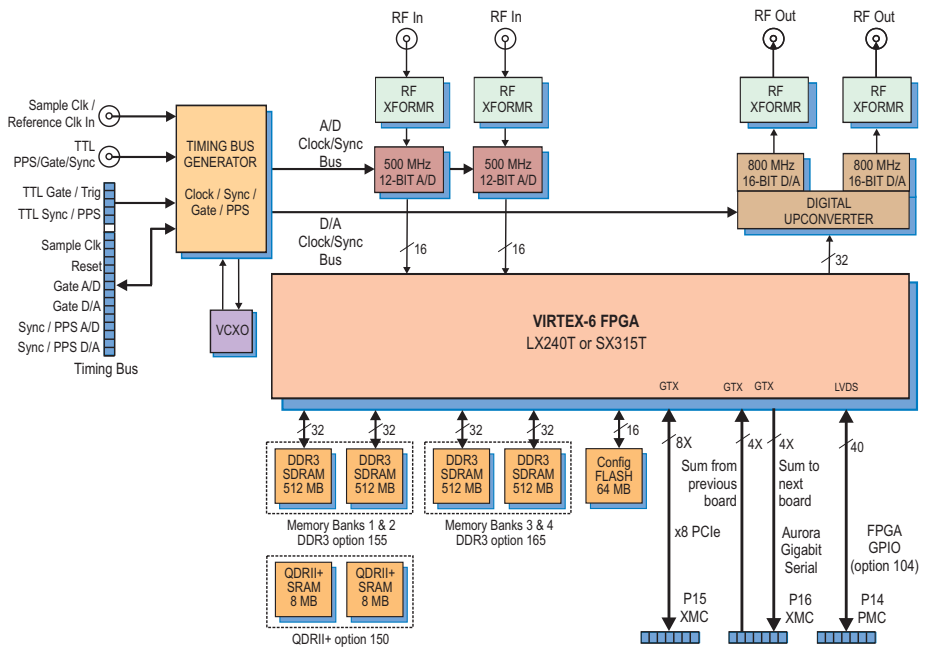
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

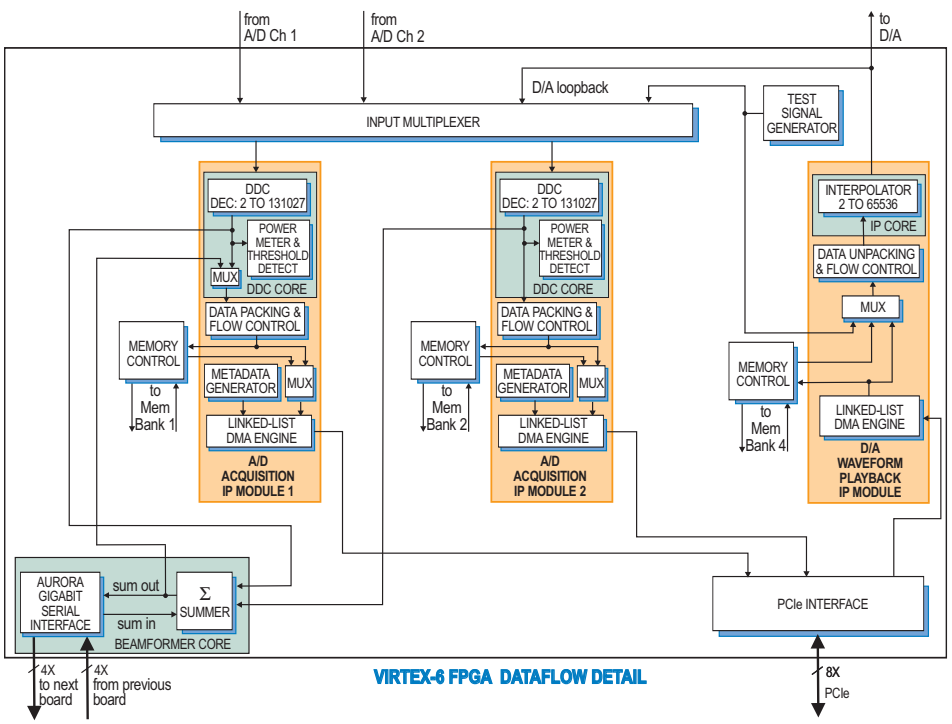
A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71651's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Model 71651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

➤ A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71651 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71651 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple modules.

PCI Express Interface

The Model 71651 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 71651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC

General Information

Model 71660 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

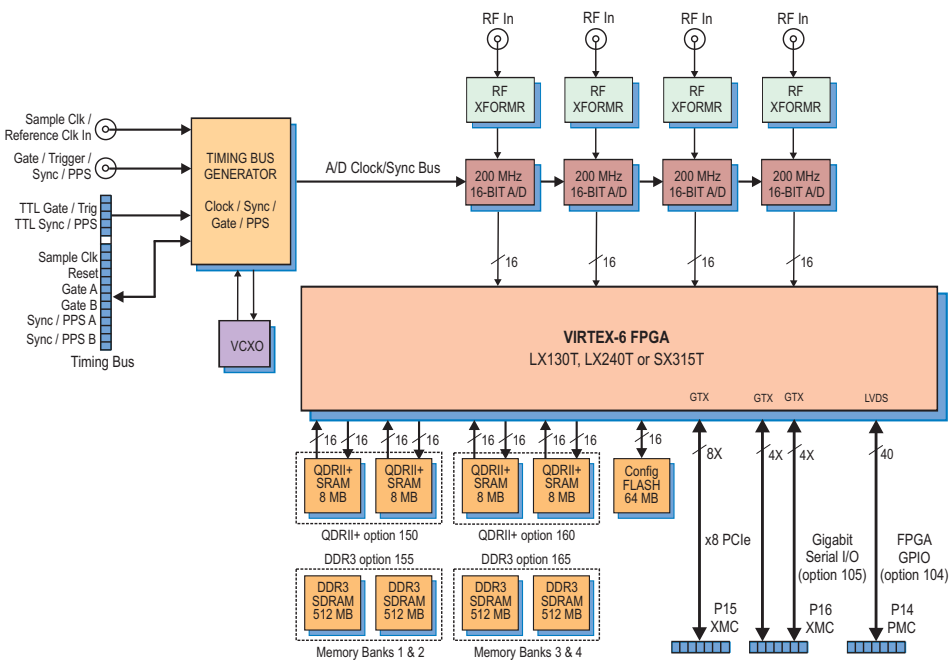
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

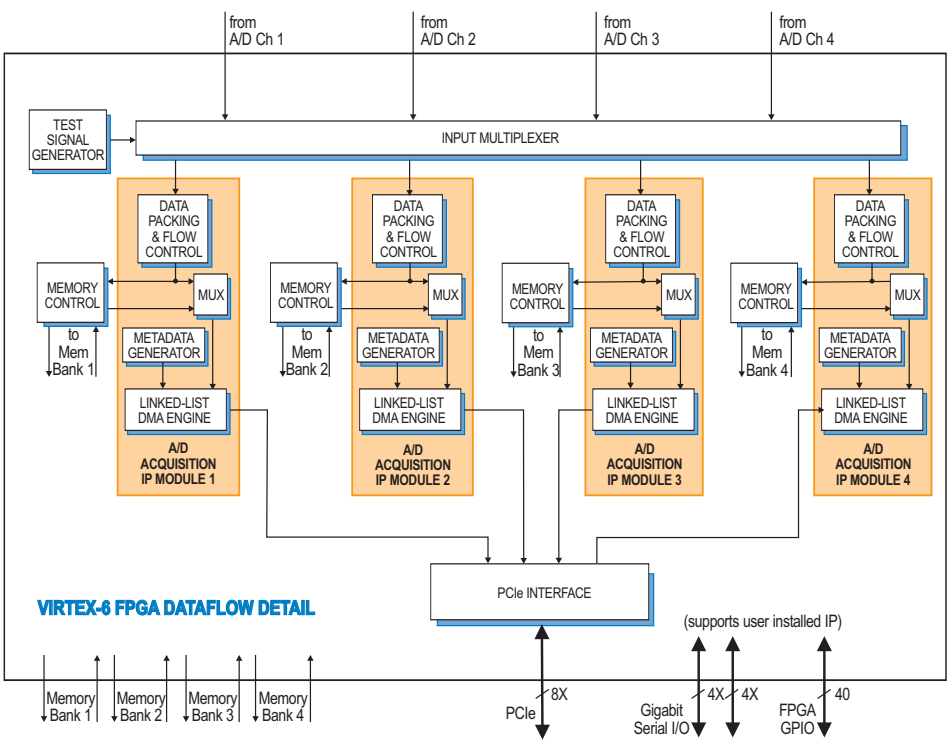
The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71660 ➤

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71660	4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC

General Information

Model 71661 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71661 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

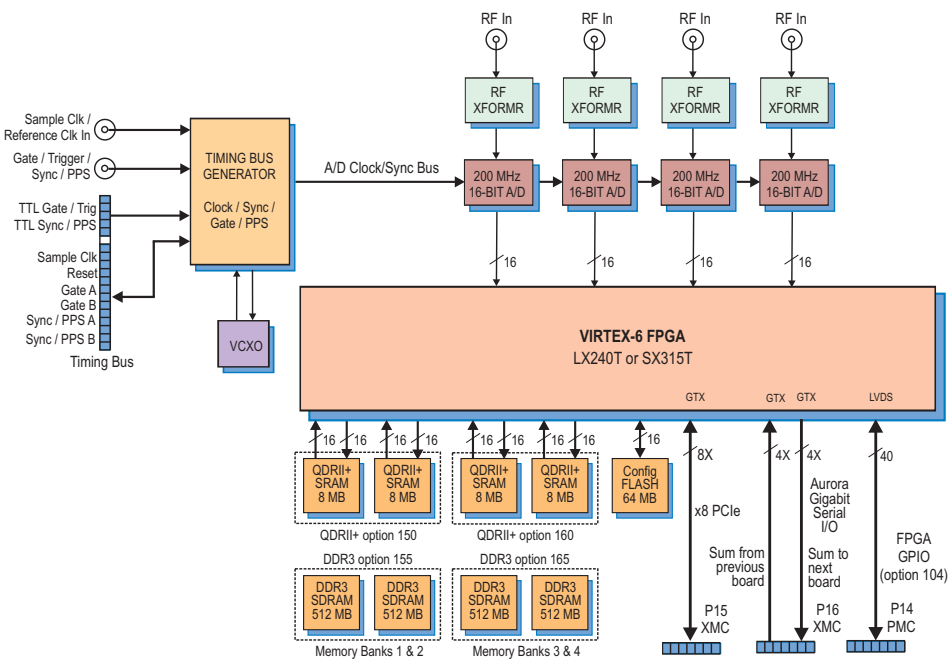
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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www.pentek.com

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

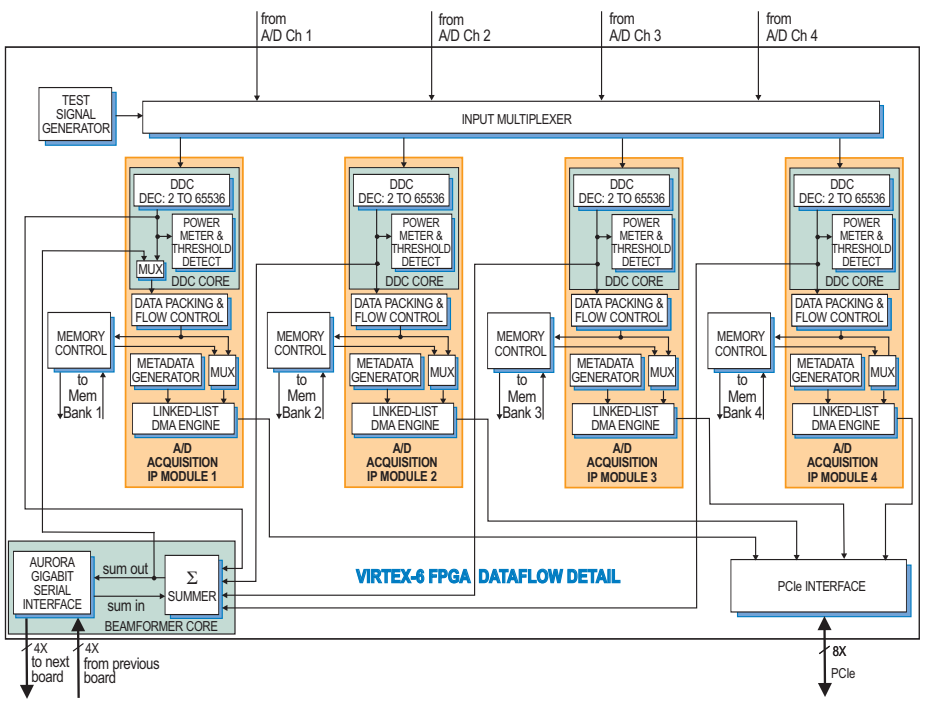
A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. ➤



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Model 71662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

General Information

Model 71662 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 71662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

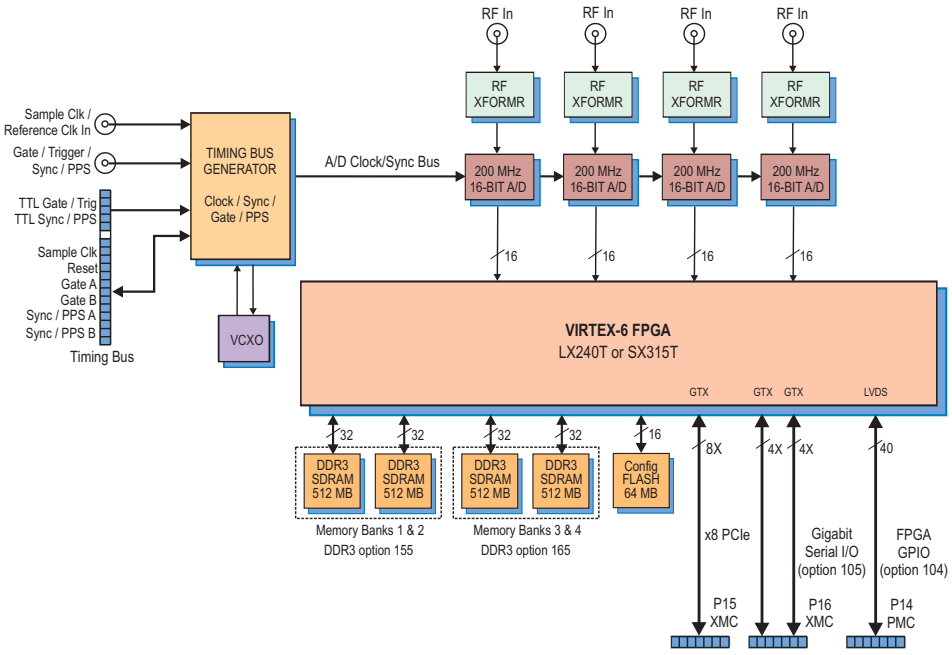
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable serial gigabit interfaces
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 71662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

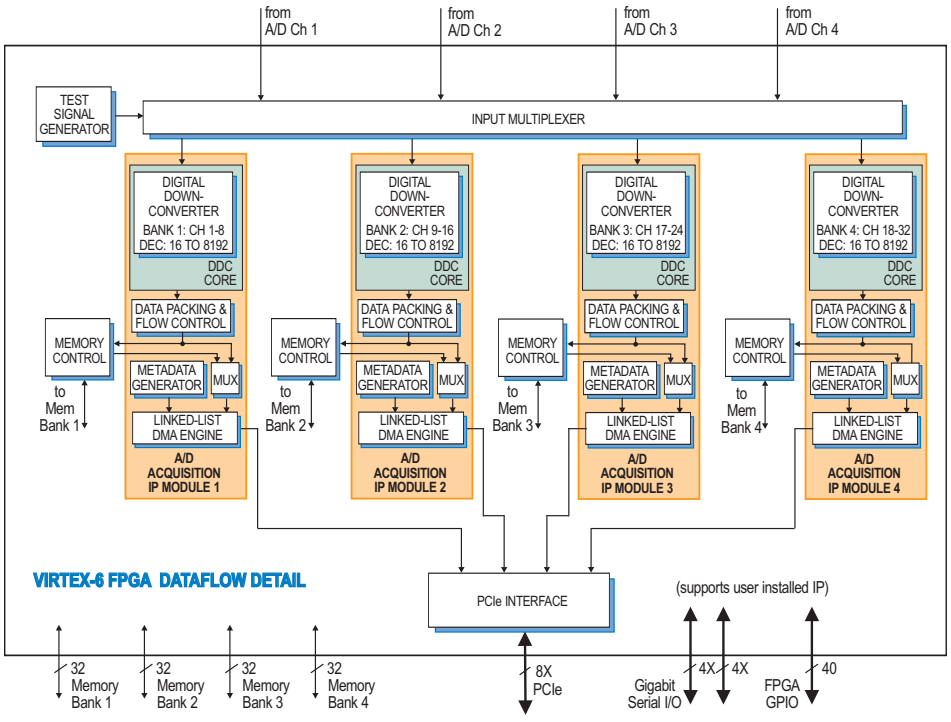
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.



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Model 71662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of ruged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71662 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71662 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71663

1100-Channel GSM Channelizer with Quad A/D - XMC

Cobalt

ReadyFlow Board Support Package

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

General Information

Model 71663 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 71663 is a complete, full-featured subsystem, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

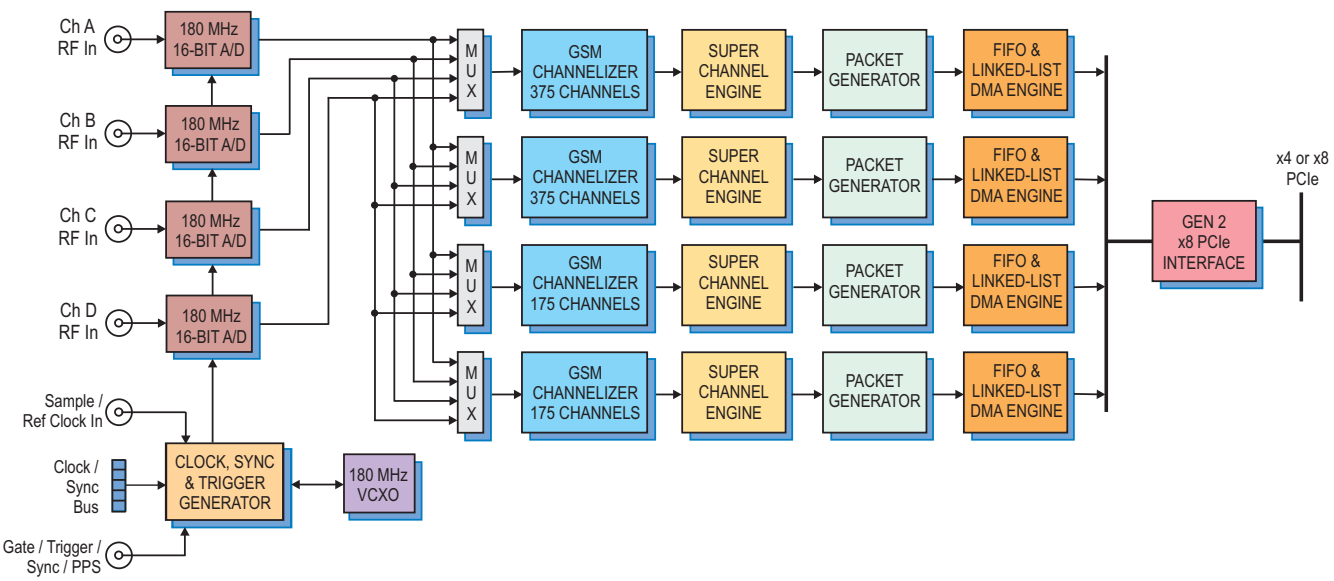
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

GSM Channelizer Cores

The 71663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤



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➤ The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 71663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 71663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 71663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 71663 and host. ➤

Model 71663 — 1100-Channel GSM Channelizer with Quad A/D - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: $-f_s/4$ (-270.8333 kHz)
  - Second: 0 Hz
  - Third: $+f_s/4$ (+270.8333 kHz)
  - Fourth: $+f_s/2$ (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
71663	1100-Channel GSM Channelizer with Quad A/D - XMC

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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New!

Model 71664

4-Ch. 200 MHz A/D w. DDCs, VITA-49.0, Virtex-6 FPGA - XMC

General Information

Model 71664 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 71664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71664 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

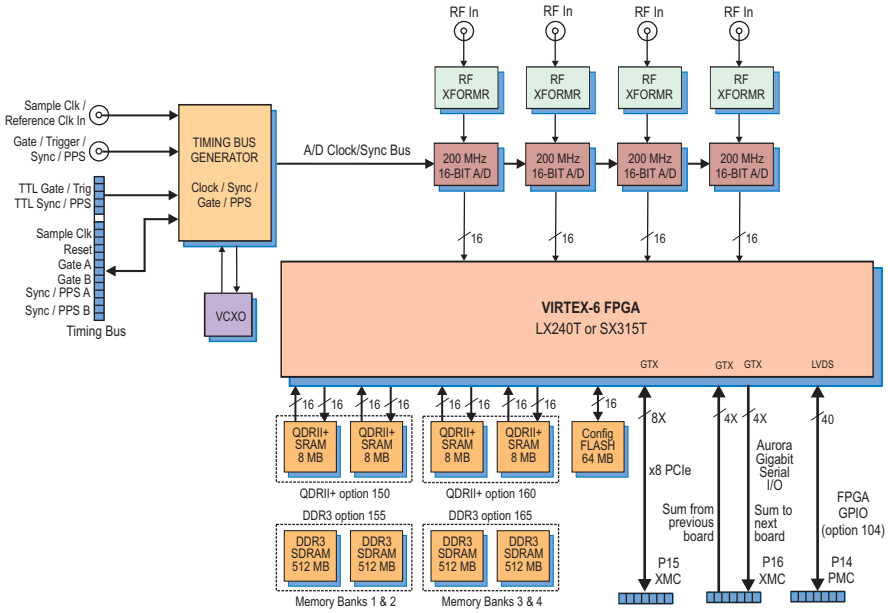
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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4-Ch. 200 MHz A/D w. DDCs, VITA-49.0, Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71664 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

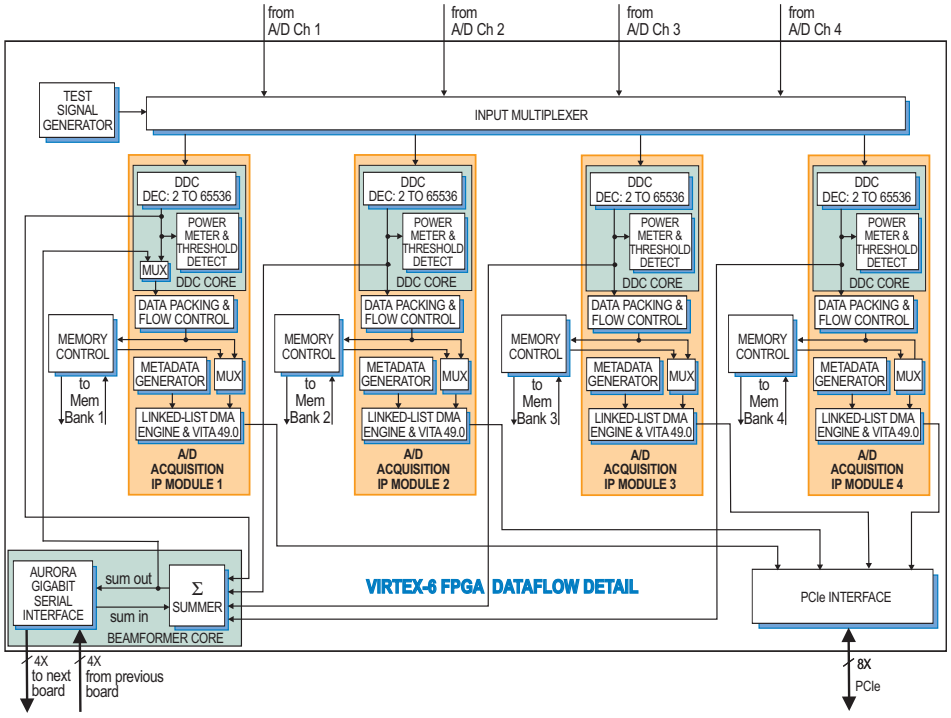
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71664's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 71664 supports fully the VITA 49.0 specification. ➤



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➤ A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71664's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71664 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71664 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple boards. ➤

Model 71664

4-Ch. 200 MHz A/D w. DDCs, VITA-49.0, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O
-150	Two 8 MB QDRII+ SRAM Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

➤

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Model 71670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC

General Information

Model 71670 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

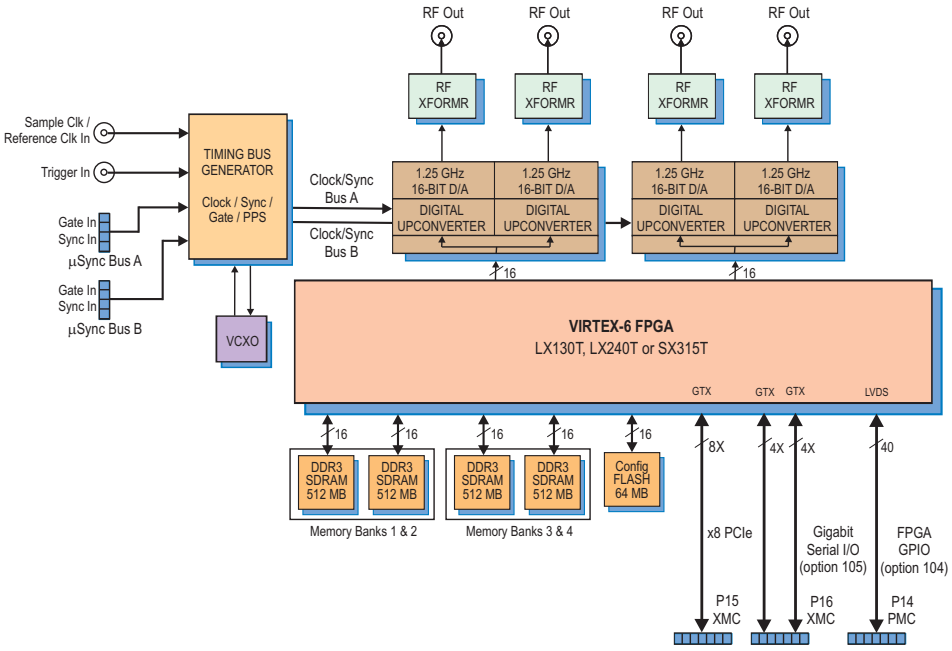
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 71670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

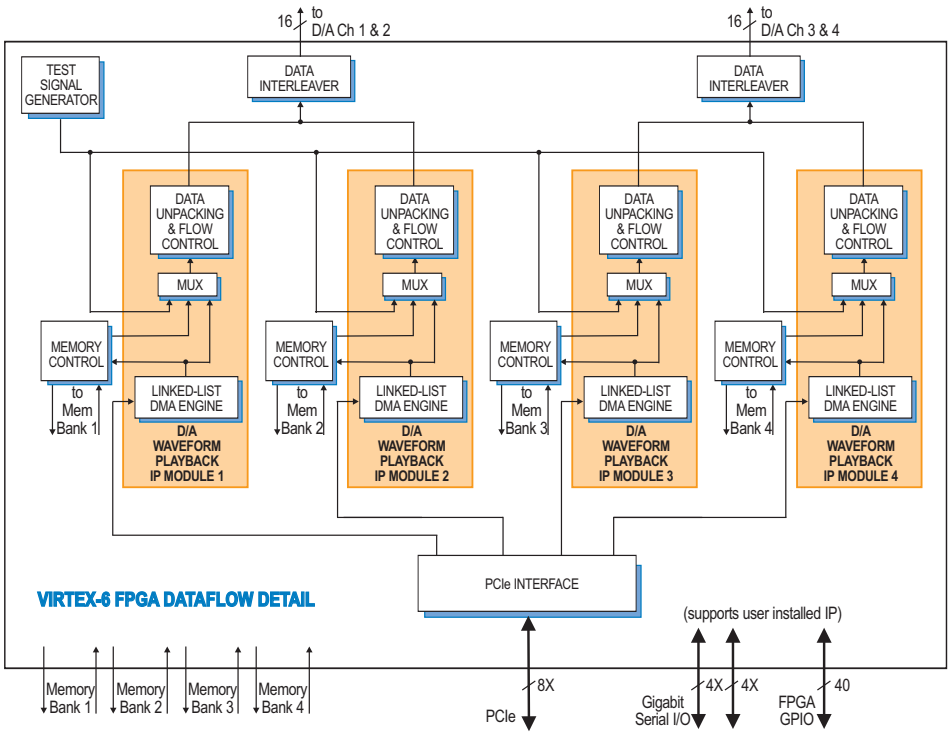
The Model 71670 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71670 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application. ➤

D/A Waveform Playback IP Module

The Model 71670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71670 — 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ PCI Express Interface

The Model 71670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC

General Information

Model 71671 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71671 includes optional general-purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

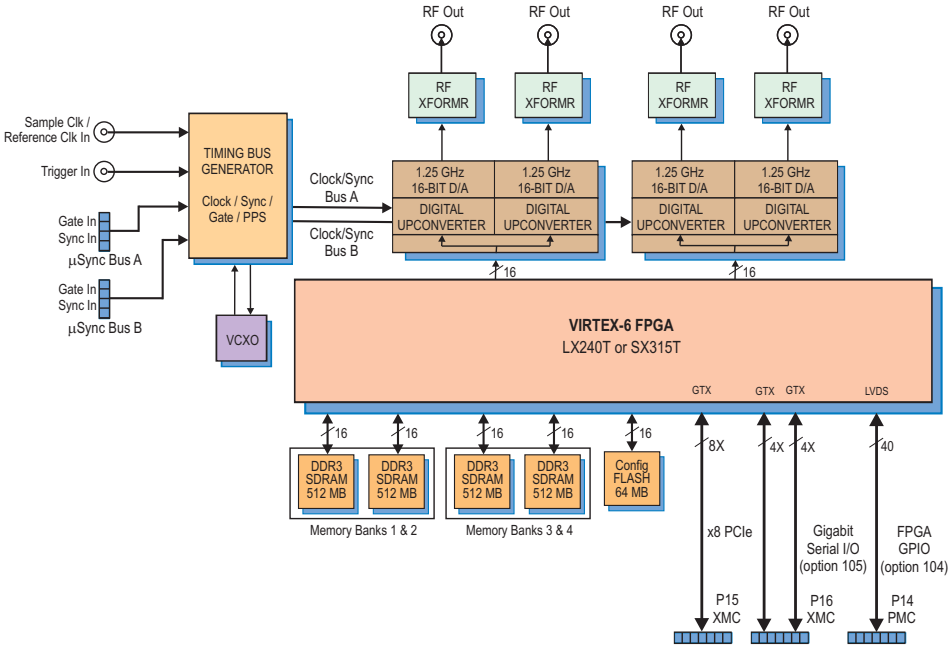
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 71671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

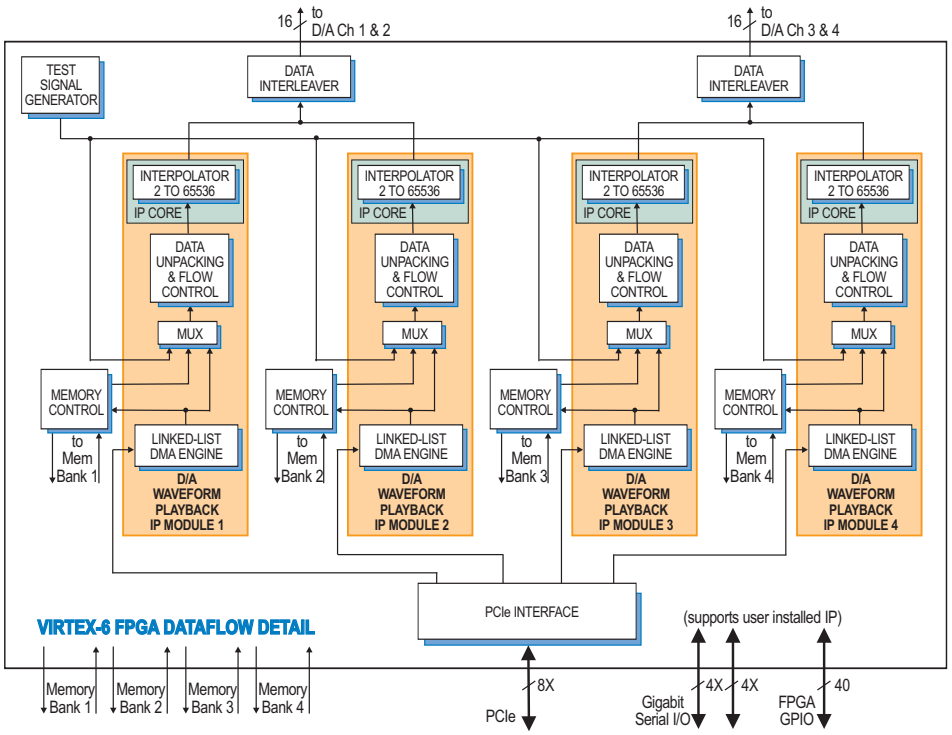
D/A Waveform Playback IP Module

The Model 71671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Model 71671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ XMC Interface

The Model 71671 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71671 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Model 71690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

General Information

Model 71690 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71690 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

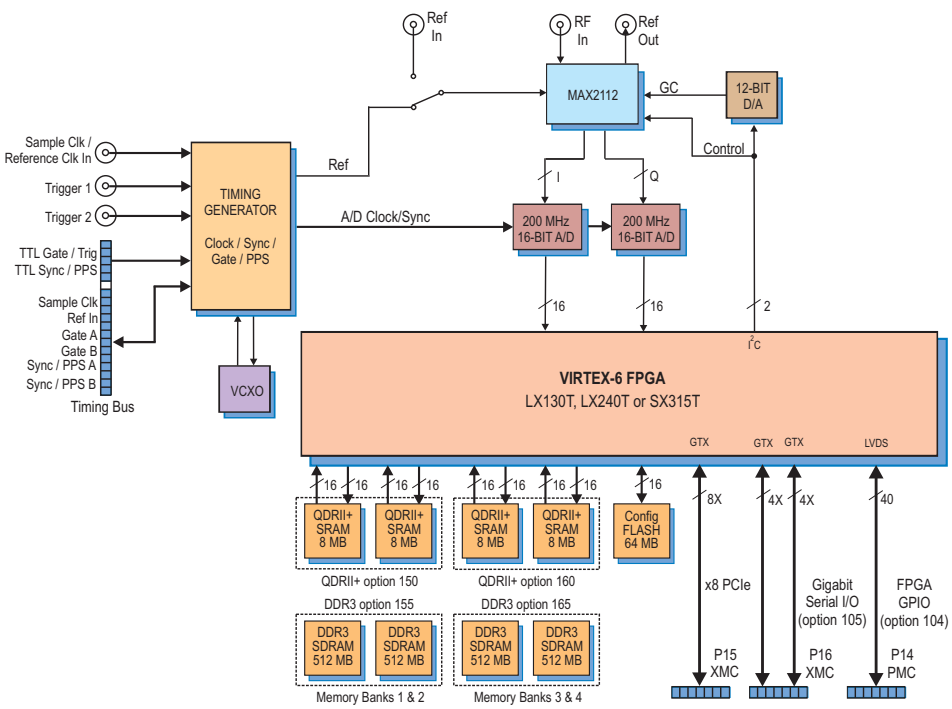
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds digitize the I + Q signals synchronously
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization

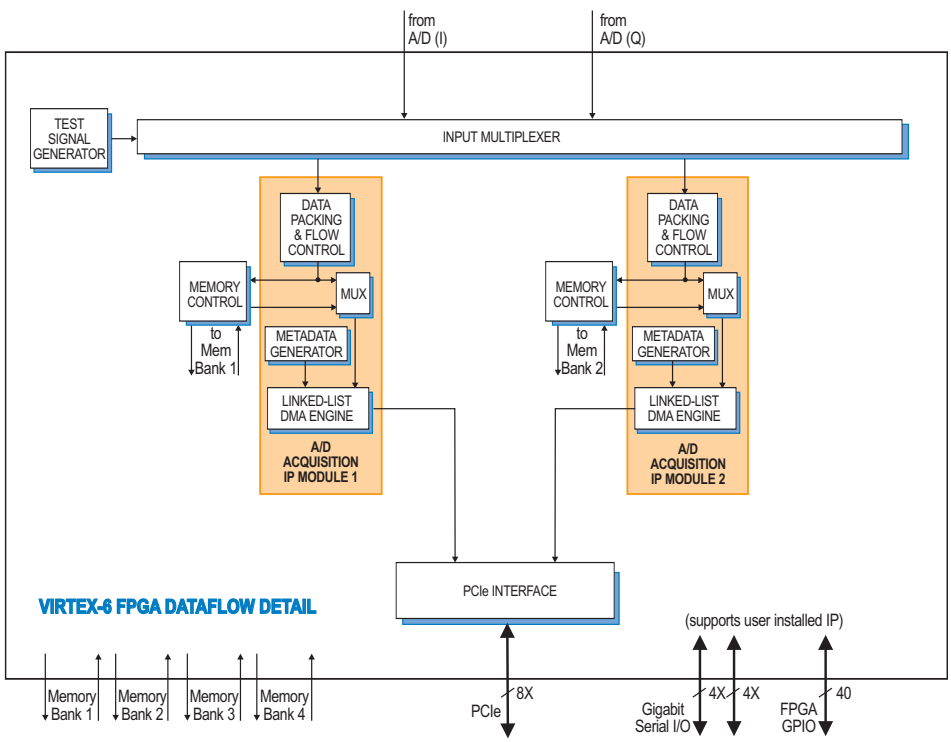
An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

XMC Interface

The Model 71690 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71690 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- ***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2 x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - XMC

General Information

Model 71720 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71720 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

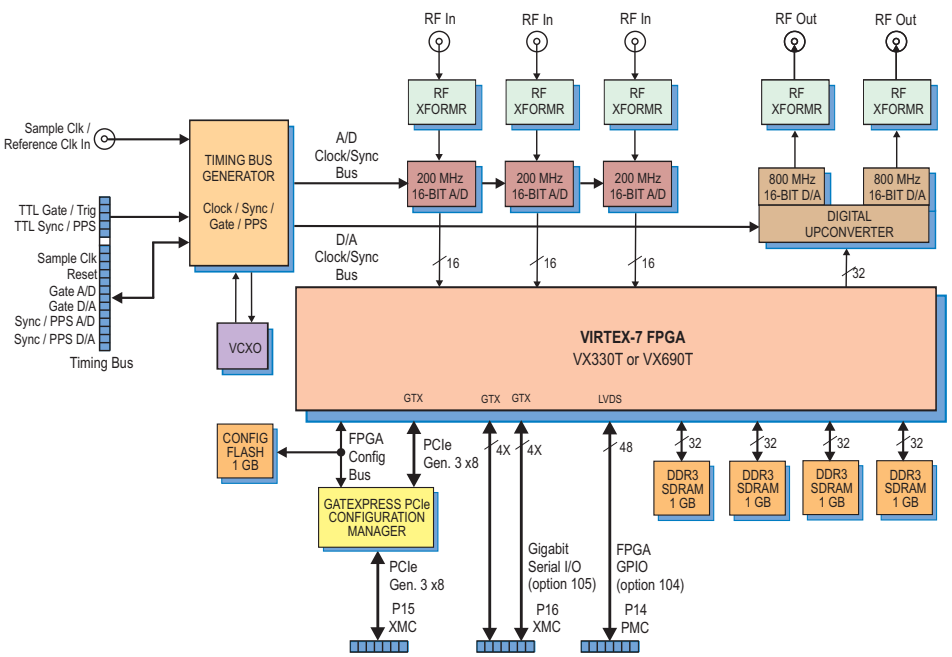
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched-fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Model 71720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - XMC

A/D Acquisition IP Modules

The 71720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

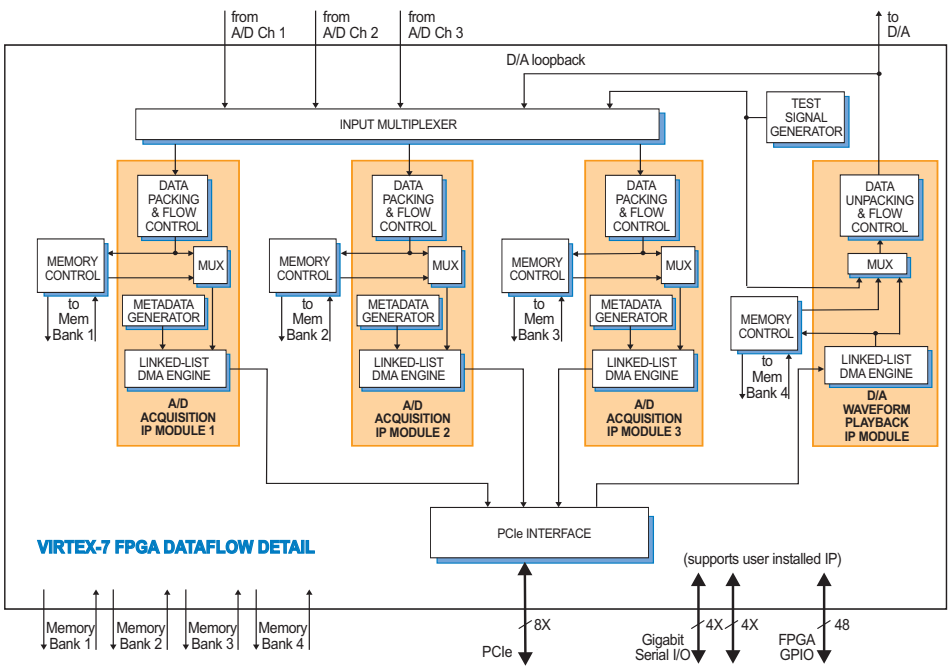
The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458

Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

Model 71720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - XMC

Memory Resources

The 71720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

XMC Interface

The Model 71720 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 GB/sec per lane. With dual XMC connectors, the 71720 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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www.pentek.com

Model 71721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

General Information

Model 71721 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71721 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

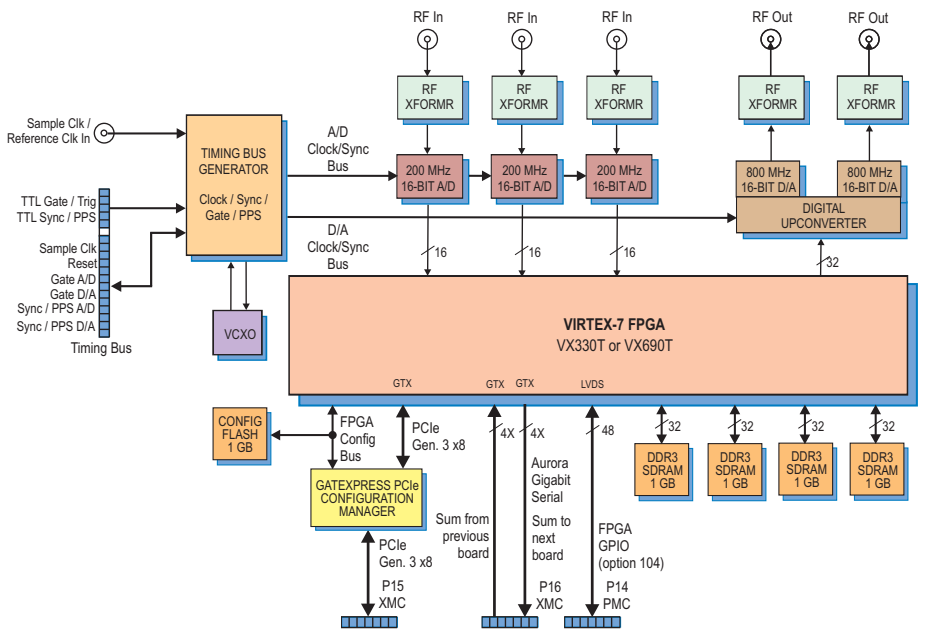
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

A/D Acquisition IP Modules

The 71721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

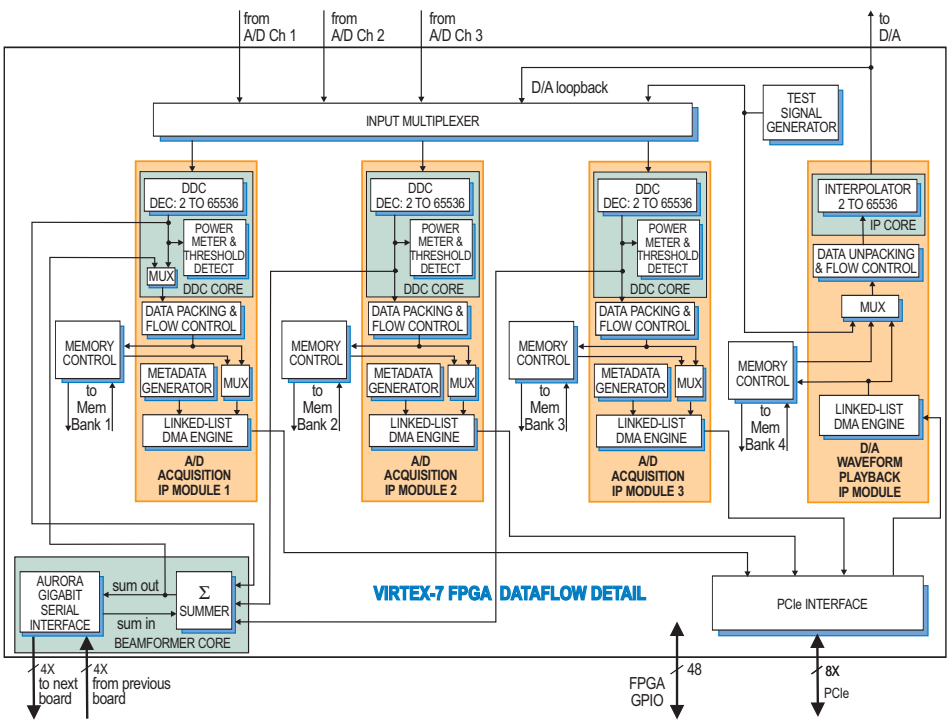
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71721's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71721's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. ➤

Model 71721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

XMC Interface

The Model 71721 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71721 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple modules.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Memory Resources

The 71721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - XMC

General Information

Model 71730 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71730 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

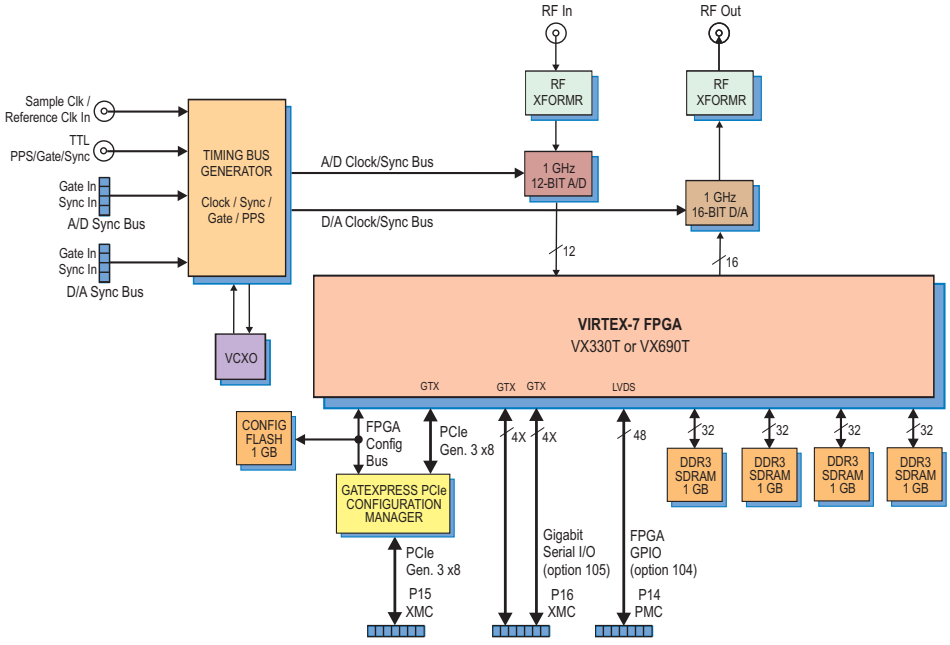
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - XMC

A/D Acquisition IP Module

The 71730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

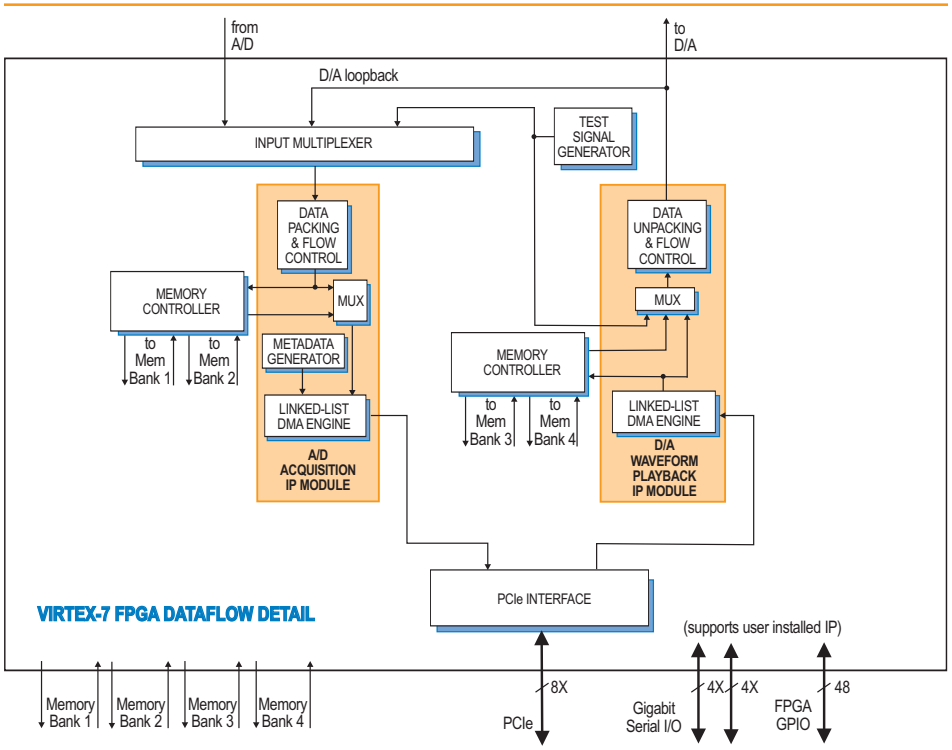
A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GS/sec, allowing it to accept full-rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - XMC

XMC Interface

The Model 71730 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71730 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71730	1 GHz A/D and D/A, Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 71730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

General Information

Model 71741 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

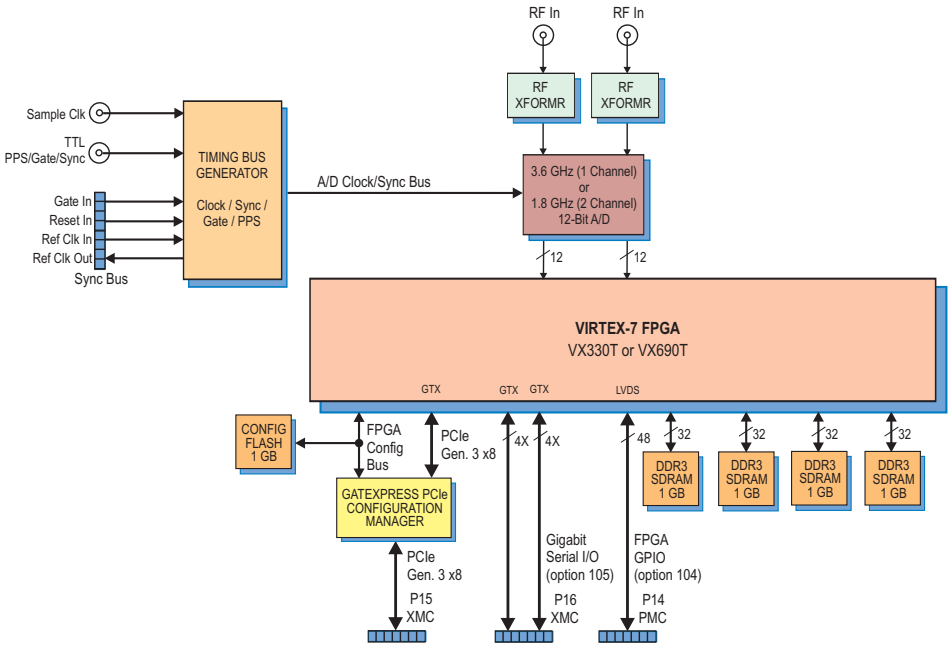
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

A/D Acquisition IP Module

The 71741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

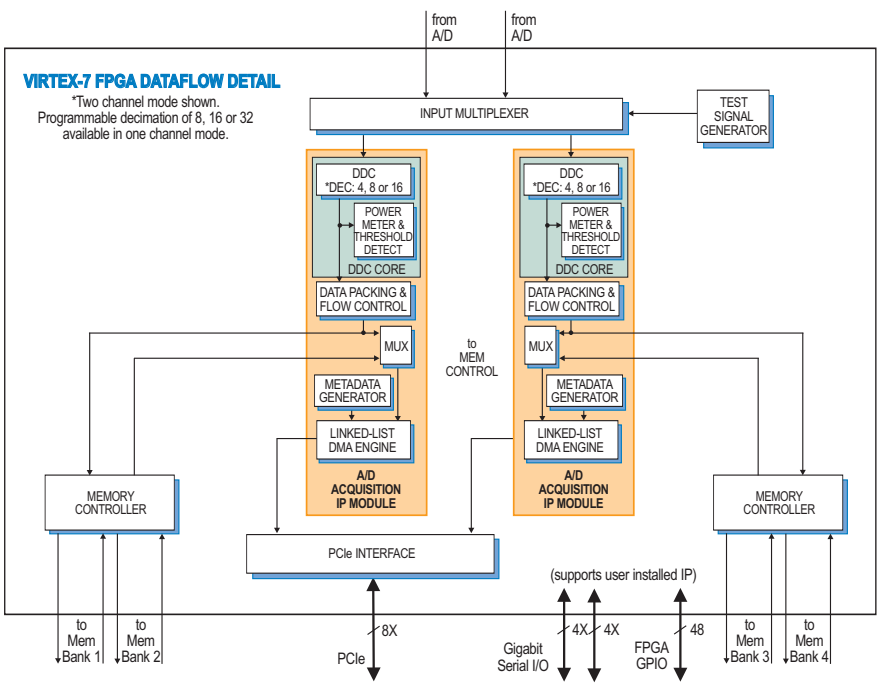
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed. ➤



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Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

Memory Resources

The 71741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

PCI Express Interface

The Model 71741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 71741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71741's can be synchronized with a simple cable. For larger systems, multiple 71741's can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

General Information

Model 71751 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71751 includes a general purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71751 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

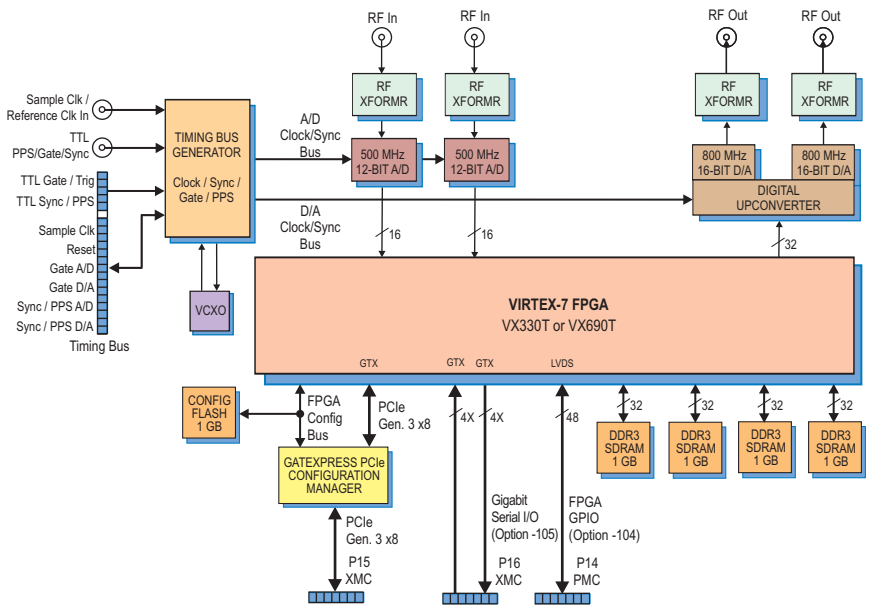
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

A/D Acquisition IP Modules

The 71751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 71751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

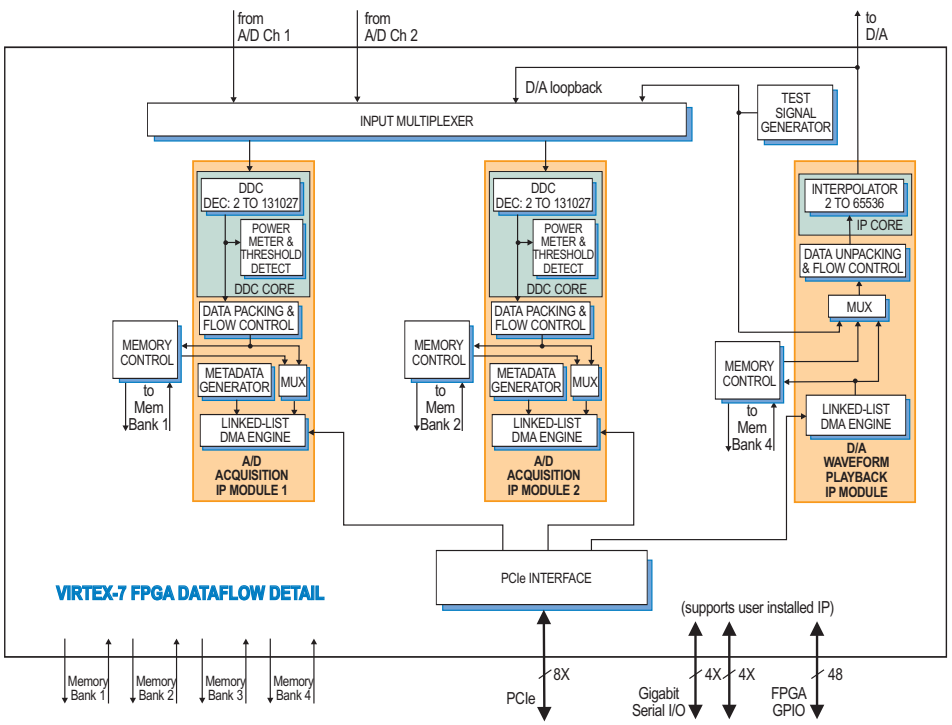
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71751's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71751 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71751 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple modules.

PCI Express Interface

The Model 71751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 71751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 71760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - XMC

General Information

Model 71760 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

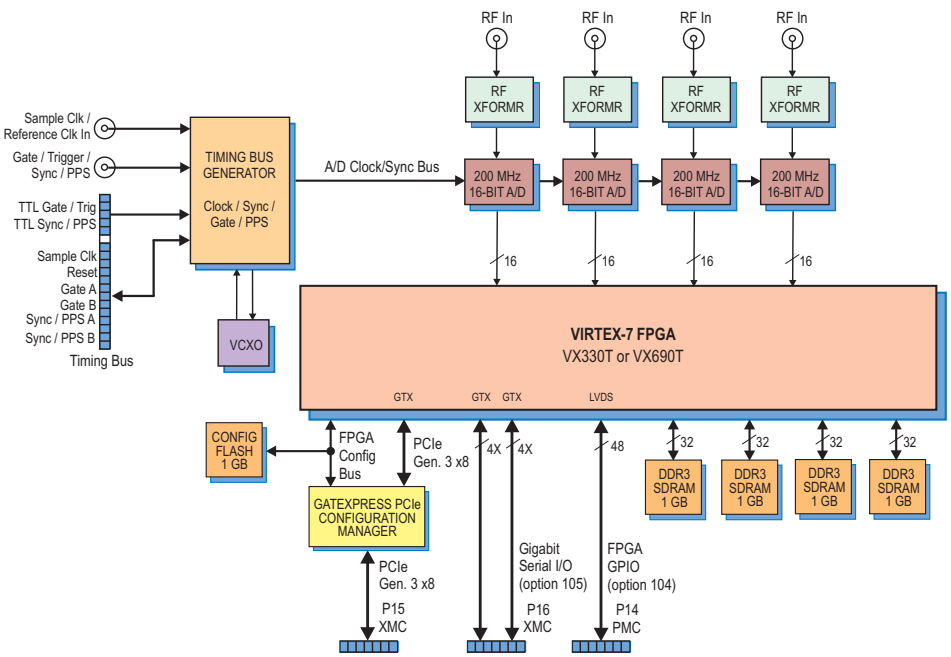
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Advanced reconfigurability features
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

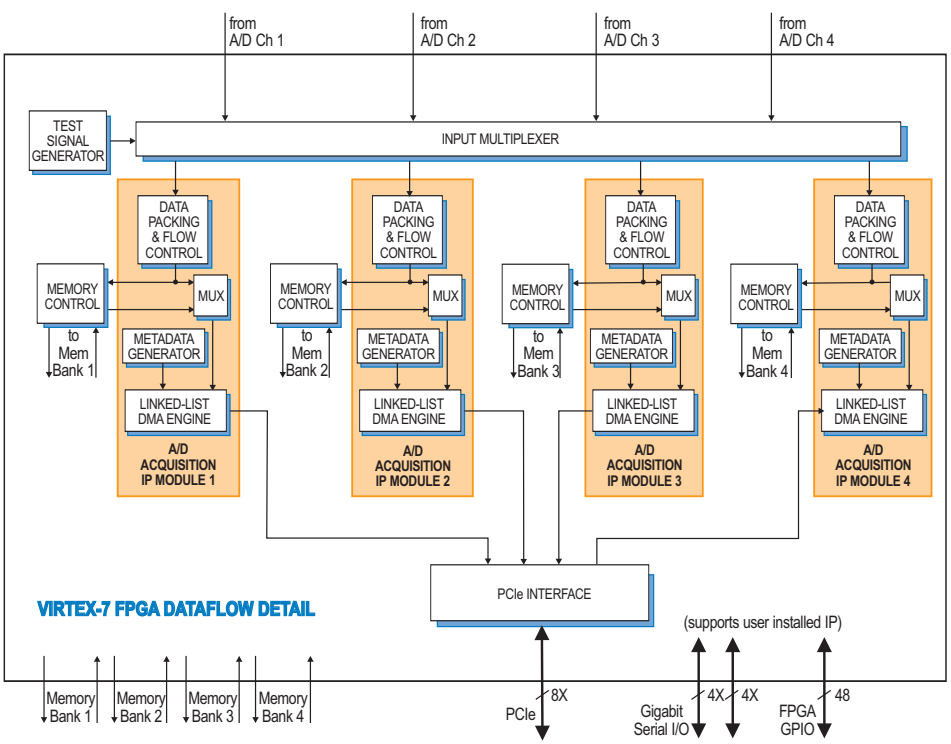
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an ➤

A/D Acquisition IP Modules

The 71760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Model 71760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71760	4-Channel 200 MHz A/D with Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71760's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71760 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71760 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8 Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71761

4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC

General Information

Model 71761 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71761 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

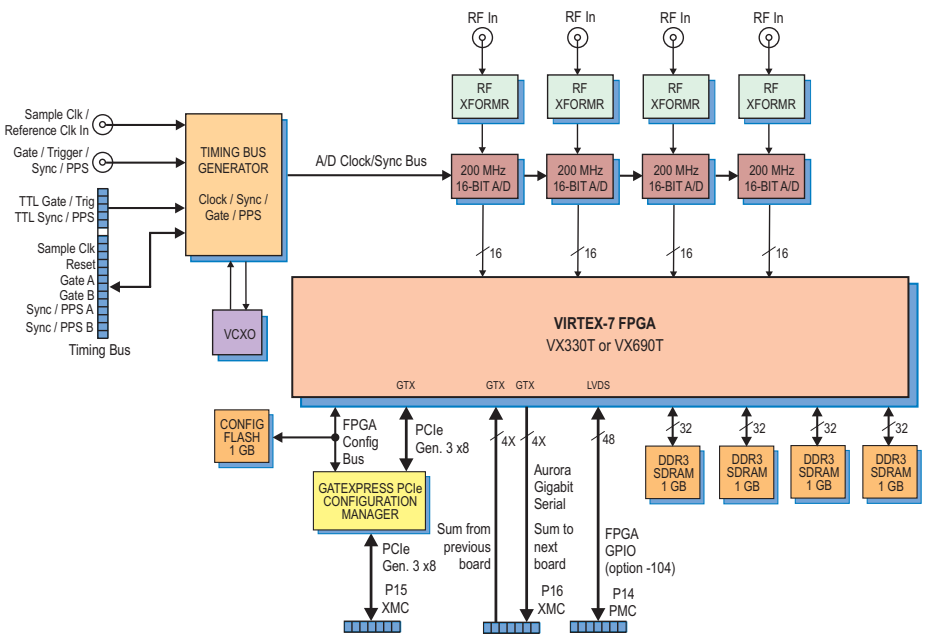
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC

A/D Acquisition IP Modules

The 71761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 71761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

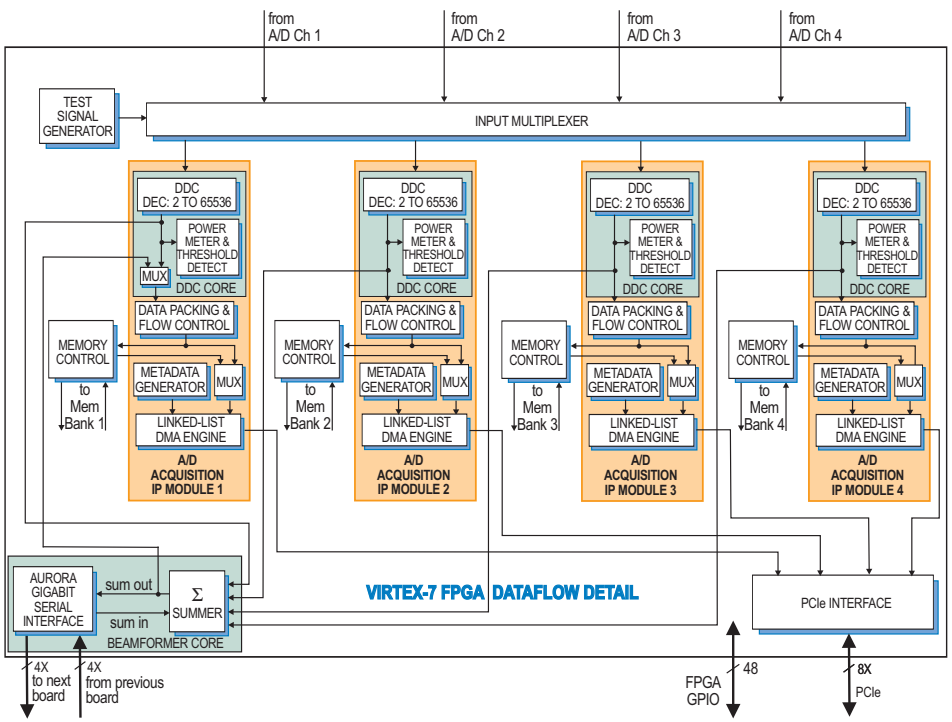
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71761's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple modules.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71761 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71761 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to board interface for beamforming accross multiple modules. ➤

Model 71761 — 4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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New!

Model 71791

L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - XMC

General Information

Model 71791 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 71791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 71791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

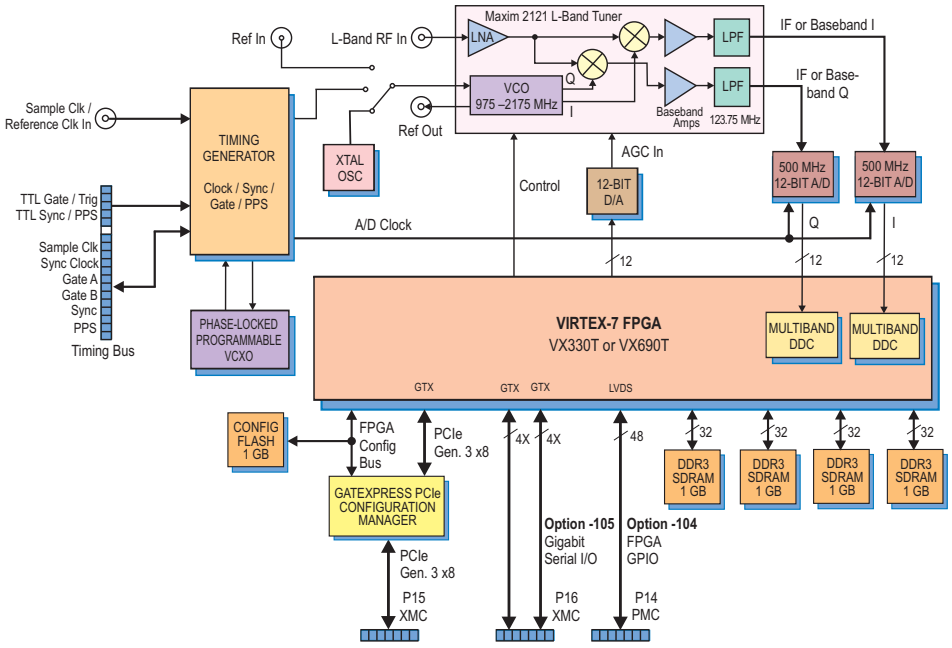
For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS to match the specific requirements of external custom I/O connections to the FPGA.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - XMC

A/D Acquisition IP Modules

The 71791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

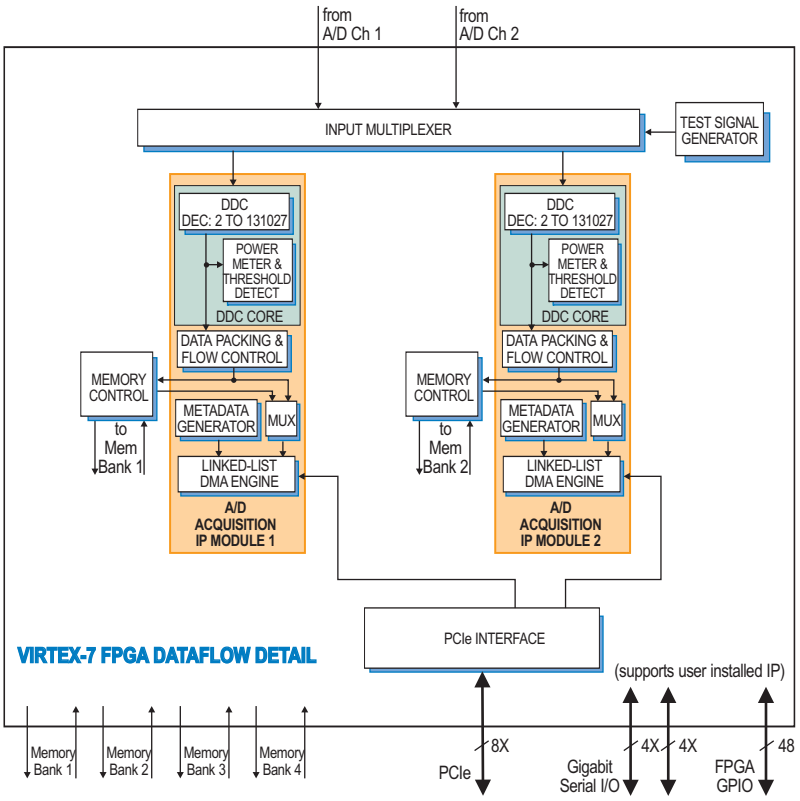
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA .

PCI Express Interface

The Model 71791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 71791

L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCIe boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - XMC

Options:

-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PCIe Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** –97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference ($freq_{REF}$):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** 3 dB cutoff frequency: 123.75 MHz

A/D Converters
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3*: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

* Gen 3 requires a compatible backplane and SBC

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Model 71131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Powerful Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71131 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71131 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

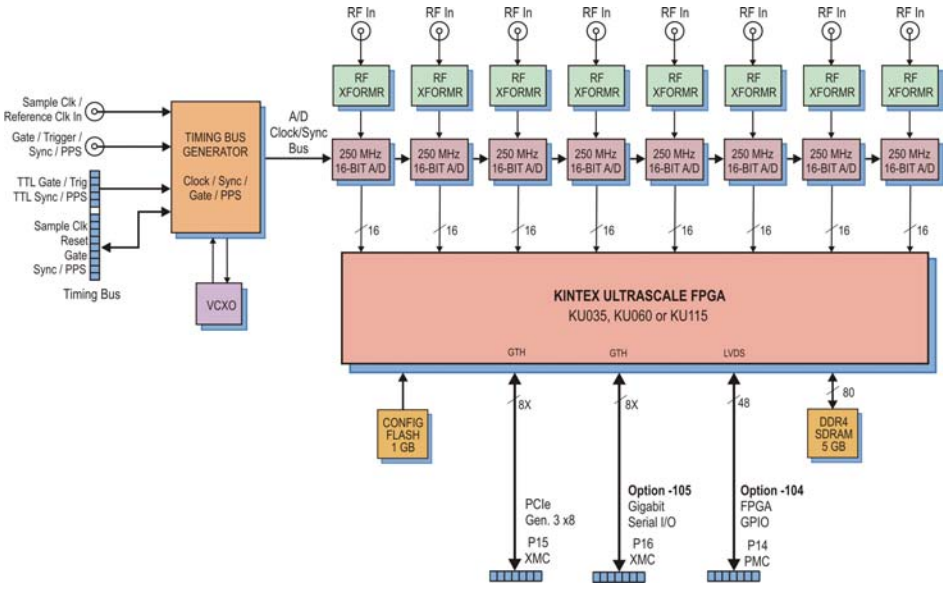
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71131 features eightA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with eight full duplex gigabit links to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

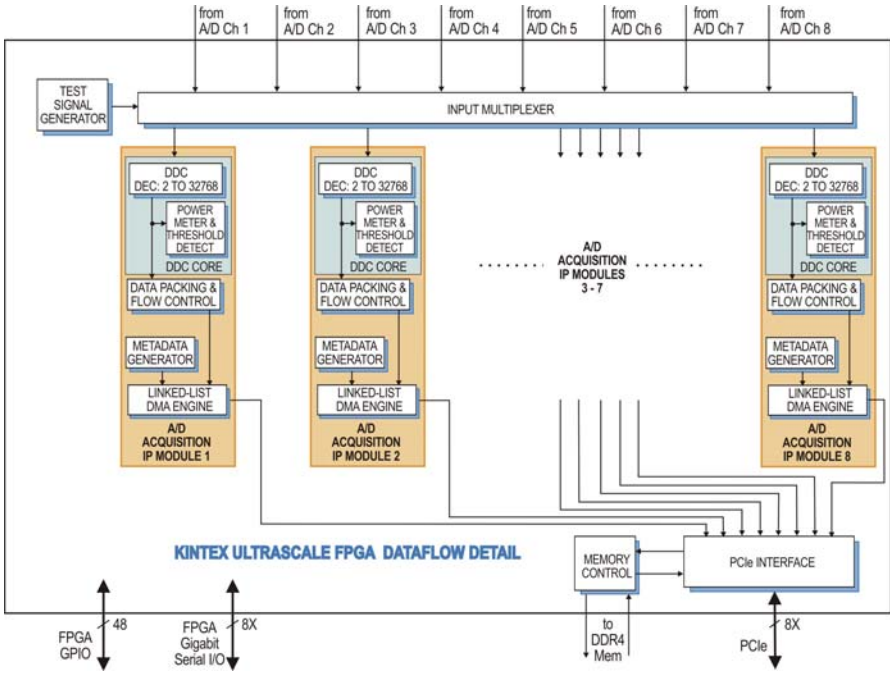
Up to three additional modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, the Model 7893 System Synchronizer supports additional modules in increments of eight.

Memory Resources

The 71131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 71131 includes an industry-standard interface fully compliant with PCI ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71131 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71131 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Standard XMC module, 2.91 in. x 5.87 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 71132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Powerful Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71132 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

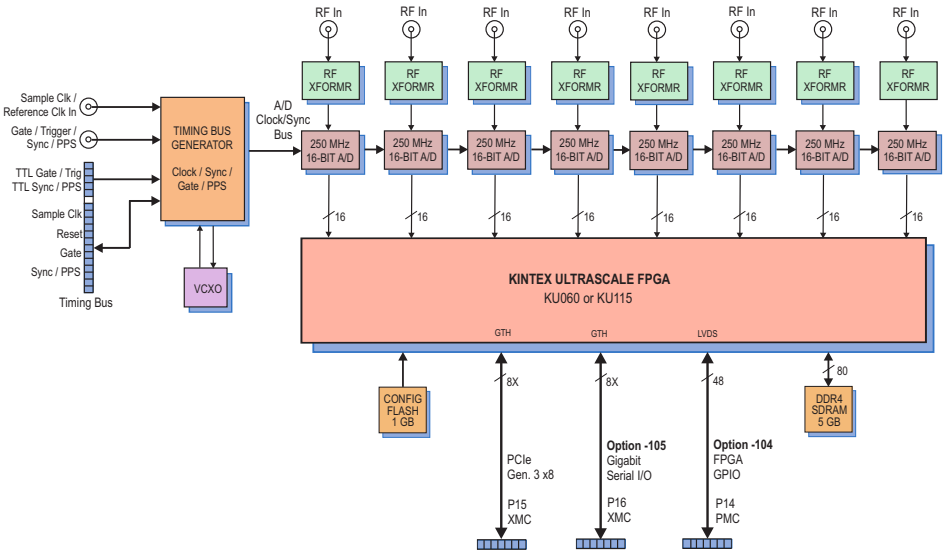
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



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www.pentek.com

Model 71132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71132 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with eight full duplex gigabit links to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

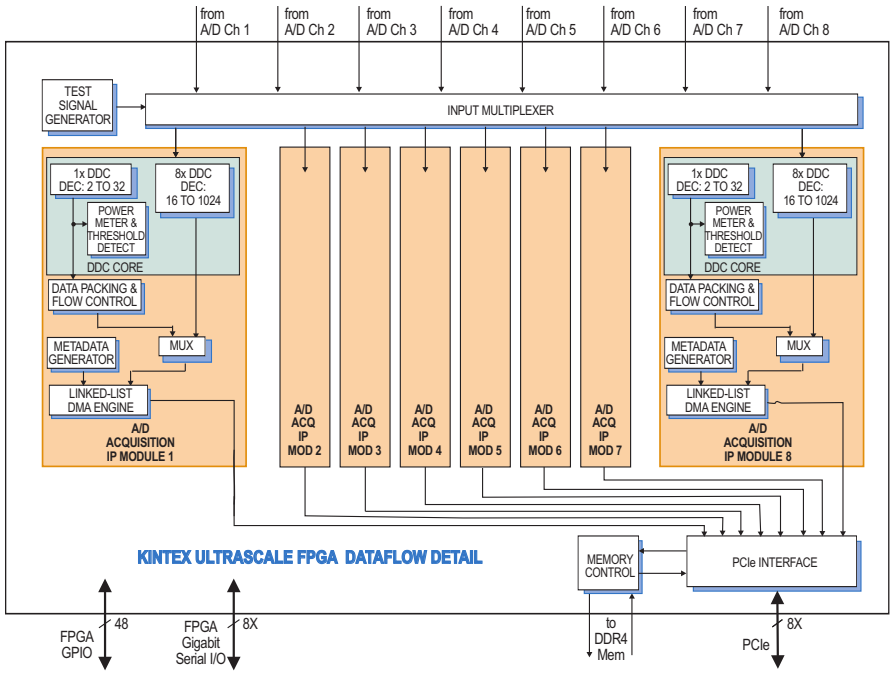
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three additional modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, the Model 7893 System Synchronizer supports additional modules in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
71132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 71132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71132 complies with the VITA 42.0 XMC specification. A connector provides a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71132 supports x8 PCIe on the first XMC connector leaving the second free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Eight banks, 8 channels per bank
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New

Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71141 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

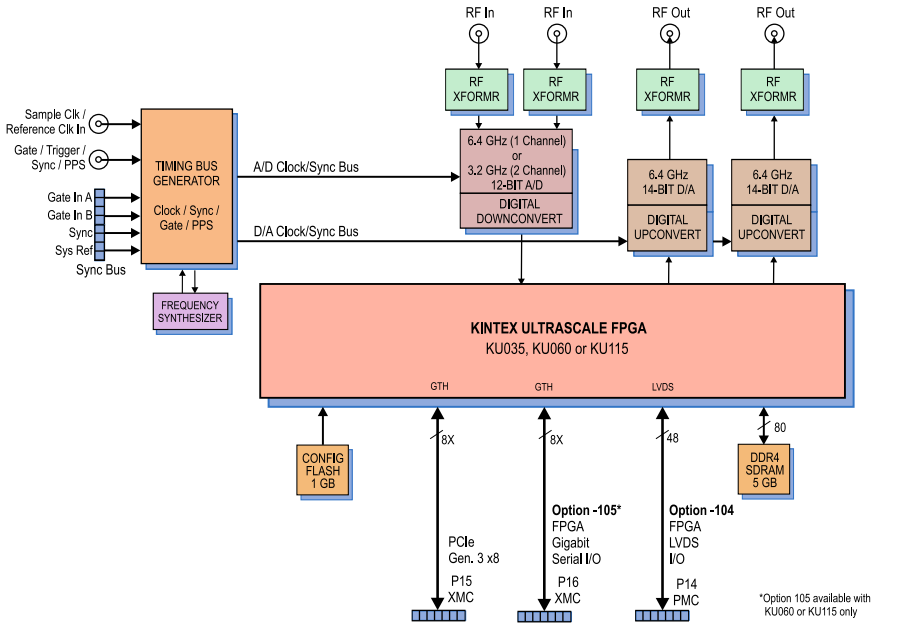
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

A/D Acquisition IP Module

The 71141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 71141 factory installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 71141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

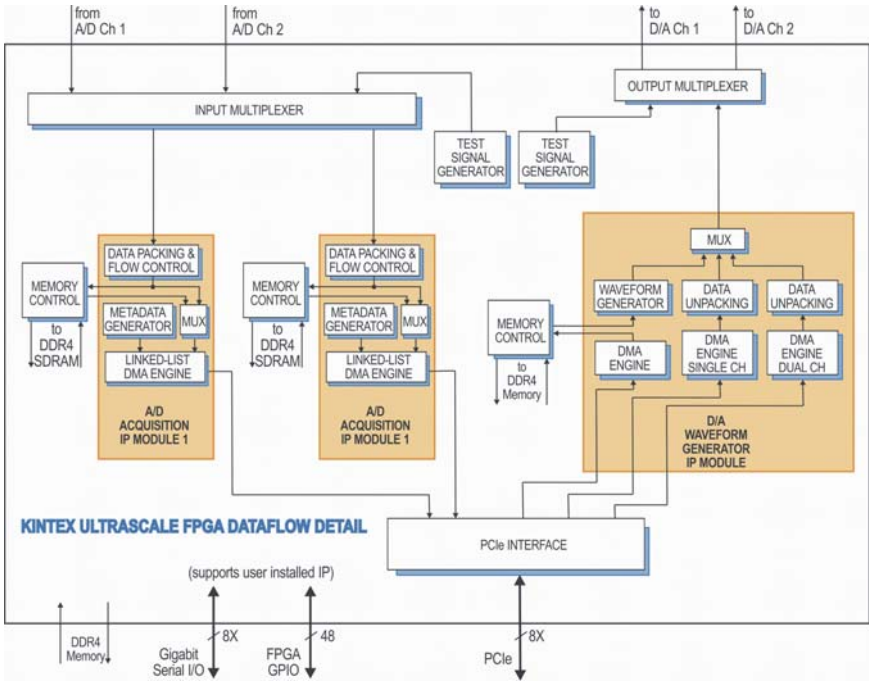
PCI Express Interface

The Model 71141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 71141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7192 high-speed sync module can be used to drive the sync bus to synchronize multichannel systems. ➤



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Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105 (only available with option -084 or -087):** Installs the XMC P16 connector configurable as one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Ordering Information

Model	Description
71141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through P14 connector
- 105	Gigabit serial FPGA I/O through P16 connector
- 702	Air cooled, Level L2
- 713	Conduction-cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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New!

Model 71821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71821 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 71821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

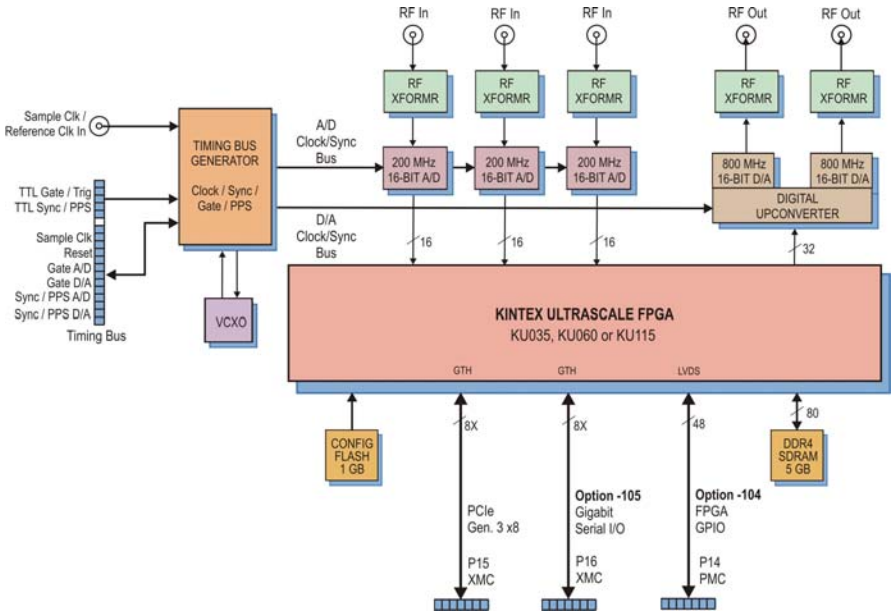
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 71821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 71821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the P16 XMC connector to support serial protocols.

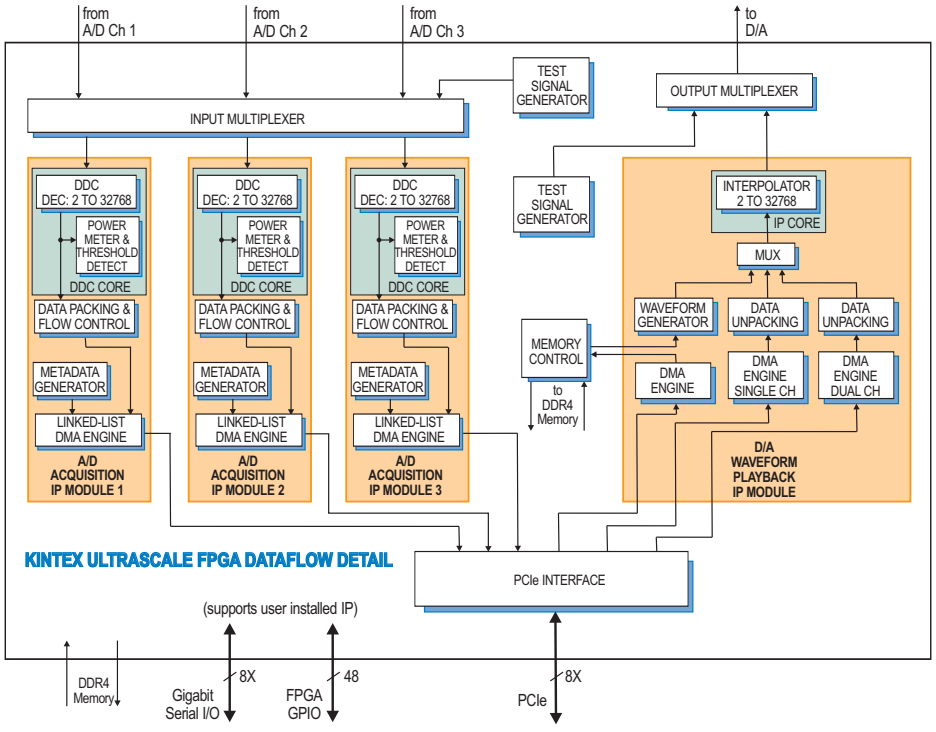
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

XMC Interface

The Model 71821 complies with the VITA 42.0 XMC specification. Each of two connectors provides a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71821 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 71821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - XMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X gigabit link between the FPGA and XMC P16 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

New!

Model 71841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - XMC

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71841 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

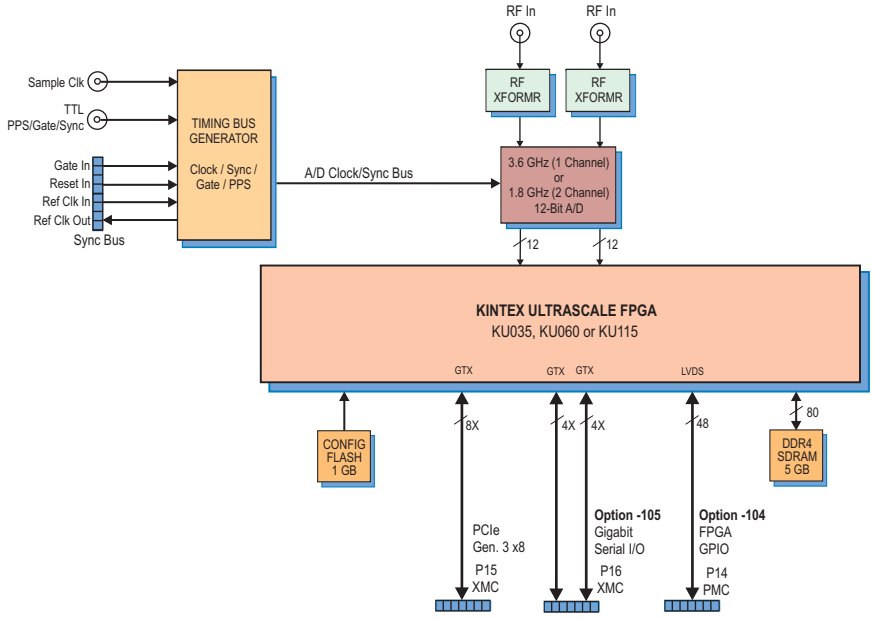
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - XMC

A/D Acquisition IP Module

The 71841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

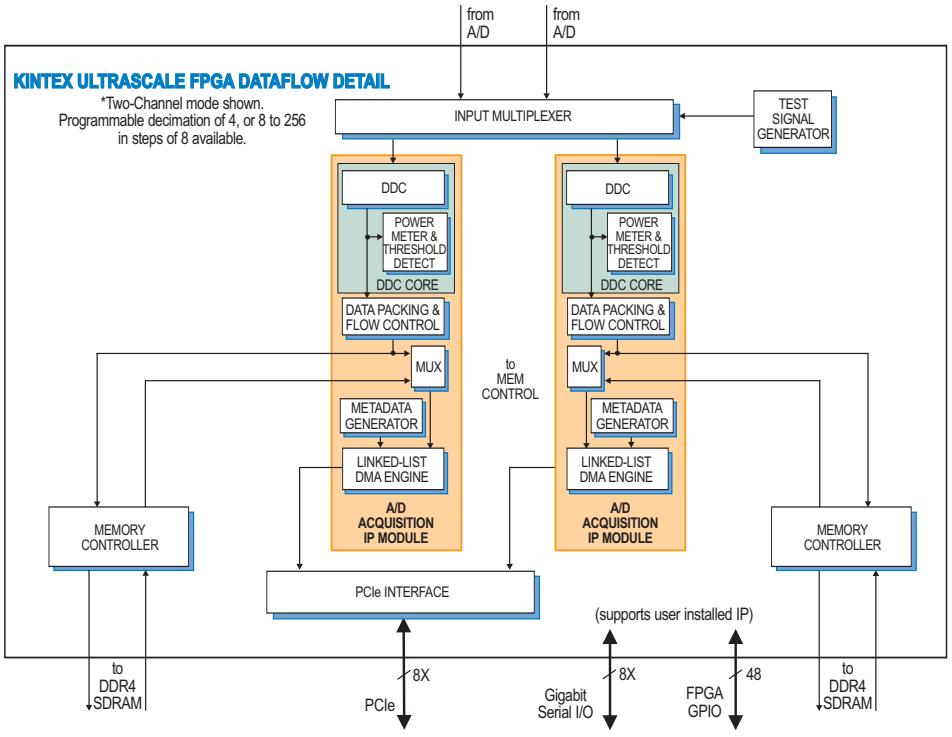
Option -105 installs the P16 XMC connector with 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - XMC

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - XMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through P14 connector
- 105	Gigabit serial FPGA I/O through P16 connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Memory Resources

The 71861 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 71841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 71841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71841's can be synchronized with a simple cable. For larger systems, multiple 71841's can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input Level:** may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Single-channel mode:** decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** the DDC can be bypassed completely
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Standard XMC module, 2.91 in. x 5.87 in.

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New!

Model 71851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

JADE
NAVIGATOR
Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Model 71851 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

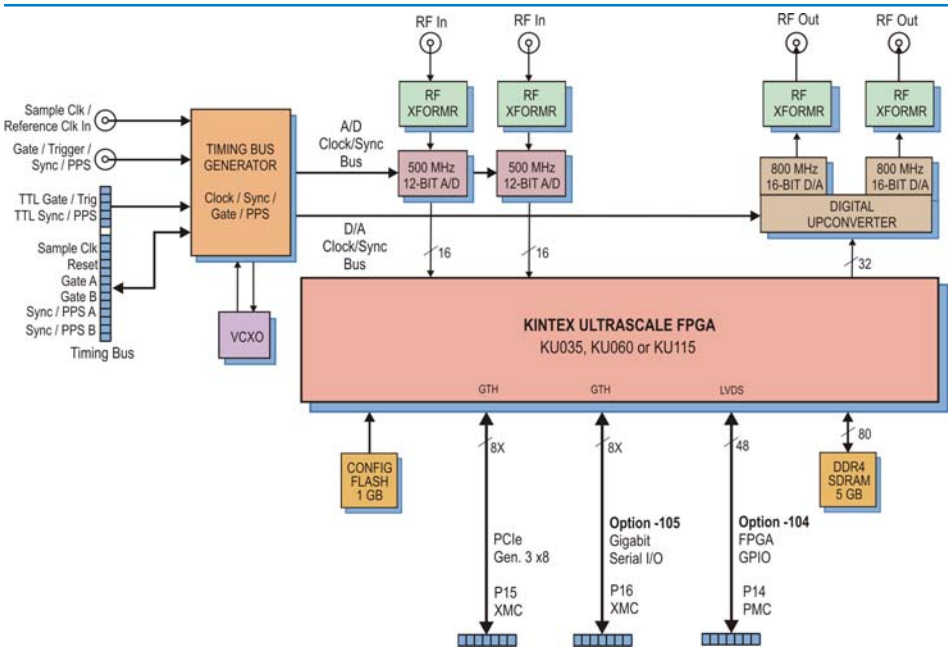
The 71851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 71851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Model 71851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 71851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

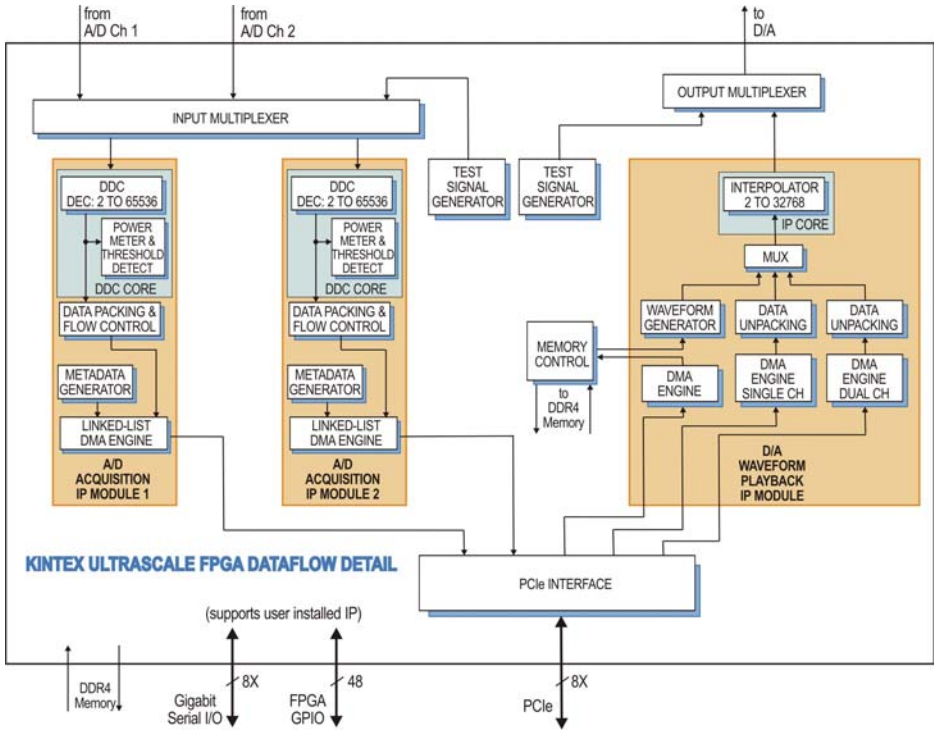
Option -105 provides one 8X gigabit link between the FPGA and the P16 XM C connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

XMC Interface

The Model 71851 complies with the VITA 42.0 XMC specification. Each of two connectors provide a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71851 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

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Model 71851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - XMC
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X gigabit link between the FPGA and XMC P16 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (73.91 mm x 149.10 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Model 71861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71861 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

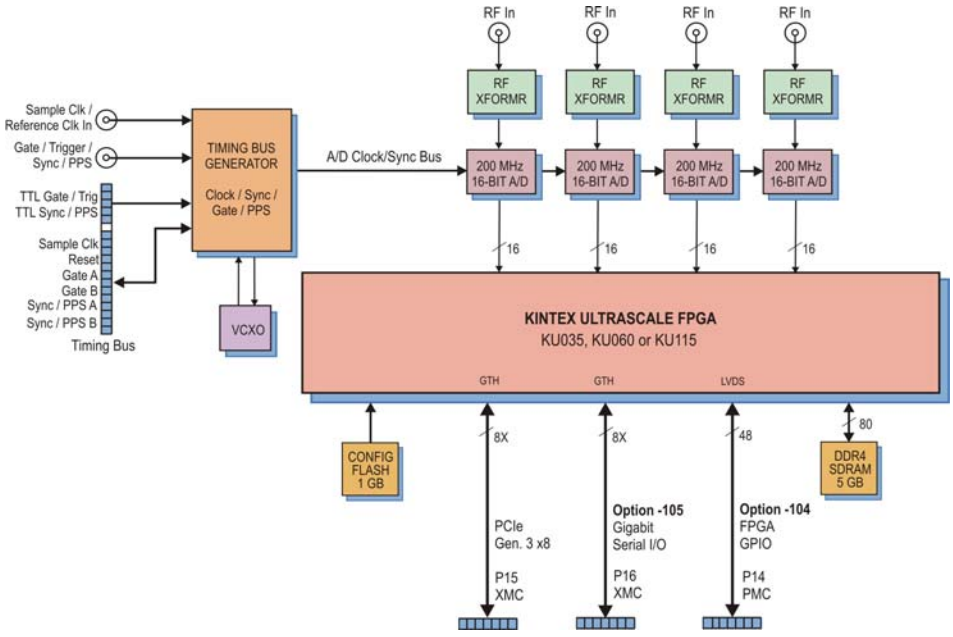
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

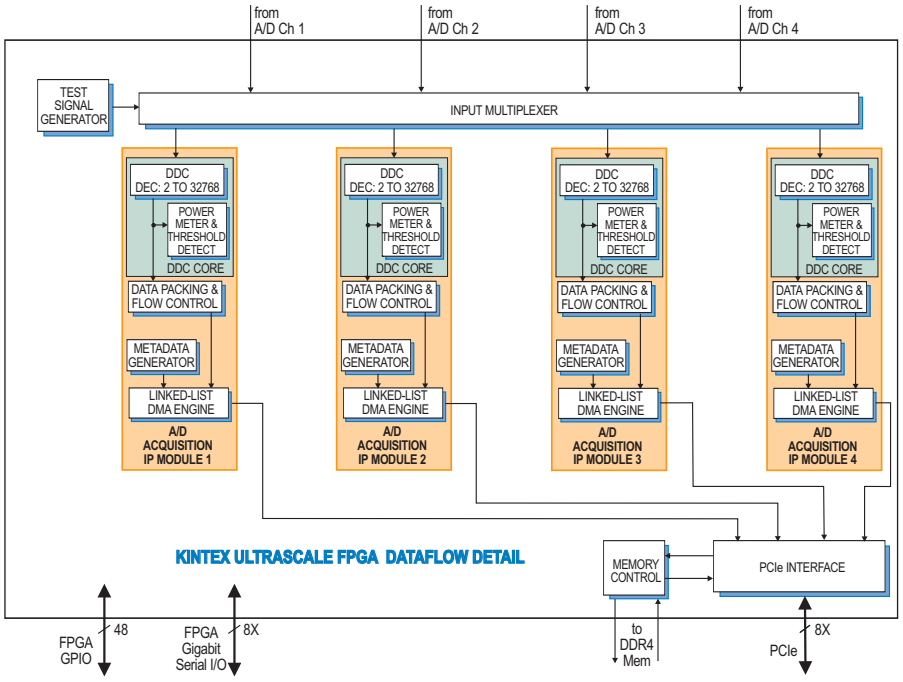
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
71861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through P14 connector
- 105	Gigabit serial FPGA I/O through P16 connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 71861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71861 complies with the VITA 42.0 XMC specification. Each of two connectors provide a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71861 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector with one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

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New!

Model 71862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71862 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

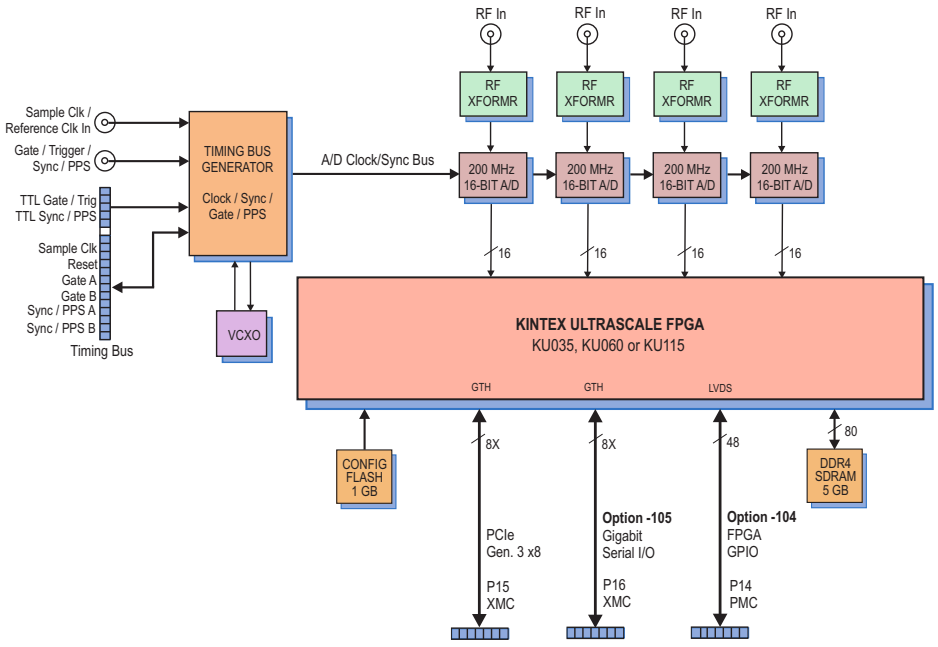
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 71862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

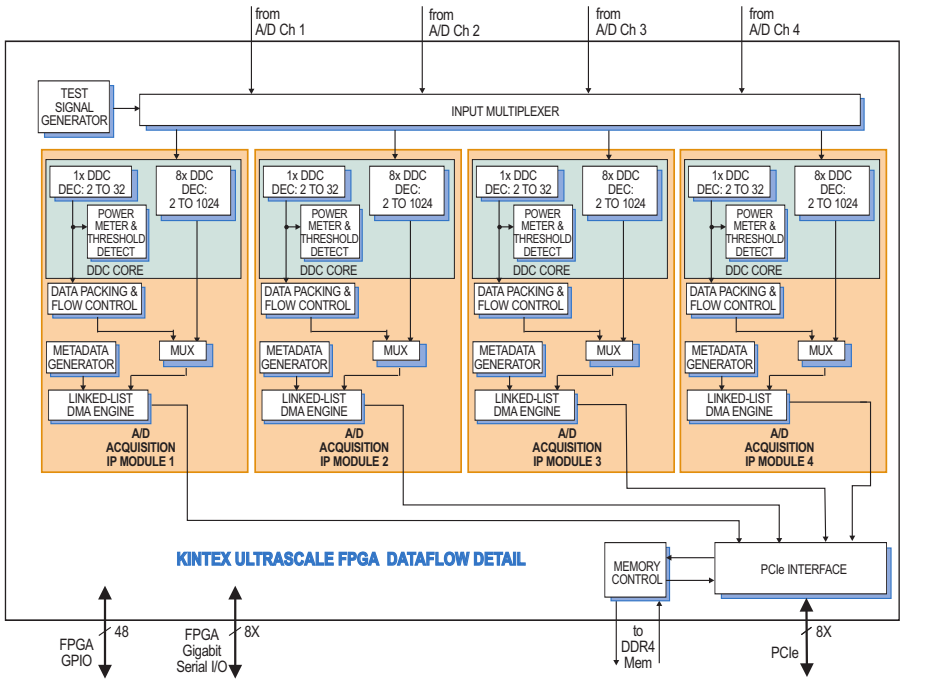
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front-panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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www.pentek.com

Model 71862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - XMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through P14 connector
- 105	Gigabit serial FPGA I/O through P16 connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 71862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71862 complies with the VITA 42.0 XMC specification. Each of two connectors provides a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71862 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Four banks, 8 channels per bank
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector with one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

PENTEK

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New!

Model 71800

Kintex UltraScale FPGA Coprocessor- XMC

JADE NAVIGATOR Design Suite

Features

- Hi-performance co-processor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 71800 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 71800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

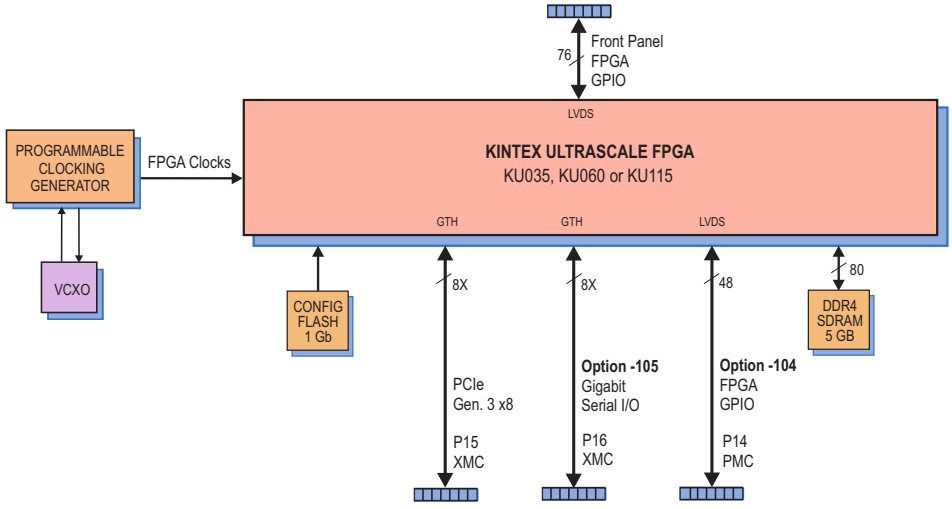
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with an 8X gigabit link to the FPGA to support serial protocols.

Front Panel Digital I/O Interface

The 71800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 71800

Kintex UltraScale FPGA Coprocessor- XMC

Memory Resources

The 71800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71800	Kintex UltraScale FPGA Coprocessor - XMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through P14 connector
- 105	Gigabit serial FPGA I/O through P16 connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 71800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

XMC Interface

The Model 71800 complies with the VITA 42.0 XMC specification. Each of two connectors provides an 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71800 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector with an 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

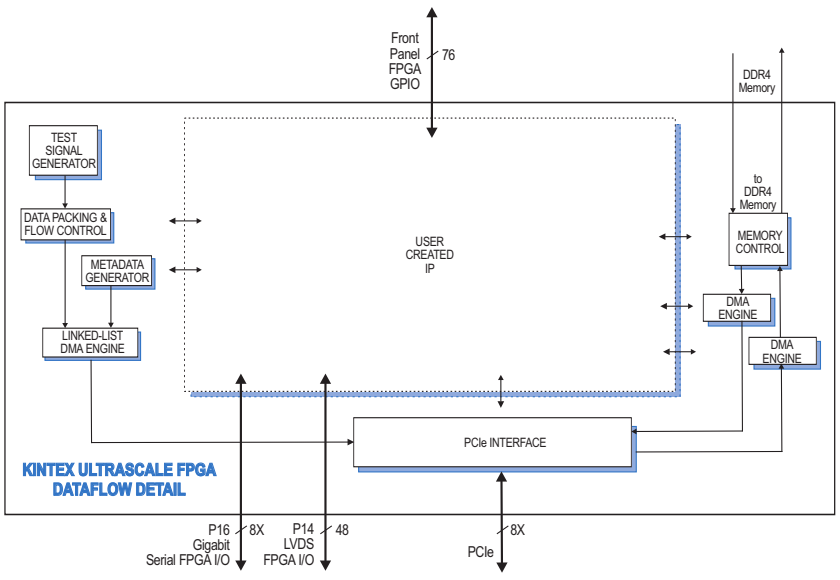
PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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Model 7120

Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC

Bandit

ReadyFlow Board Support Package

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

General Information

The Bandit® Model 7120 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PMC/XMC module with front-panel connectors for easy integration into RF systems, the module offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7120 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 7120 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 7120 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 7120 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

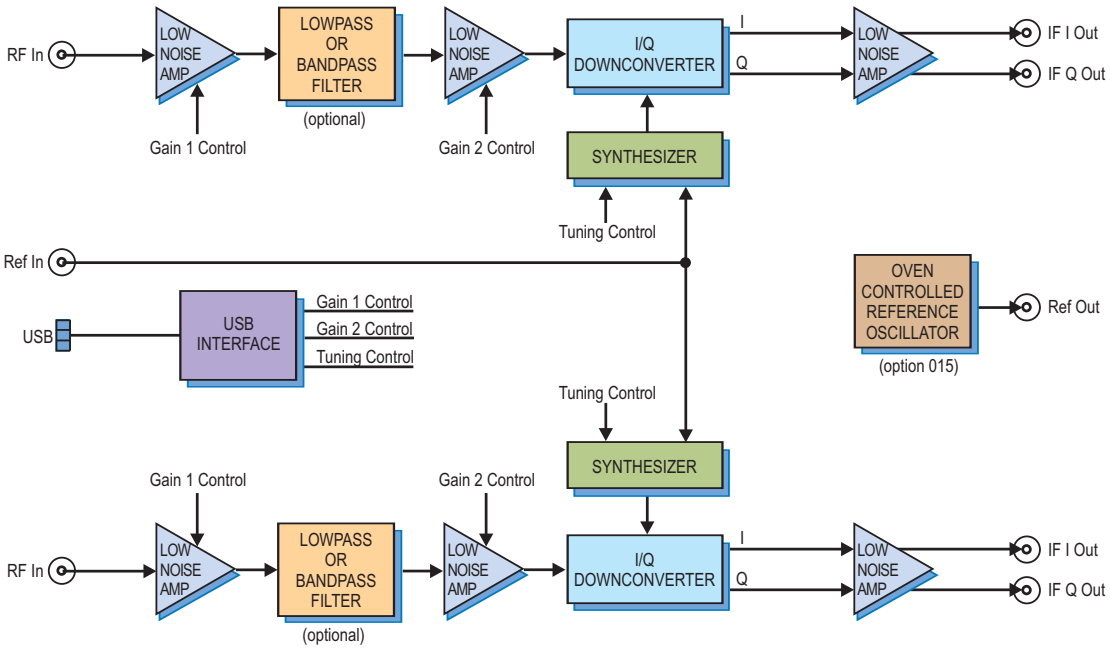
On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 7120 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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Model 7120

Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC

➤ Specifications

RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** –60 dBm to –20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

Phase Noise
- **1 kHz:** –90 dBc/Hz
- **100 kHz:** –110 dBc/Hz
- **1 MHz:** –130 dBc/Hz

Noise Figure (referred to input)
- **60 dB gain:** 2.6 dB

Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedence:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

Reference Output Signal
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm
- **Aging**
  - **Daily:** ±10 ppb/day
  - **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm
- **Phase Noise**
  - **1 Hz Offset:** –67 dBc/Hz
  - **10 Hz Offset:** –100 dBc/Hz
  - **100 Hz Offset:** –130 dBc/Hz
  - **1 KHz Offset:** –148 dBc/Hz
  - **10 KHz Offset:** –154 dBc/Hz
  - **100 KHz Offset:** –155 dBc/Hz

IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

PMC/XMC Interface: Power only on PMC P11 (option -104) or XMC P15 (option -105)

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7120	Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC

Option	Description
-015	Oven Controlled Refernece Oscillator
-104	PMC P11 Power
-105	XMC P15 Power
-106	PCIe 6-pin connector (Power only)
-145	1.45 GHz lowpass input filter
-280	2.80 GHz lowpass input filter

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RADAR & SDR I/O - CompactPCI

MODEL	DESCRIPTION
Cobalt 72620, 73620, 74620	3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72621, 73621, 74621	3/6-Ch 200 MHz A/D, DDCs, DUC, 2/4-Ch. 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72624, 73624, 74624	2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - 6U/3U cPCI
Cobalt 72630, 73630, 74630	1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72640, 73640, 74640	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72641, 73641, 74641	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72650, 73650, 74650	2/4 500 MHz A/Ds, 1/2 DUCs, 2/4 800 MHz D/As, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72651, 73651, 74651	2/4-Ch 500 MHz A/D w. DDC, DUC w. 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72660, 73660, 74660	4/8-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72661, 73661, 74661	4/8-Ch 200 MHz A/D with DDCs, Beamformer and Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72662, 73662, 74662	4/8-Ch 200 MHz A/D with 32/64-Ch DDC and Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72663, 73663, 74663	1100/2200-Channel GSM Channelizer with Quad or Octal A/D - 6U/3U cPCI
Cobalt 72664, 73664, 74664	4/8-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72670, 73670, 74670	4/8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72671, 73671, 74671	4/8-Ch 1.25 GHz D/A with DUC, Extend. Interpol. and Virtex-6 FPGA - 6U/3U cPCI
Cobalt 72690, 73690, 74690	1/2-Ch L-Band RF Tuner, 2/4-Ch 200 MHz A/D, Virtex-6 FPGA - 6U/3U cPCI
Onyx 72720, 73720, 74720	3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI
Onyx 72721, 73721, 74721	3/6-Ch 200 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI
Onyx 72730, 73730, 74730	1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-7 FPGA - 6U/3U cPCI
Onyx 72741, 73741, 74741	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz, 12-bit A/D, DDC,Virtex-7 FPGA - 6U/3U cPCI
Onyx 72751, 73751, 74751	2/4-Ch 500 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI
Onyx 72760, 73760, 74760	4/8-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U/3U cPCI
Onyx 72761, 73761, 74761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 6U/3U cPCI
Onyx 72791, 73791, 74791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 6U/3U cPCI
Jade 72131, 73131, 74131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U/3U cPCI
Jade 72132, 73132, 74132	8-Ch. 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U/3U cPCI
Jade 72141, 73141, 74141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex FPGA - 6U/3U cPCI
Jade 72821, 73821, 74821	3-Chan. 200 MHz A/D, DDC, DUC 2-Ch. 800 MHz D/A, Kintex FPGA - 6U/3U cPCI
Jade 72841, 73841, 74841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex FPGA - 6U/3U cPCI
Jade 72851, 73851, 74851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex FPGA - 6U/3U cPCI
Jade 72861, 73861, 74861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - 6U/3U cPCI
Jade 72862, 73862, 74862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - 6U/3U cPCI
Jade 72800, 73800, 74800	Kintex UltraScale FPGA Coprocessor - 3U/6U cPCI
Bandit 7220, 7320, 7420	Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI
	Customer Information

RADAR & SDR I/O - PMC/XMC

Click Here for the PRODUCT SELECTOR

RADAR & SDR I/O - x8 PCI Express

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RADAR & SDR I/O - AMC

RADAR & SDR I/O - 3U VPX - FORMAT 2

RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated: March 2018

Models 72620 73620 and 74620

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

Model 74620 *Model 73620*

General Information

Models 72620, 73620 and 74620 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71620 XMC modules mounted on a cPCI carrier board.

Model 72620 is a 6U cPCI board while the Model 73620 is a 3U cPCI board; both are equipped with one Model 71620 XMC. Model 74620 is a 6U cPCI board with two XMC modules rather than one.

These models include three or sixA/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

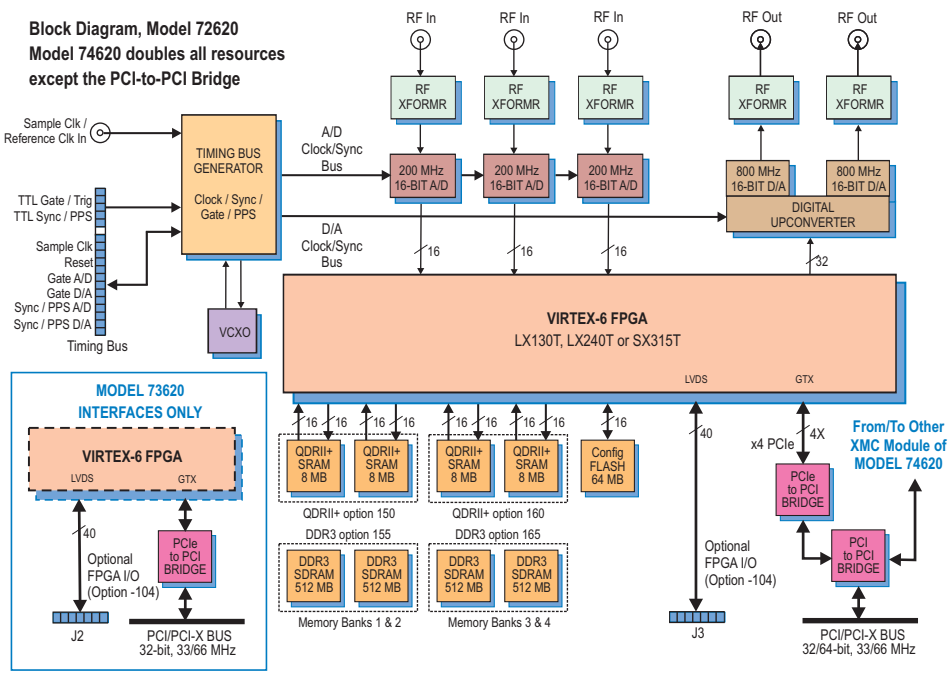
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73620; J3 connector, Model 72620; J3 and J5 connectors, Model 74620. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Models 72620 73620 and 74620

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

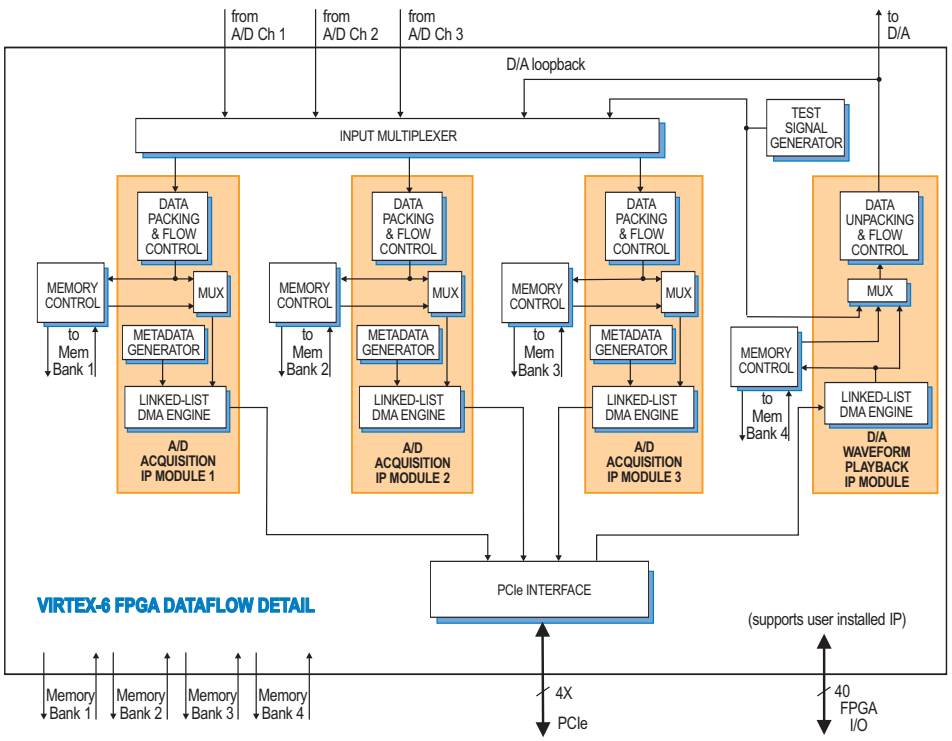
Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73620: 32 bits only.

Specifications

Model 72620 or Model 73620: 3 A/Ds, 1 DUC, 2 D/As
Model 74620: 6 A/Ds, 2 DUCs, 4 D/As
Front Panel Analog Signal Inputs (3 or 6)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits
Front Panel Analog Signal Outputs (2 or 4)
Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73620; J3 connector, Model 72620; J3 and J5 connectors, Model 74620
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73620: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 6U cPCI
73620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 3U cPCI
74620	6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A and two Virtex-6 FPGAs - 6U cPCI
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73620; J3 connector, Model 72620; J3 and J5 connectors, Model 74620
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model 72621, 73621 and 74621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

Model 74621 *Model 73621*

General Information

Models 72621, 73621 and 74621 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71621 XMC modules mounted on a cPCI carrier board.

Model 72621 is a 6U cPCI board while the Model 73621 is a 3U cPCI board; both are equipped with one Model 71621 XMC. Model 74621 is a 6U cPCI board with two XMC modules rather than one.

These models include three or six A/Ds, three or six multiband DDCs, one ot two DUCs, two or four D/As and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

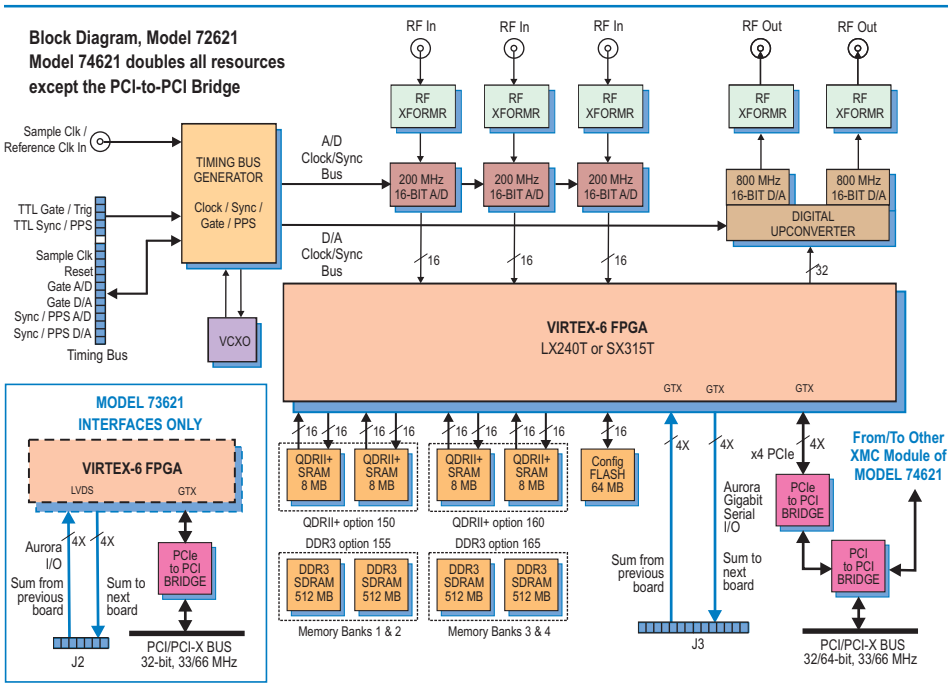
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization



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Model 72621, 73621 and 74621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

➤ A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

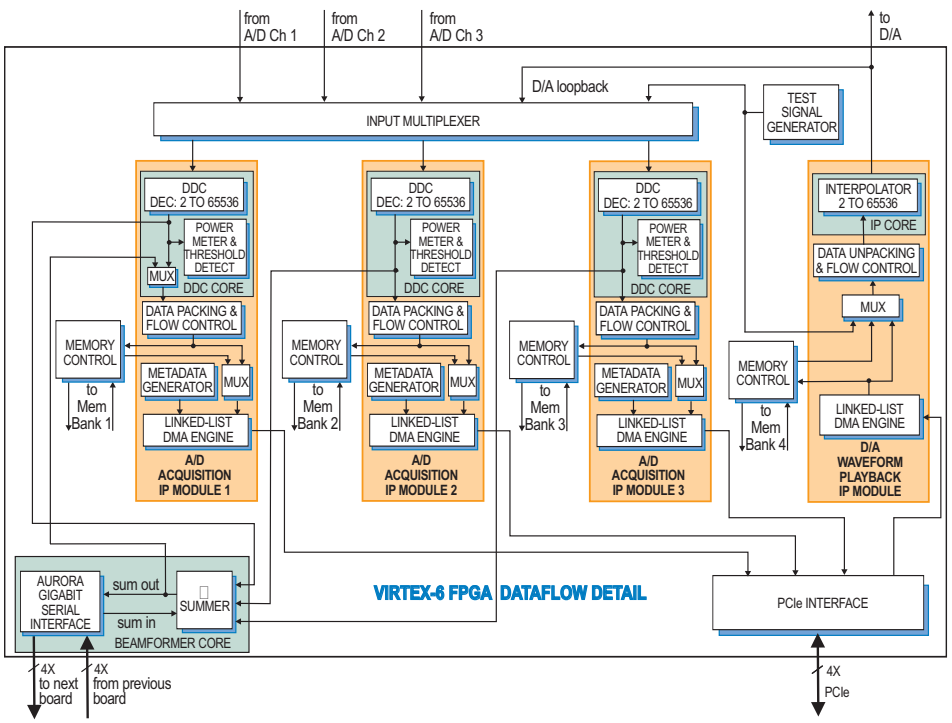
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via the built-in Xilinx Aurora gigabit serial interfaces through the J3 and J5 connectors. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions include sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73621: 32 bits only. ➤

Model 72621, 73621 and 74621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

Ordering Information

Model	Description
72621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U cPCI
73621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U cPCI
74621	6-Channel 200 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U cPCI
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

➤ Specifications

Model 72621 or Model 73621: 3 A/Ds, 3 DDCs, 1 DUC, 2 D/As

Model 74621: 6 A/Ds, 6 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (3 or 6)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via J3 connector using Aurora protocol; via J3 and J5 for Model 74621
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73621: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

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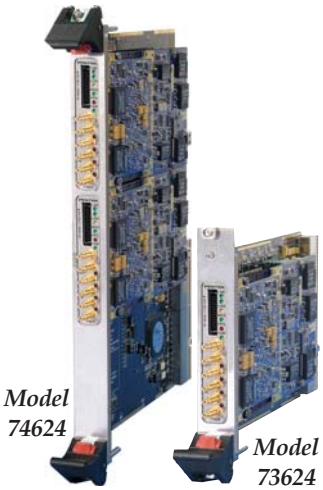
New!

Models 72624 73624 and 74624

2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI



Features

- Modifies 34 or 68 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two/four 200 MHz 16-bit A/Ds
- Two/four 800 MHz 16-bit D/As
- 34/68 DDCs and 34/68 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI-X system interface

General Information

Models 72624, 73624 and 74624 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71624 XMC modules mounted on a cPCI carrier board. Model 72624 is a 6U cPCI board while the Model 73624 is a 3U cPCI board; both are equipped with one Model 71624 XMC. Model 74624 is a 6U cPCI board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board

These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCI-X system interface supports control, status and data transfers.

Adaptive Relay Input Overview

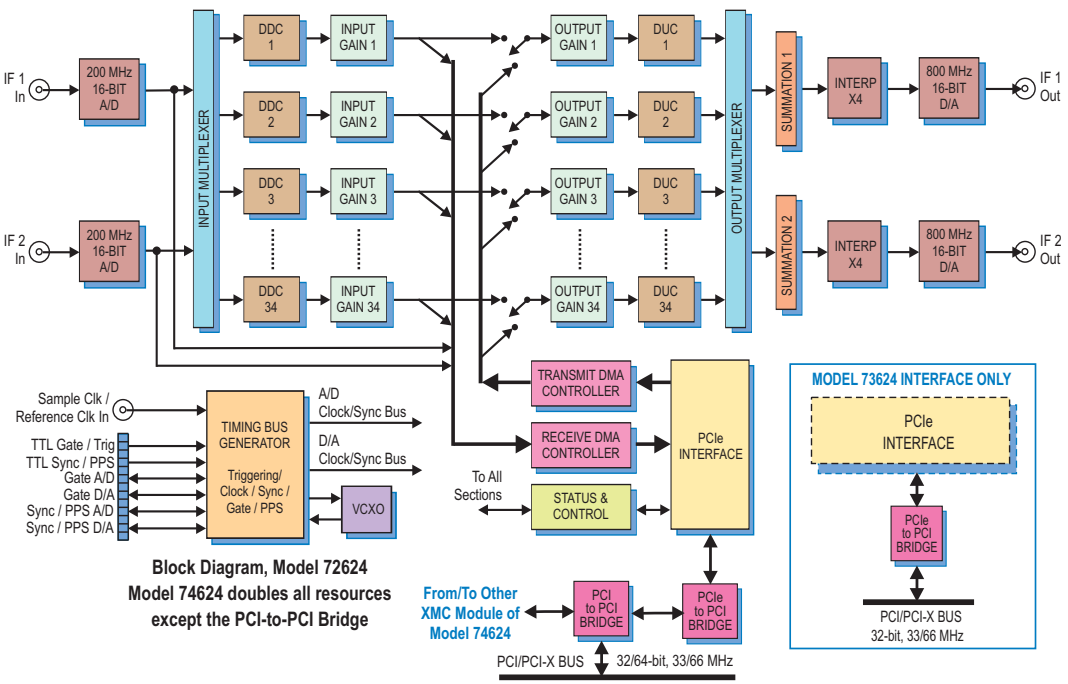
These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCI-X system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCI-X to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The output stage of these models consists of 34 or 68 DUCs (digital upconverters) and two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q ➤



Block Diagram, Model 72624
Model 74624 doubles all resources except the PCI-to-PCI Bridge

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➤ signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the adaptive relay of these models. Because of the complexity and proprietary nature of these functions, the FPGAs cannot be extended or modified by the user.

A/D Converters

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 or 68 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controllers

Two or four output DMA engines deliver data across the PCI-X interface into user-specified memory locations in PCI-X target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs of the first XMC module. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of Model 74624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begin filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCI-X target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB. ➤

➤ Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

One or two TI DAC5688 dual-channel D/As accept the summed upconverted data streams, one from each summation block, and operate in their non-translating dual, real baseband mode. Their built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

Clocking and Synchronization

Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from one or two on-board programmable VCXOs (voltage-controlled crystal oscillators). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73624: 32 bits only.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI

Ordering Information

Model	Description
72624	Dual-Channel 34-Signal Adaptive IF Relay - 6U cPCI
73624	Dual-Channel 34-Signal Adaptive IF Relay - 3U cPCI
74624	Quad-Channel 68-Signal Adaptive IF Relay - 6U cPCI
Options:	
-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

➤ Specifications

Models 72624 & 73624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As

Model 74624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2 or 4
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34 or 68
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/–48 dB

Output Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/–48 dB

Digital Upconverters
- **Quantity:** 34 or 68
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2 or 4
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
On-board clock synthesizers generate two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
- **Type:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Required:** Xilinx Virtex-6 XC6VSX315T

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
  Model 73624: 32 bits only

Environmental

Standard:
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Option 702 L2 Extended Temp (air-cooled):
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-cond.

Option 712 L2 Extended Temp (conduction-cooled):
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

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Models 72630, 73630 and 74630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - cPCI

Model 74630 *Model 73630*

General Information

Models 72630, 73630 and 74630 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a cPCI carrier board.

Model 72630 is a 6U cPCI board while the Model 73630 is a 3U cPCI board; both are equipped with one Model 71630 XMC. Model 74630 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP module. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these modles to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

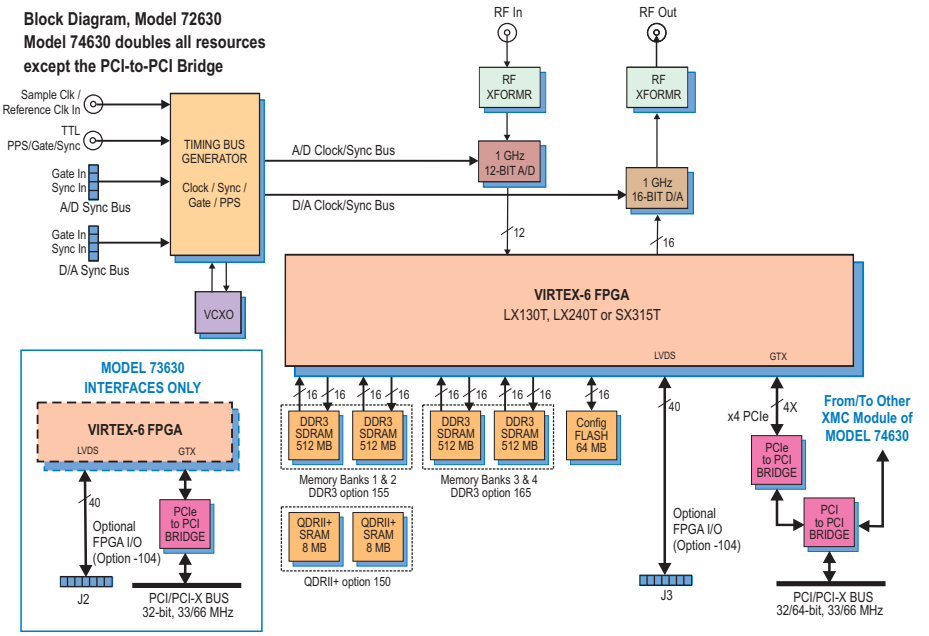
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Models 72630, 73630 and 74630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - cPCI

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts one or two analog HF or IF input on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to acept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

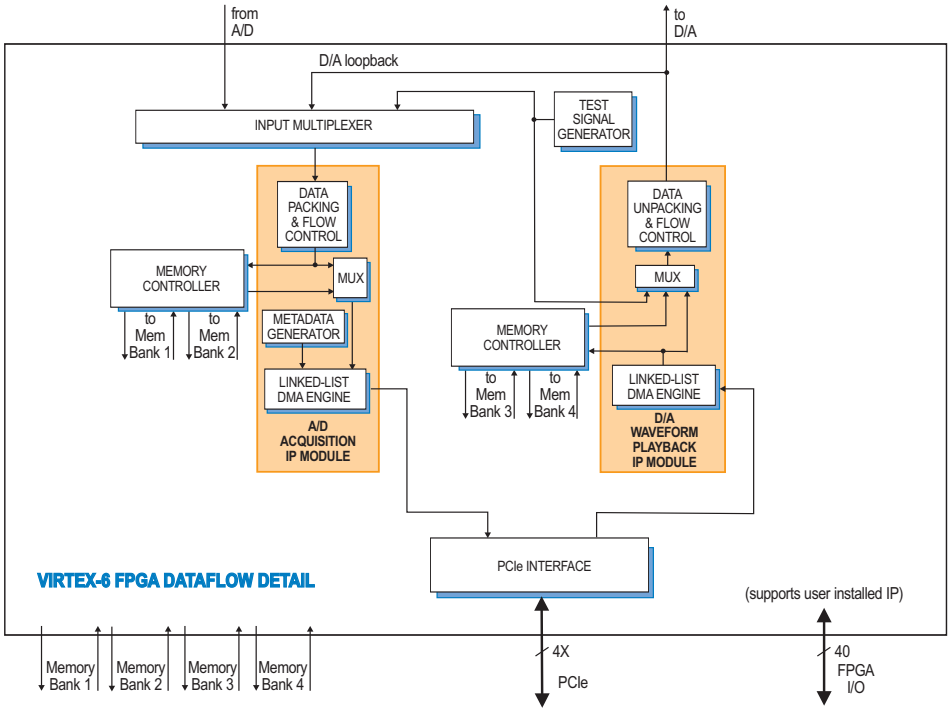
A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7292 and Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Models 72630, 73630 and 74630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73630: 32 bits only.

Specifications

Model 72630 or Model 73630: 1 A/D, 1 D/A
Model 74630: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converters (1 or 2)
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)
Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630

Memory Banks (1 or 2)
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73630: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72630	1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI
73630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U cPCI
74630	Two 1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

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Models 72640, 73640 and 74640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

Model 74640 *Model 73640*

General Information

Models 72640, 73640 and 74640 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board.

Model 72640 is a 6U cPCI board while the Model 73640 is a 3U cPCI board; both are equipped with one Model 71640 XMC. Model 74640 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

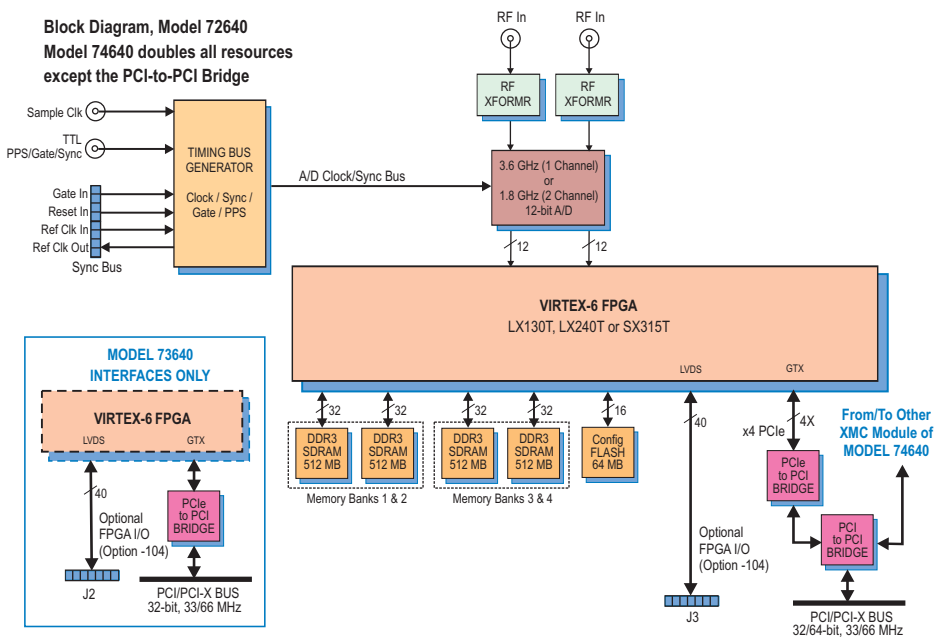
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 or 4 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

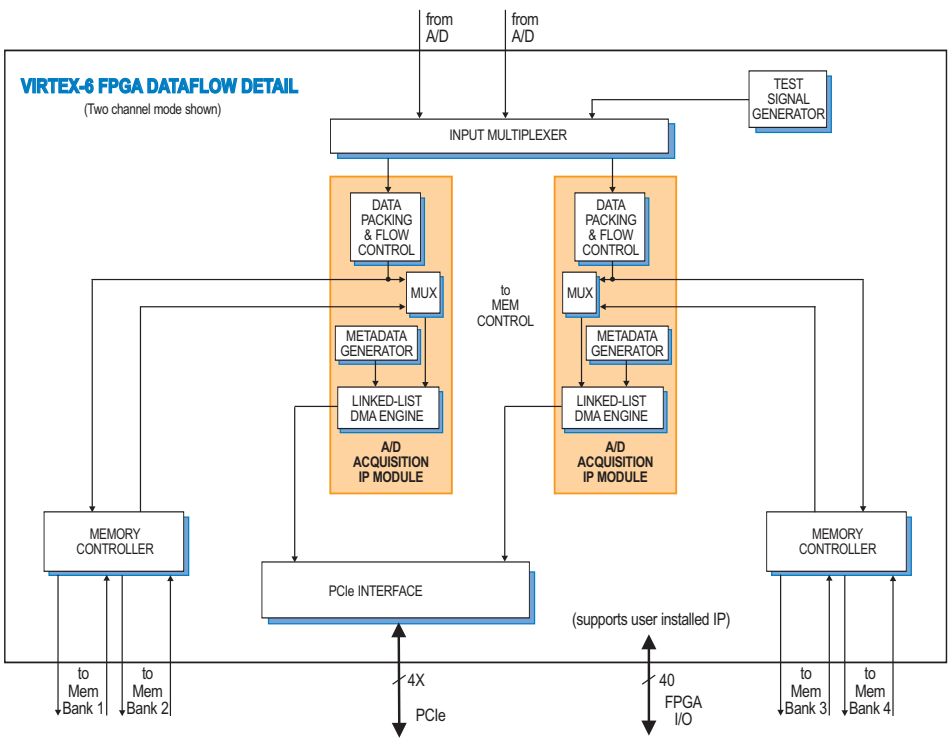
Memory Resources

The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73640: 32 bits only. ➤



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Models 72640, 73640 and 74640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

➤ Specifications

Model 72640 or Model 73640: One A/D
Model 74640: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Sync Bus (1 or 2)
Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640

Memory Banks (1 or 2)
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73640: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI
73640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U cPCI
74640	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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Models 72641, 73641 and 74641

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - cPCI

Model 74641 *Model 73641*

General Information

Models 72641, 73641 and 74641 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71641 XMC modules mounted on a cPCI carrier board.

Model 72641 is a 6U cPCI board while the Model 73641 is a 3U cPCI board; both are equipped with one Model 71641 XMC. Model 74641 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73641; J3 connector, Model 72641; J3 and J5 connectors, Model 74641.

A/D Converter Stage

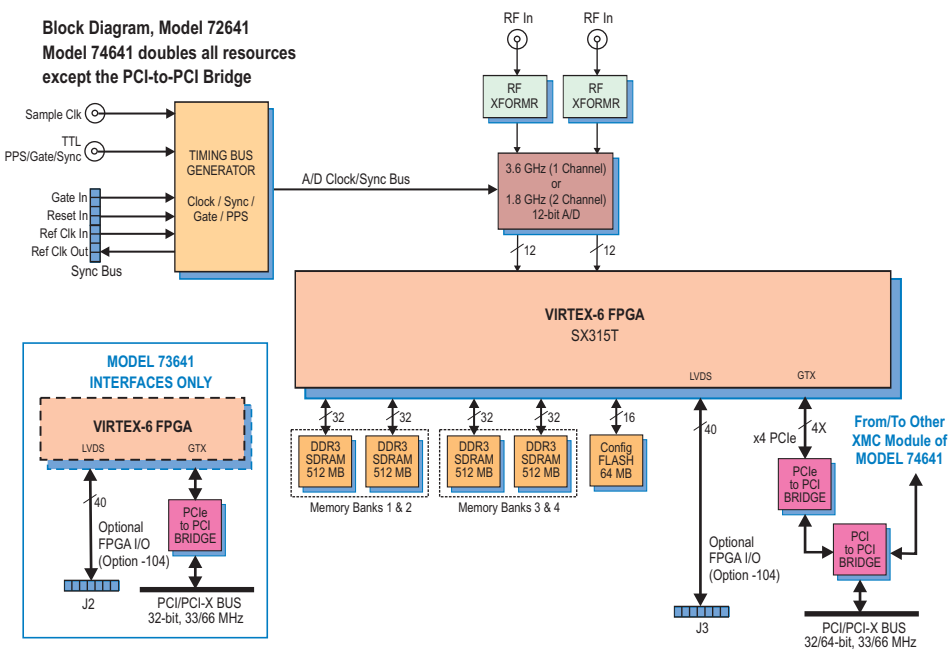
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

Features

- Ideal radar and software radio interface solution
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 or 4 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.
In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

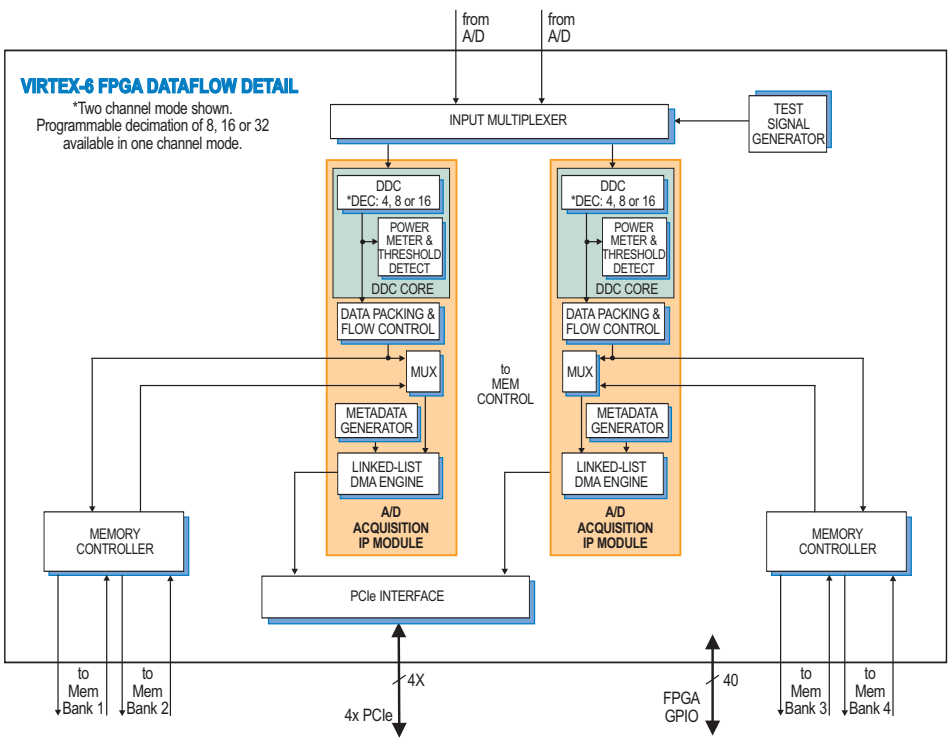
Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Models 72641, 73641 and 74641

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - cPCI

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73641: 32 bits only.

Specifications

Model 72641 or Model 73641: One A/D
Model 74641: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Sync Bus (1 or 2)
Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640

Memory Banks (1 or 2)
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73641: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U cPCI
73641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U cPCI
74641	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U cPCI

Options:

-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS I/O between the FPGA and J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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Models 72650, 73650 and 74650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

Model 74650 Model 73650

General Information

Models 72650, 73650 and 74650 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71650 XMC modules mounted on a cPCI carrier board.

Model 72650 is a 6U cPCI board while the Model 73650 is a 3U cPCI board; both are equipped with one Model 71650 XMC. Model 74650 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, one or two DUCs, two or four D/As and four banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these modles include two or four A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

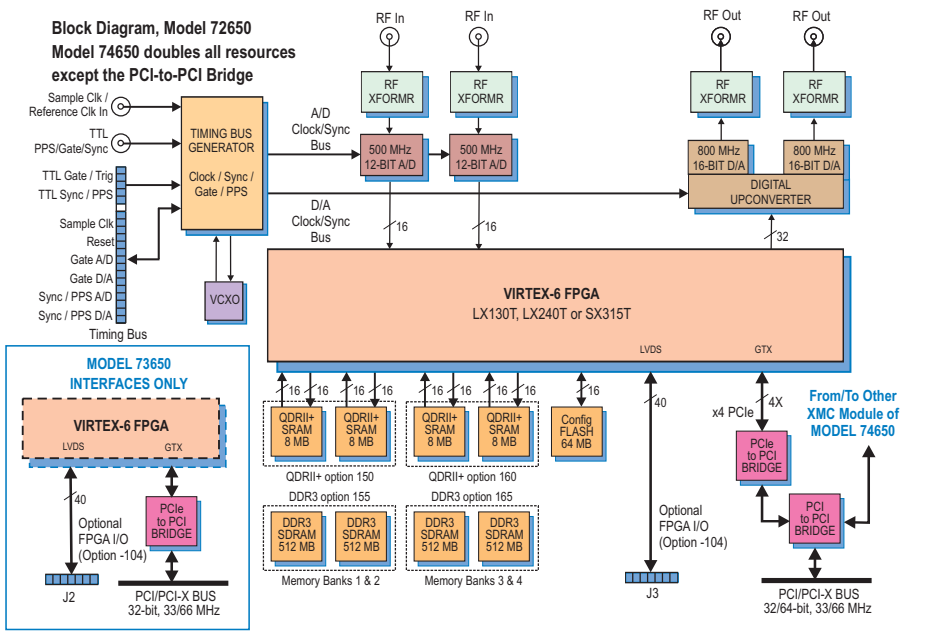
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Models 72650, 73650 and 74650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs and D/As accept a baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

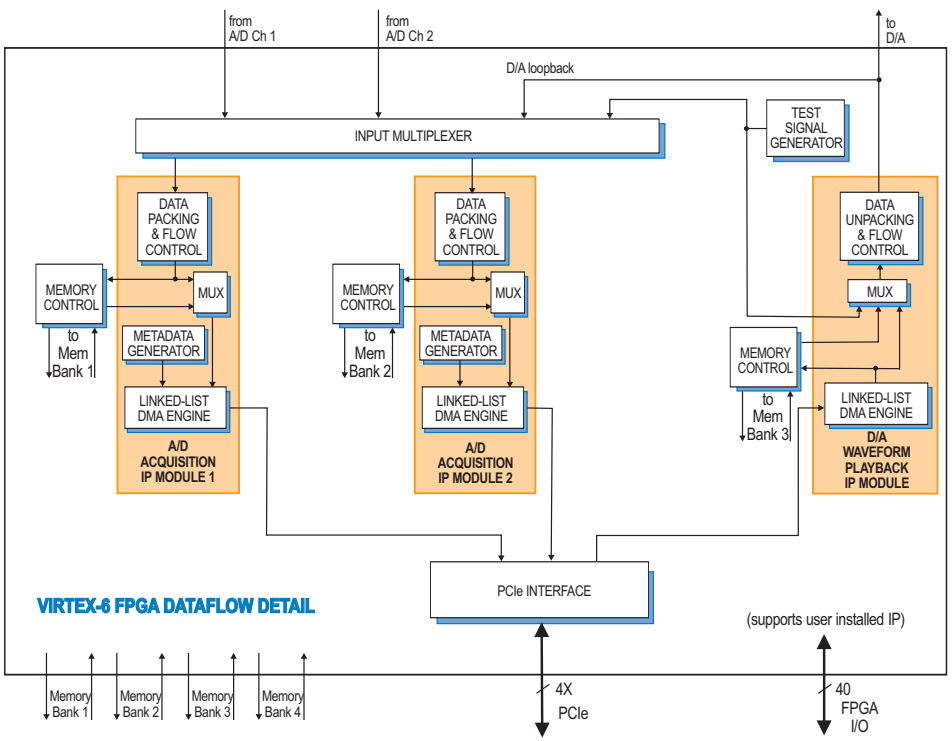
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Models 72650, 73650 and 74650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

Ordering Information

Model	Description
72650	Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 6U cPCI
73650	Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 3U cPCI
74650	Four 500 MHz A/Ds, Two DUCs, Four 800 MHz D/As with Virtex-6 FPGA - 6U cPCI

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73650: 32 bits only.

Specifications

Models 72650 and 73650: 2 A/Ds, 1 DUC, 2 D/As

Model 74650: 4 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014) (2 or 4)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73650: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard 6U or 3U cPCI board

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Model 72651, 73651 and 74651

2 or 4-Channel 500 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

Model 74651 Model 73651

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- Two or four 800 MHz 16-bit D/As
- One or two DUCs (digital upconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or 16 or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 72651, 73651 and 74651 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board.

Model 72651 is a 6U cPCI board while the Model 73651 is a 3U cPCI board; both are equipped with one Model 71651 XMC. Model 74651 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As and three or six banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

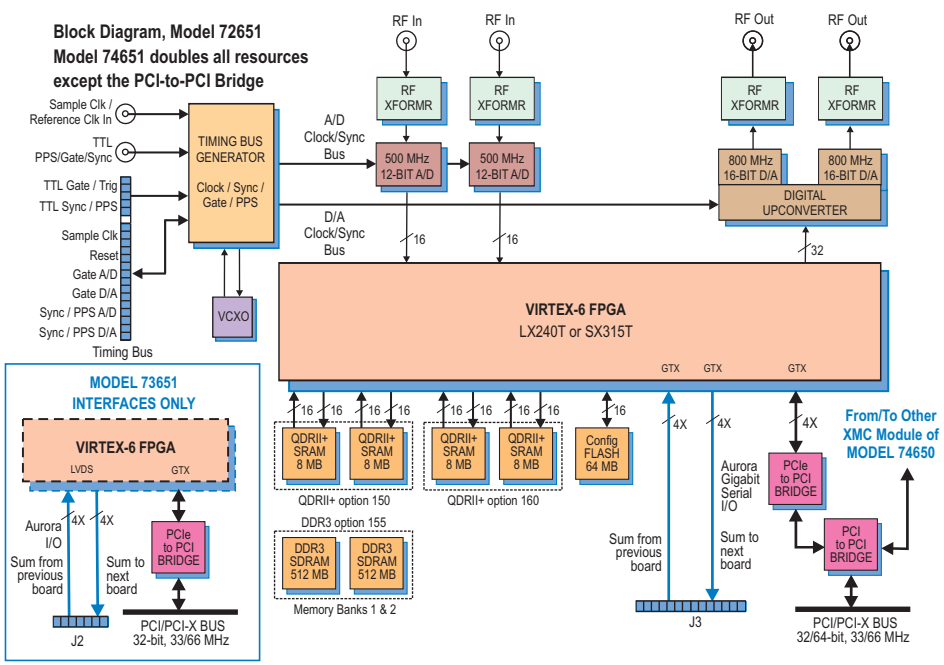
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed. ➤



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www.pentek.com

Model 72651, 73651 and 74651

2 or 4-Channel 500 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

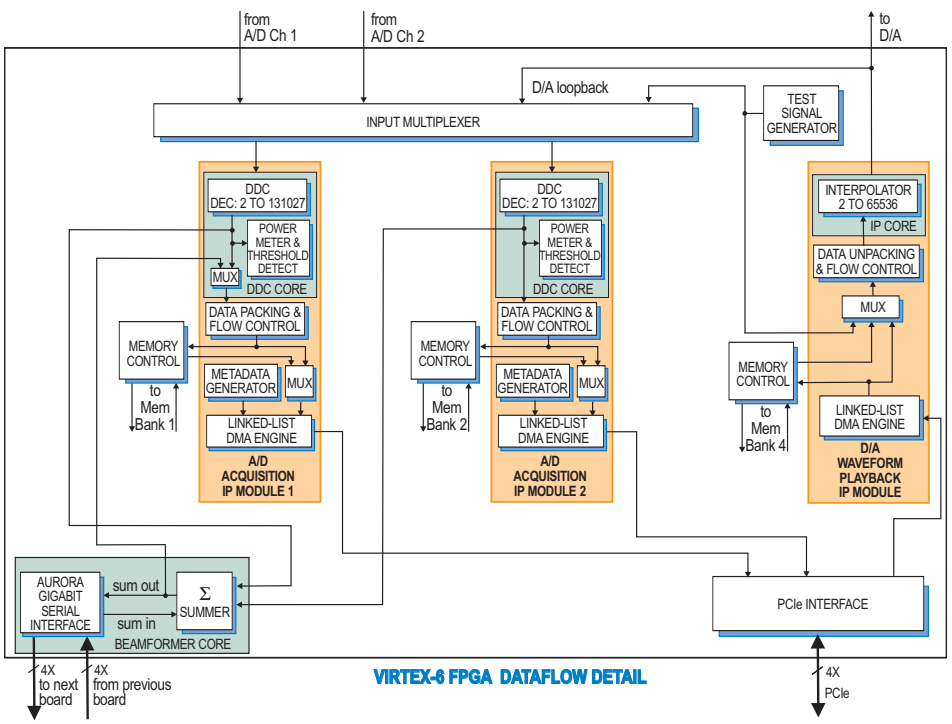
A programmable summation block provides summing of any of the DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple models can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



VIRTEX-6 FPGA DATAFLOW DETAIL

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458

Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

2 or 4-Channel 500 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to three or six independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73651: 32 bits only. ➤

Model 72651, 73651 and 74651

2 or 4-Channel 500 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - cPCI

➤ Specifications

Model 72651 or Model 73651: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

Model 74651: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (Option -014) (2 or 4)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters (2 or 4)
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
- **Summation:** Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via a dual 4X connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Memory (1 or 2)
- **Option -150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option -155 or -165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73651: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U cPCI
73651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U cPCI
74651	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U cPCI

Options:

002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 72660, 73660 and 74660

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - cPCI

Model 74660 *Model 73660*

General Information

Models 72660, 73660 and 74660 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a cPCI carrier board.

Model 72660 is a 6U cPCI board while the Model 73660 is a 3U cPCI board; both are equipped with one Model 71660 XMC. Model 74660 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

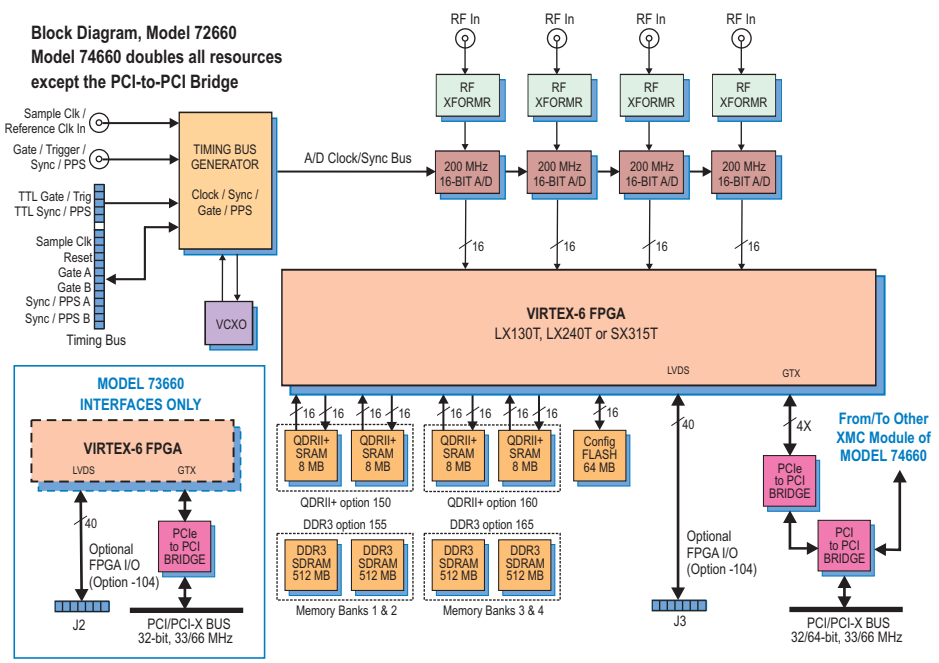
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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www.pentek.com

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - cPCI

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

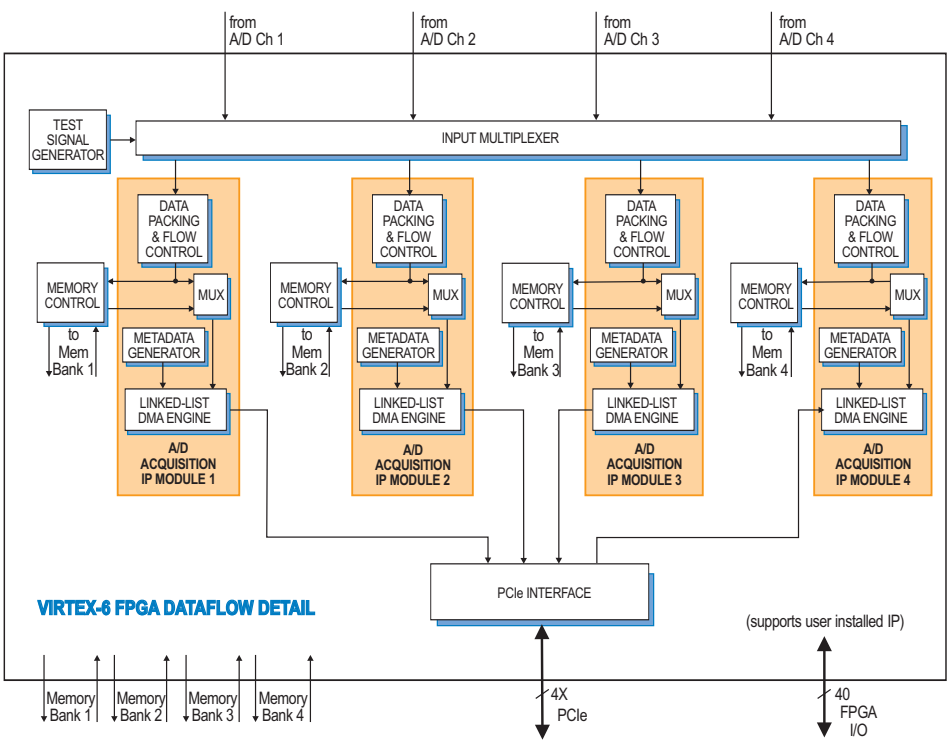
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73660: 32 bits only. ➤

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - cPCI

Specifications

Model 72660 or Model 73660: 4 A/Ds
Model 74660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources (1 or 2)
- On-board clock synthesizers

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73660: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U cPCI
73660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 3U cPCI
74660	8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U cPCI
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Models 72661, 73661 and 74661

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - cPCI

Model 74661 *Model 73661*

General Information

Models 72661, 73661 and 74661 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a cPCI carrier board.

Model 72661 is a 6U cPCI board while the Model 73661 is a 3U cPCI board; both are equipped with one Model 71661 XMC. Model 74661 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, four or eight multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

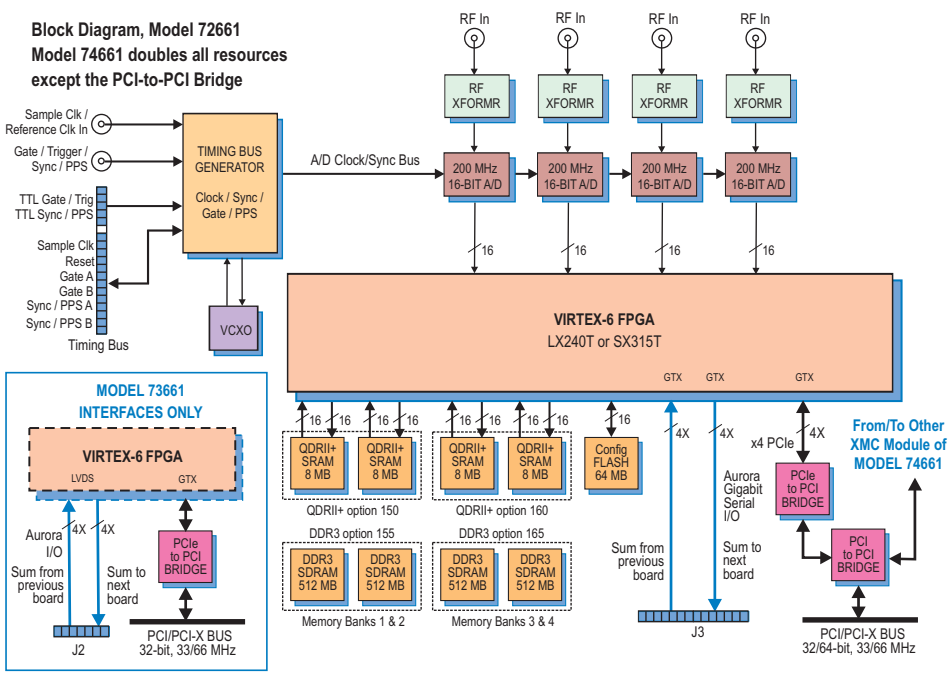
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

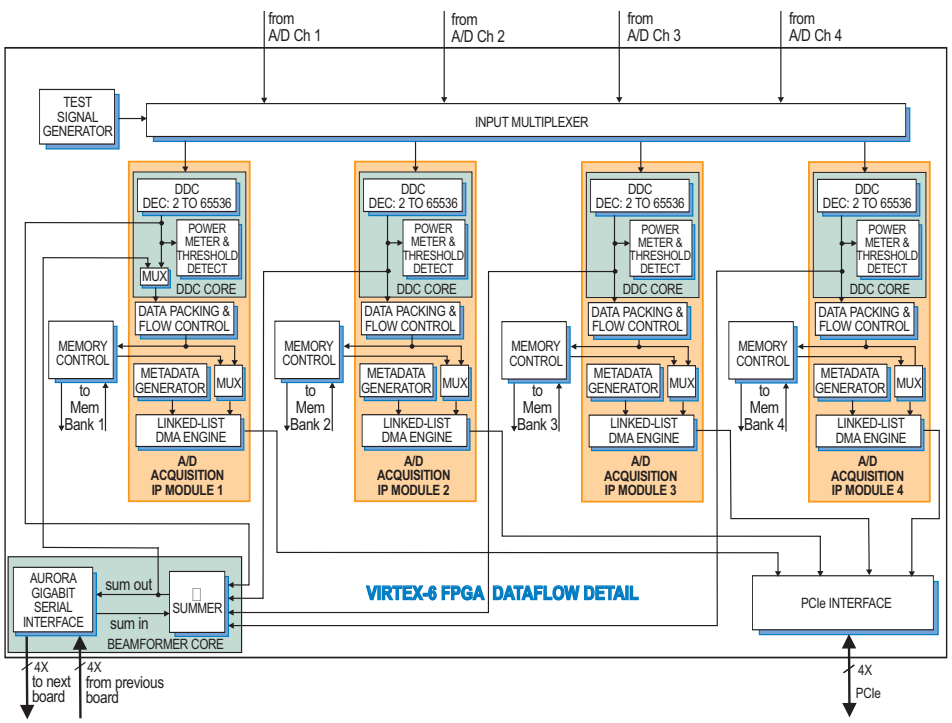
A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ➤



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PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73661: 32 bits only.

Ordering Information

Model	Description
72661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U cPCI
73661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U cPCI
74661	8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGAs - 6U cPCI
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

➤ controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72661 or Model 73661: 4 A/Ds
Model 74660: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (4 or 8)
Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Beamformers (1 or 2)
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73661: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Models 72662, 73662 and 74662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - cPCI

Model 74662 *Model 73662*

General Information

Models 72662, 73662 and 74662 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a cPCI carrier board.

Model 72662 is a 6U cPCI board while the Model 73662 is a 3U cPCI board; both are equipped with one Model 71662 XMC. Model 74662 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, 32 or 64 multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

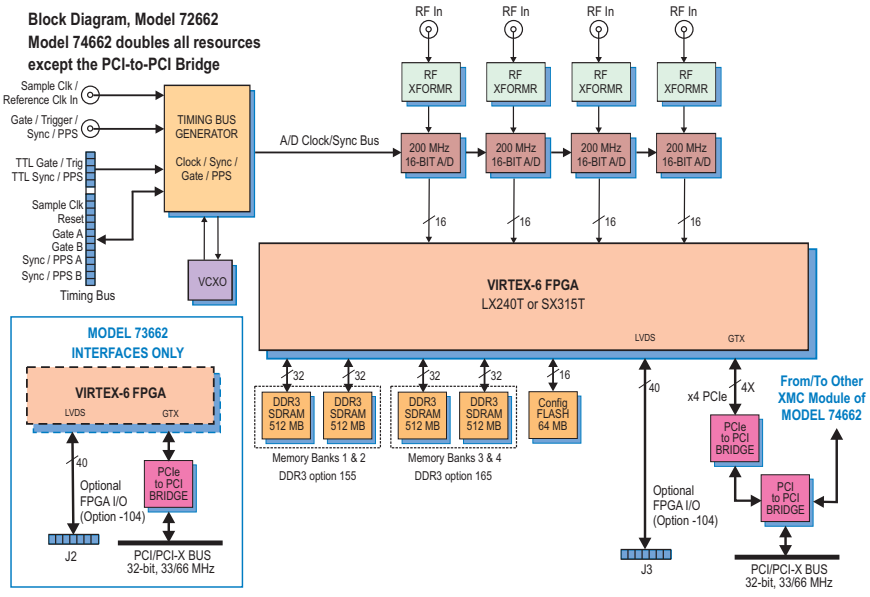
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- 32 or 64 channels of multiband DDCs (digital downconverters)
- Up to 2 or 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Models 72662, 73662 and 74662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

➤ A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

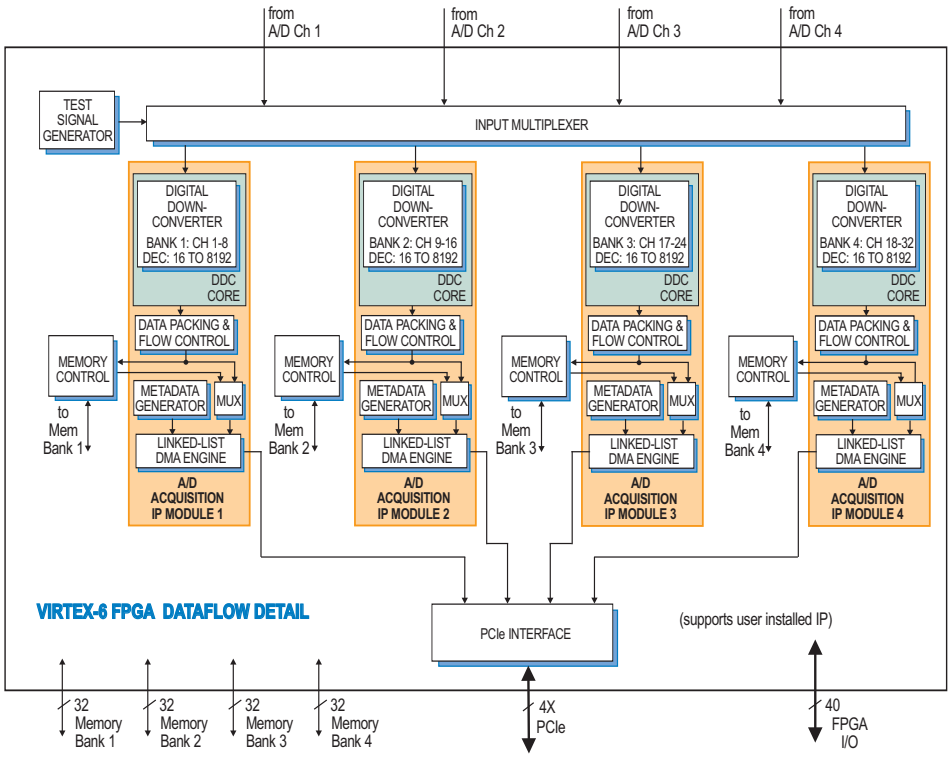
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with DDR3 SDRAM. ➤



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Models 72662, 73662 and 74662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - cPCI

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the Board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73662: 32 bits only.

Specifications

Model 72662 or Model 73662: 4 A/Ds, 32 DDCs
Model 74660: 8 A/Ds, 64 DDCs
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (32 or 64)
Quantity: Four 8-channel banks, one per acquisition module
Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, >100 dB stopband attenuation
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662
MemoryBanks (1 or 2)
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73662: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 6U cPCI
73662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U cPCI
74662	8-Ch 200 MHz A/D with 64-Ch DDC and Virtex-6 FPGA - 6U cPCI
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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New!

Models 72663, 73663 and 74663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

Model 74663 *Model 73663*

Features

- Complete GSM channelizer with analog IF interface
- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 72663, 73663 and 74663 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a cPCI carrier board.

Model 72663 is a 6U cPCI board while the Model 73663 is a 3U cPCI board; both are equipped with one Model 71663 XMC. Model 74663 is a 6U cPCI board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

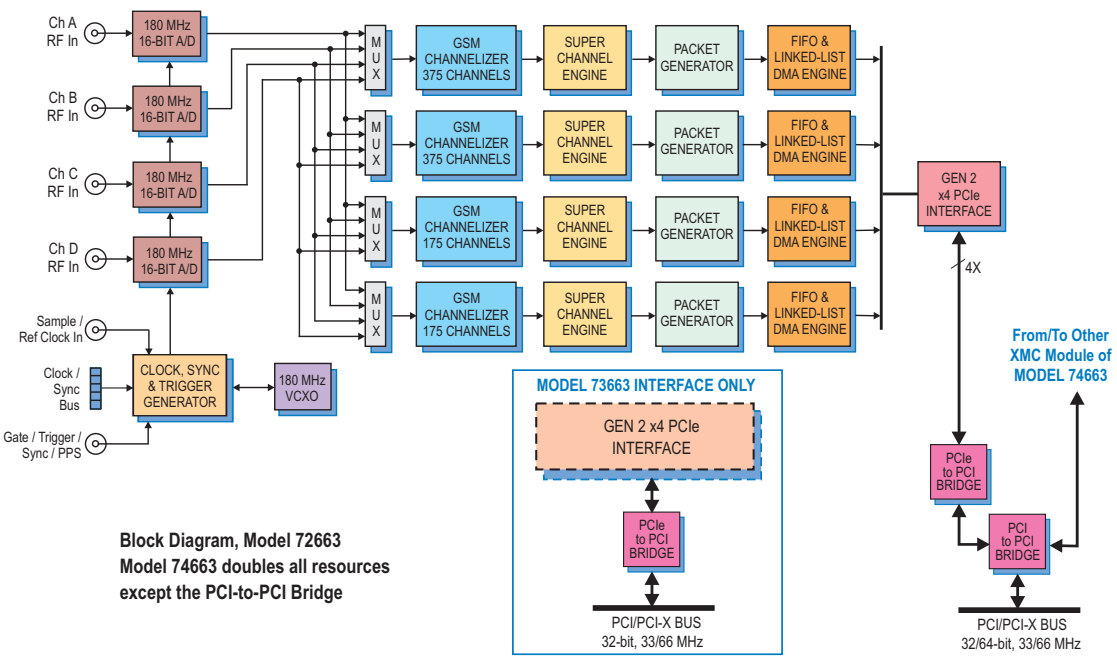
The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤



Block Diagram, Model 72663
Model 74663 doubles all resources except the PCI-to-PCI Bridge

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1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

➤ GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digtitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once compete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73663: 32 bits only.

The PCI-X interface is also used as the programming interface for all status and control between these models and host. ➤

Models 72663, 73663 and 74663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

Specifications

Model 72663 or Model 73663: 4 A/Ds
Model 74663: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
GSM Channel Banks (1 or 2)
DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz
DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 KHz
> 96 dB attenuation at > ±3 MHz
DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
DDC Data Output Format:
24 bits I + 24 bits Q
Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
Frequency Offsets for each DDC:
First: $-f_s/4$ (-270.8333 kHz)
Second: 0 Hz
Third: $+f_s/4$ (+270.8333 kHz)
Fourth: $+f_s/2$ (+541.666 kHz)
Superchannel Sample Rate: f_s
Superchannel Output Format:
26 bits I + 26 bits Q
Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94
Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73663: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72663	1100-Channel GSM Channelizer with Quad A/D - 6U cPCI
73663	1100-Channel GSM Channelizer with Quad A/D - 3U cPCI
74663	2200-Channel GSM Channelizer with Octal A/D - 6U cPCI

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New!

Models 72664, 73664 and 74664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - cPCI

Model 74664 *Model 73664*

General Information

Models 72664, 73664 and 74664 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71664 XMC modules mounted on a cPCI carrier board.

Model 72664 is a 6U cPCI board while the Model 73664 is a 3U cPCI board; both are equipped with one Model 71664 XMC. Model 74664 is a 6U cPCI board with two XMC modules rather than one.

The output of these models supports fully the VITA 49.0 Radio Transport (VRT) Standard.

These models include four or eight A/Ds, four or eight multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

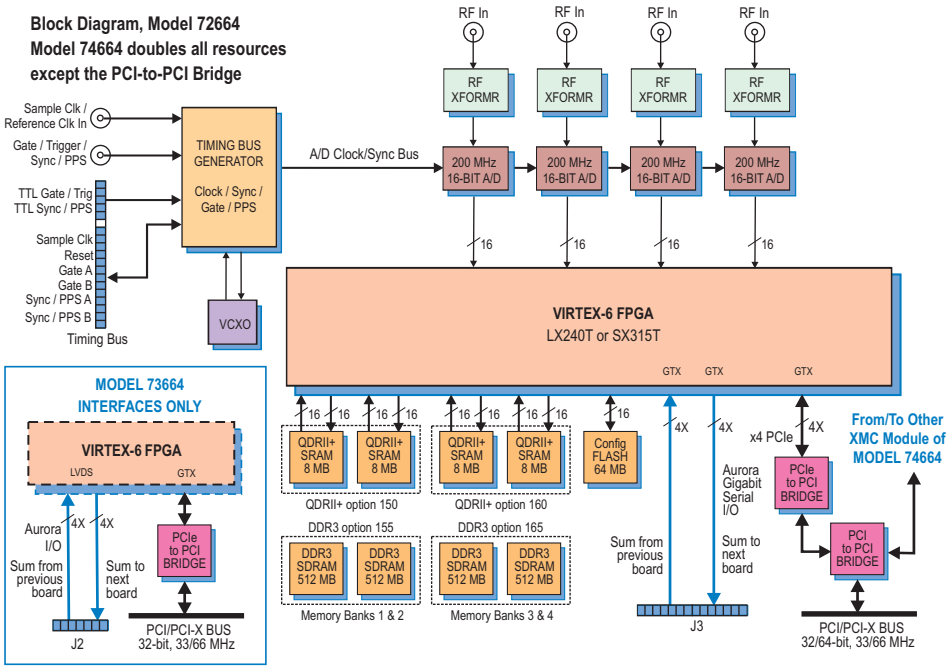
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed. ➤

Features

- Complete radar and software radio interface solutions
- Support VITA 49.0 Radio Transport (VRT) Standard
- Support Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization



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Models 72664, 73664 and 74664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

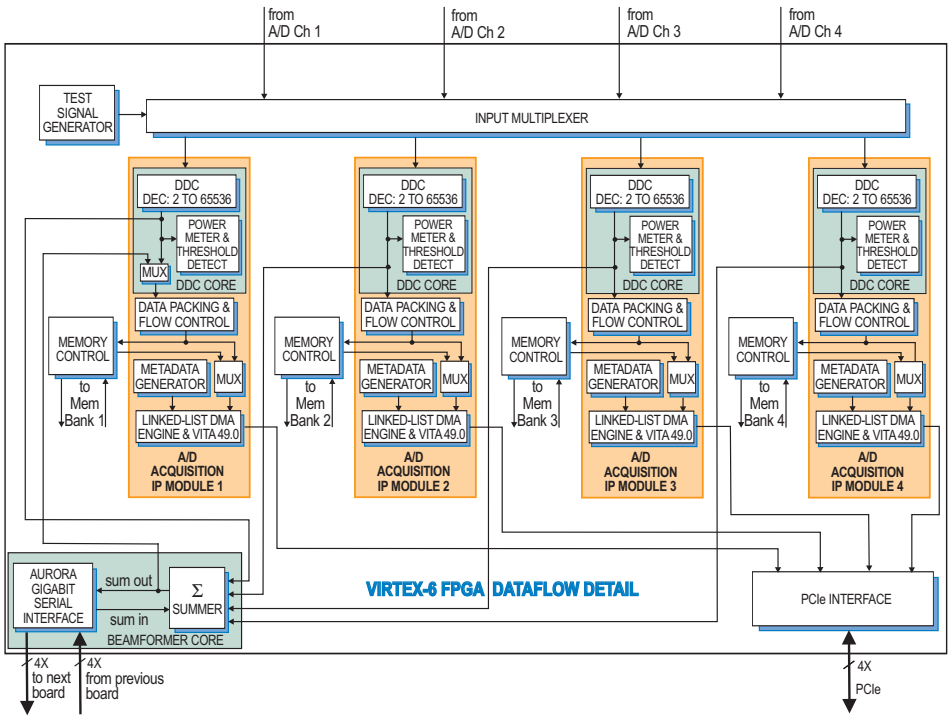
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

These models support fully the VITA 49.0 specification. ➤



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4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - cPCI

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73664: 32 bits only.

Models 72664, 73664 and 74664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - cPCI

Specifications

Model 72664 or Model 73664: 4 A/Ds
Model 74664: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (4 or 8)
Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Beamformers (1 or 2)
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73664: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72664	4-Channel 200 MHz A/D with DDCs, VITA 49.0, one Virtex-6 FPGA - 6U cPCI
73664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 one Virtex-6 FPGA - 3U cPCI
74664	8-Channel 200 MHz A/D with DDCs, VITA 49.0, two Virtex-6 FPGAs - 6U cPCI
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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Models 72670, 73670 and 74670

4- or 8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - cPCI

Model 74670 Model 73670

General Information

Models 72670, 73670 and 74670 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a cPCI carrier board.

Model 72670 is a 6U cPCI board while the Model 73670 is a 3U cPCI board; both are equipped with one Model 71670 XMC. Model 74670 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight D/As, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eightD/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

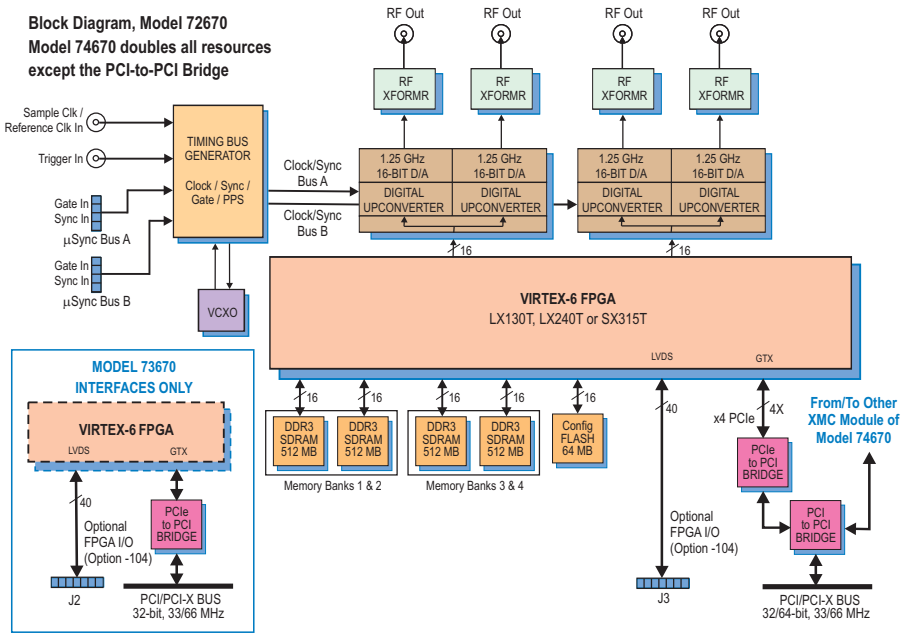
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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4- or 8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - cPCI

➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7292, 7392 and 7492 or the 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73670: 32 bits only. ➤

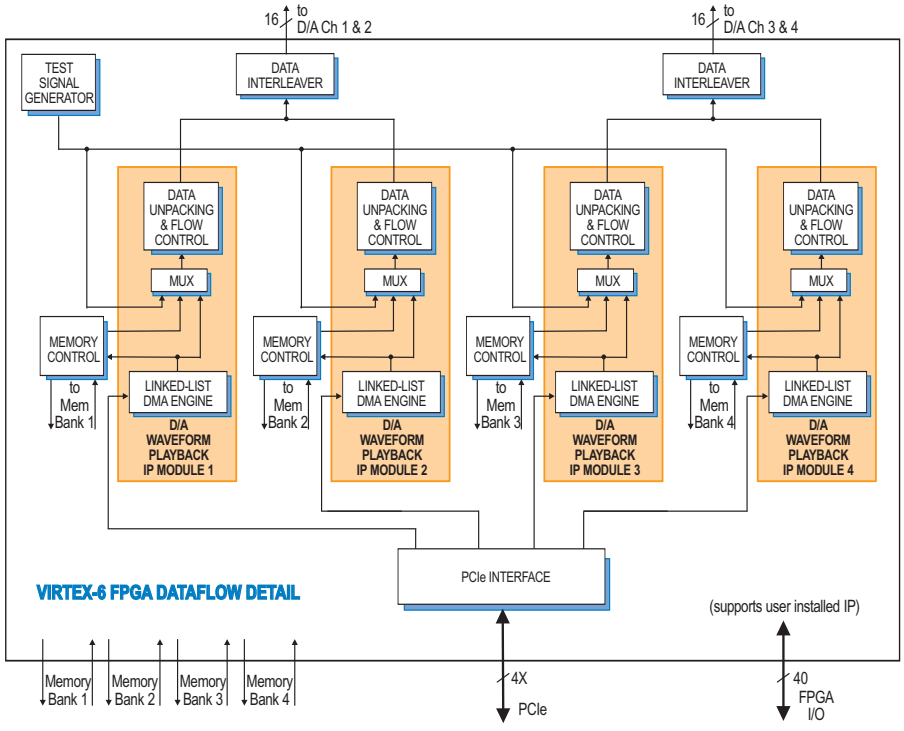
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 74670.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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4- or 8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - cPCI

➤ Specifications

Models 72670 and 73670: 4-Channel DUC, 4-channel D/A

Model 74670: 8-Channel DUC, 4-channel D/A

D/A Converters (4 or8)

Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs (4 or 8)

Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670

Memory Banks (1 or 2)

Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73670: 32 bits only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI
73670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U cPCI
74670	8-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 72671, 73671 and 74671

4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - cPCI

Model 74671 Model 73671

General Information

Models 72671, 73671 and 74671 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71671 XMC modules mounted on a cPCI carrier board.

Model 72671 is a 6U cPCI board while the Model 73671 is a 3U cPCI board; both are equipped with one Model 71671 XMC. Model 74671 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

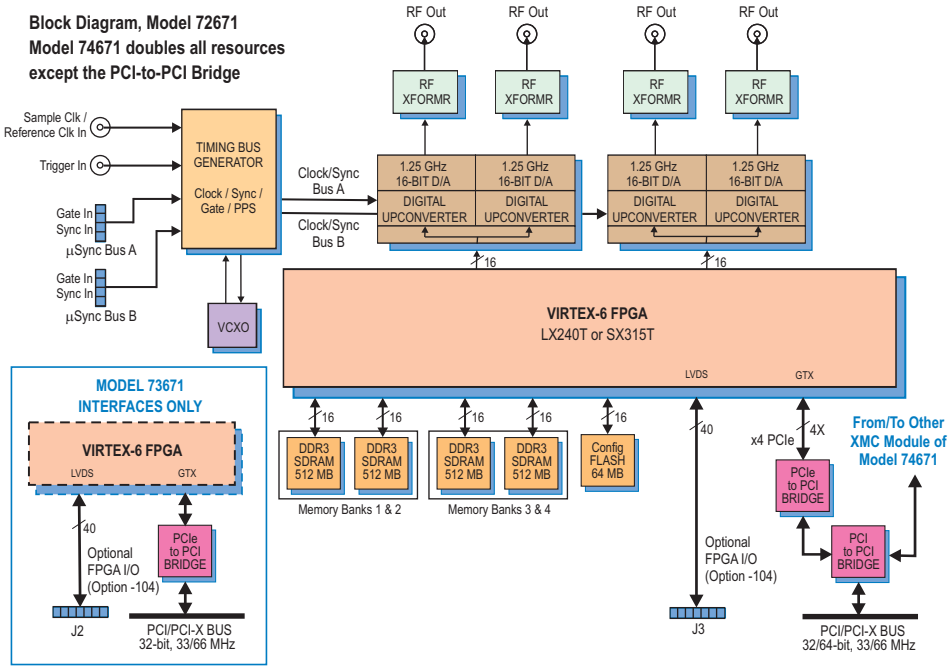
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - cPCI

➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, these models feature an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog outputs are through front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7292, 7392 and 7492 or the 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

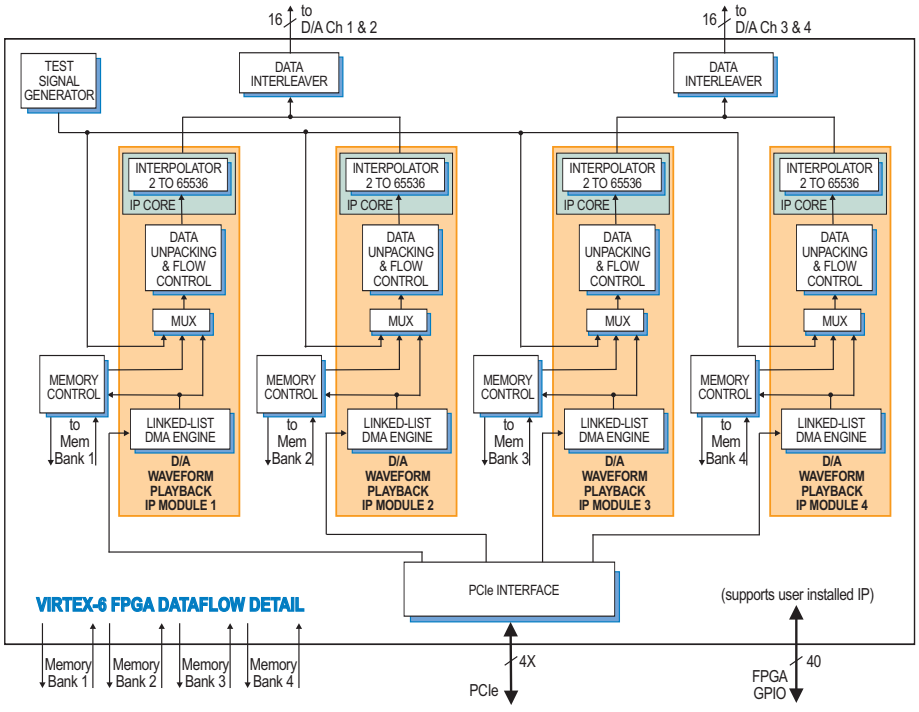
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked-list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 74671.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Models 72671, 73671 and 74671

4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73671: 32 bits only.

Specifications

Models 72671 and 73671: 4-Channel DUC, 4-channel D/A

Model 74671: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or8)

Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (4 or 8)

Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)

Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671

Memory Banks (1 or 2)

Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73671: 32 bits only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U cPCI
73671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U cPCI
74671	8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U cPCI
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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Models 72690, 73690 and 74690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

Model 74690 *Model 73690*

General Information

Models 72690, 73690 and 74690 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a cPCI carrier board.

Model 72690 is a 6U cPCI board while the Model 73690 is a 3U cPCI board; both are equipped with one Model 71690 XMC. Model 74690 is a 6U cPCI board with two XMC modules rather than one.

These models include one ot two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

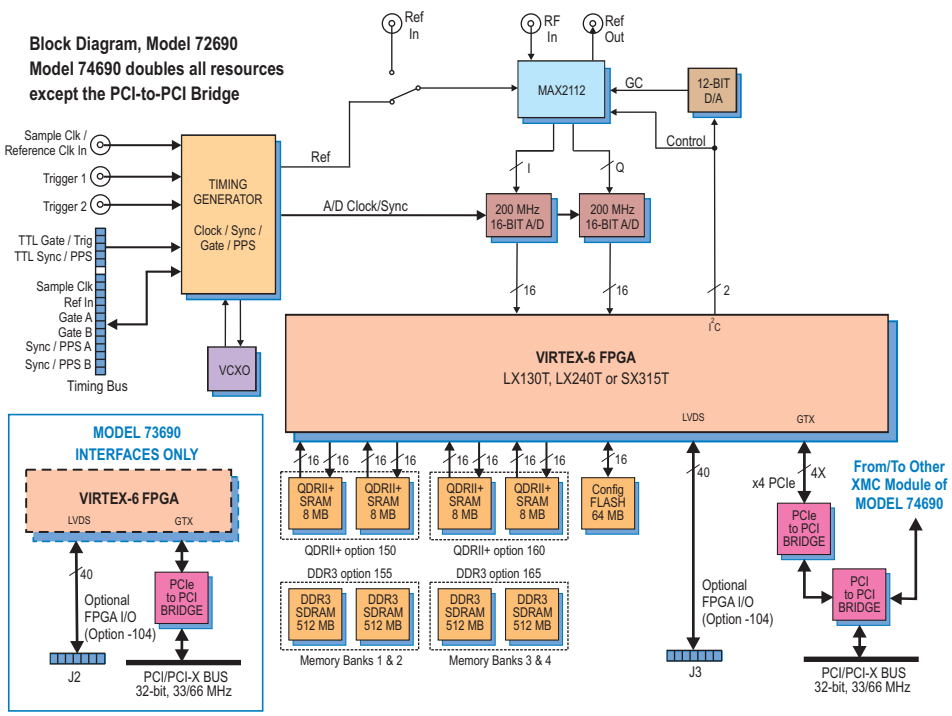
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74690. ➤

Features

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

A/D Acquisition IP Modules

These models feature two or fourA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

➤ RF Tuner Stage

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LNBs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization

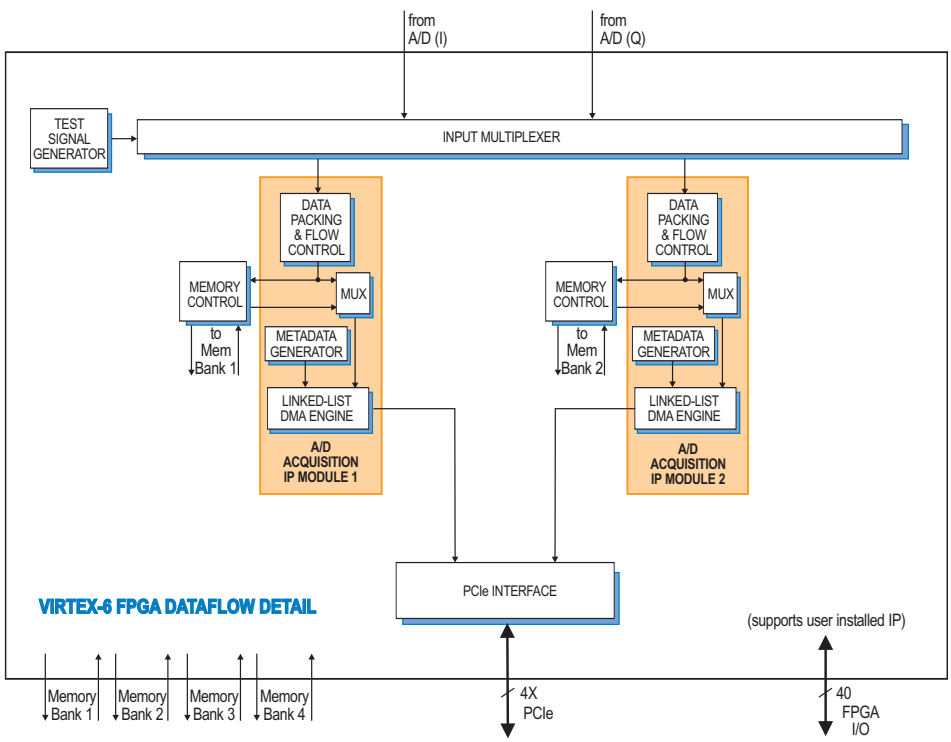
An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the bosrd. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave bosrds, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤



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Models 72690, 73690 and 74690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

PCI-X Interface

The models include an industry-standard interface compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73690: 32 bits only.

Specifications

Model 72690 or Model 73690: 1 RF tuner, 2 A/Ds

Model 74690: 2 RF tuners, four A/Ds

Front Panel Analog Signal Inputs (1 or 2)

Connector: Front panel female SSMC

Impedance: 50 ohms

L-Band Tuners (1 or 2)

Type: Maxim MAX2112

Input Frequency Range: 925 MHz to 2175 MHz

Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz

Fractional-N PLL Synthesizer: $freq_{VCO}$ = (N.F) x $freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value

PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*

Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*

***Usable Full-Scale Input Range:** –50 dBm to +10 dBm

Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters (2 or 4)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources (1 or 2)

On-board timing generator/synthesizer

A/D Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Inputs (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (2 or 4)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or2)

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74950

Memory Banks (1 or 2)

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73690: 32 bits only

Environmental

Operating Temp: 0° to 50° C

Storage Temp: –20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
71690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74690
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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Models 72720 73720 and 74720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

Model 74720 *Model 73720*

General Information

Models 72720, 73720 and 74720 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71720 XMC modules mounted on a cPCI carrier board.

Model 72720 is a 6U cPCI board while the Model 73720 is a 3U cPCI board; both are equipped with one Model 71720 XMC. Model 74720 is a 6U cPCI board with two XMC modules rather than one.

These models include three or sixA/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCI-X interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

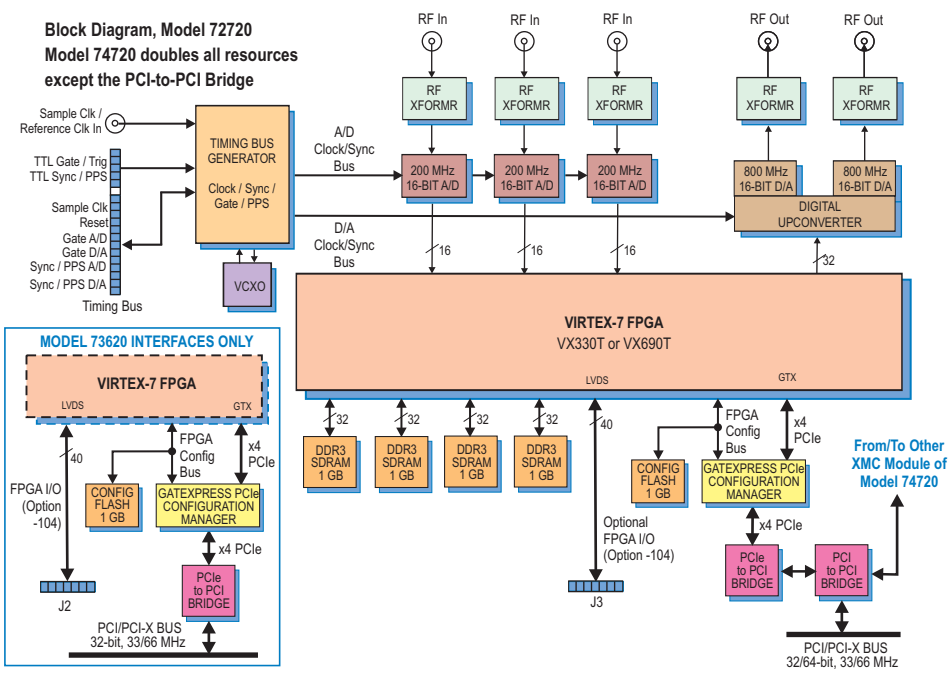
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Models 72720 73720 and 74720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

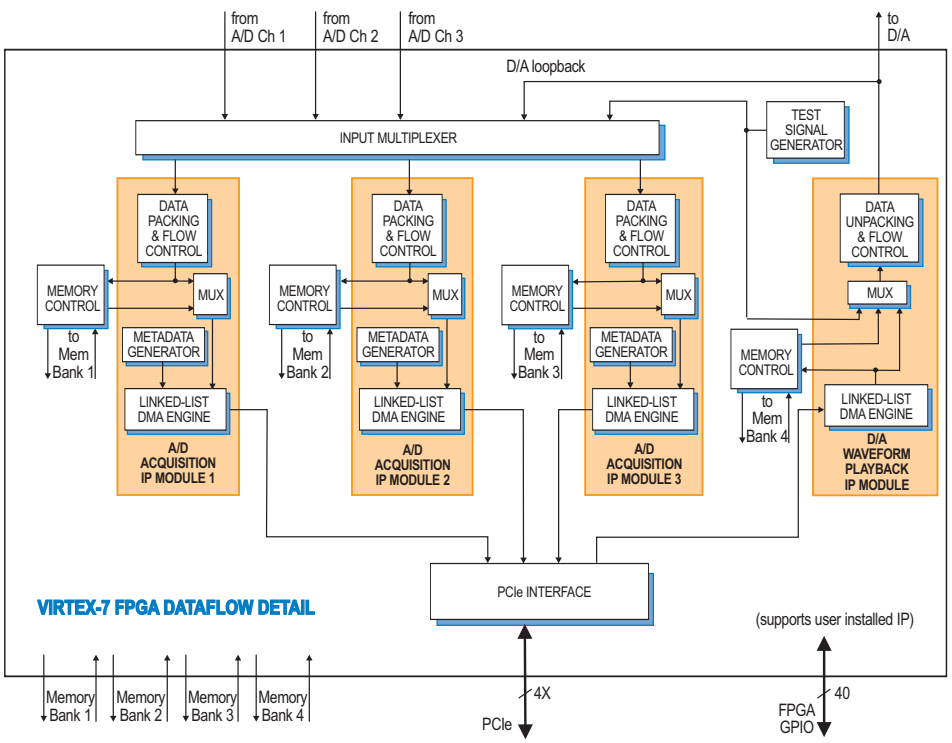
A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 72720 73720 and 74720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73620: 32 bits only.

Ordering Information

Model	Description
72720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex7 FPGA - 6U cPCI
73720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 3U cPCI
74720	6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A and two Virtex-7 FPGAs - 6U cPCI

Options:

-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Specifications

Model 72620 or Model 73620: 3 A/Ds, 1 DUC, 2 D/As
Model 74620: 6 A/Ds, 2 DUCs, 4 D/As
Front Panel Analog Signal Inputs (3 or 6)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits
Front Panel Analog Signal Outputs (2 or 4)
Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720
Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73620: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

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New!

Models 72721 73721 and 74721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

Model 74721 *Model 73721*

General Information

Models 72721, 73721 and 74721 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71721 XMC modules mounted on a cPCI carrier board.

Model 72721 is a 6U cPCI board while the Model 73721 is a 3U cPCI board; both are equipped with one Model 71721 XMC. Model 74721 is a 6U cPCI board with two XMC modules rather than one.

These models include three or sixA/Ds, programmable DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains one or two intrepolation IP cores, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

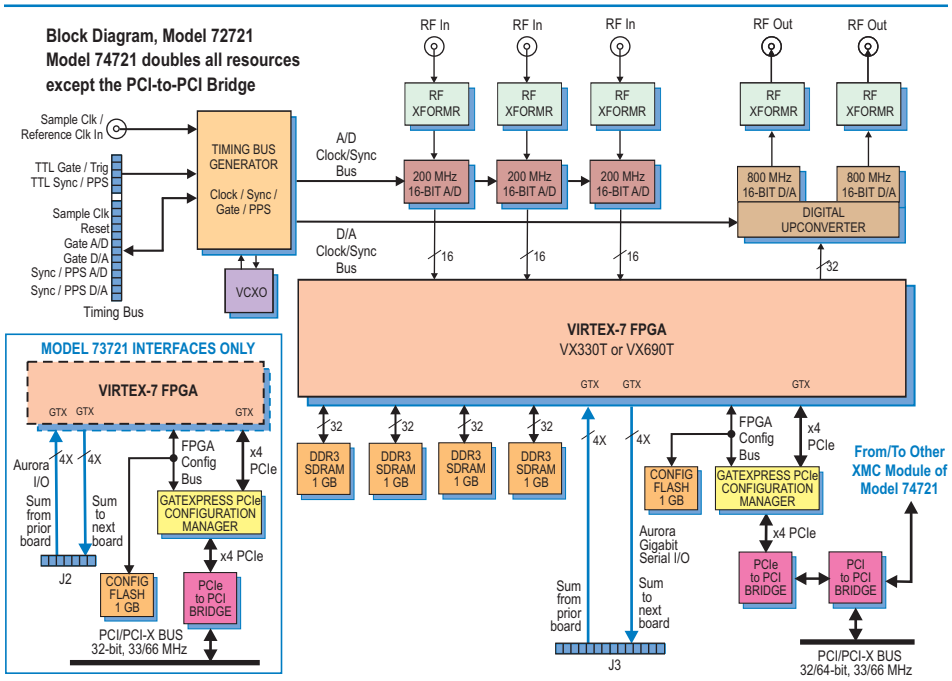
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs
- Two or four 800 MHz 16-bit D/As
- One or two DUCs
- Multiboard programmable beamformer
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 72721 73721 and 74721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

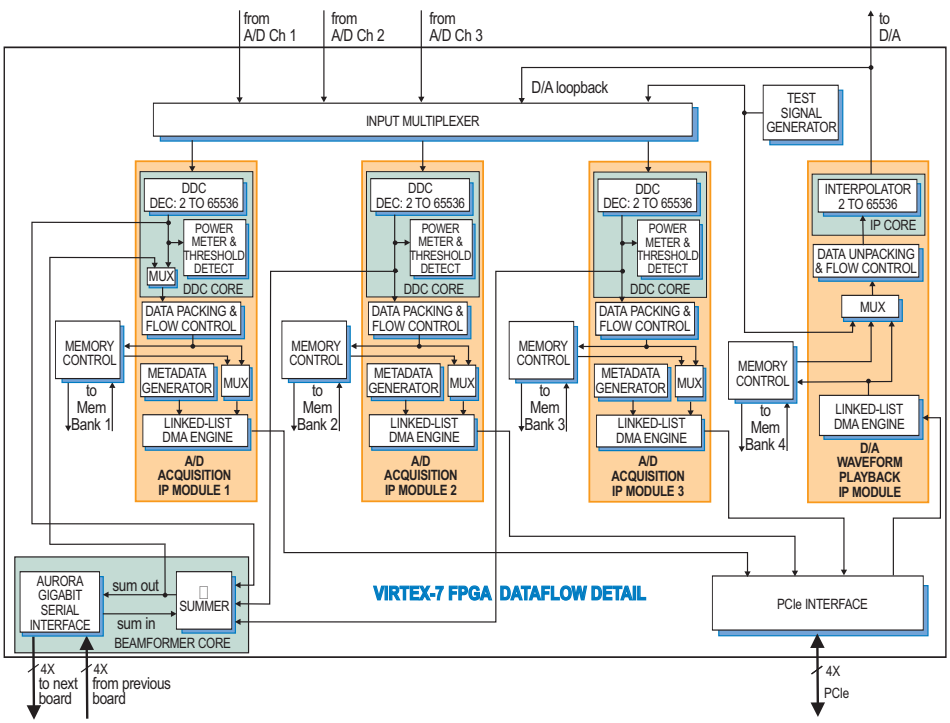
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

Thefactory-installed functions in these models includeone or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUC (digital upconverters) and D/As accept baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73721: 32 bits only. ➤

Models 72721 73721 and 74721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

➤ Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72721 or Model 73721: 3 A/Ds, 1 DUC, 2 D/As

Model 74721: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (3 or 6)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Memory Banks (1 or 2)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73721: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U cPCI
73721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U cPCI
74721	6-Channel 200 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs - 6U cPCI
Option:	
-076	XC7VX690T-2 FPGA

Models 72730, 73730 and 74730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - cPCI

Model 74730 *Model 73730*

General Information

Models 72730, 73730 and 74730 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a cPCI carrier board.

Model 72730 is a 6U cPCI board while the Model 73730 is a 3U cPCI board; both are equipped with one Model 71730 XMC. Model 74730 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include ne or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

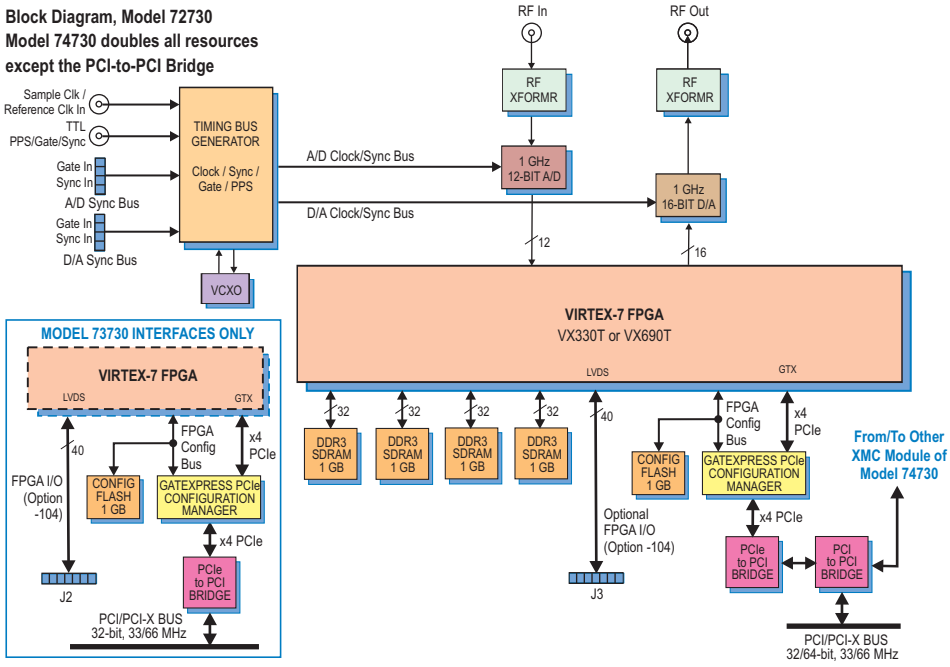
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Block Diagram, Model 72730
Model 74730 doubles all resources except the PCI-to-PCI Bridge



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Models 72730, 73730 and 74730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - cPCI

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

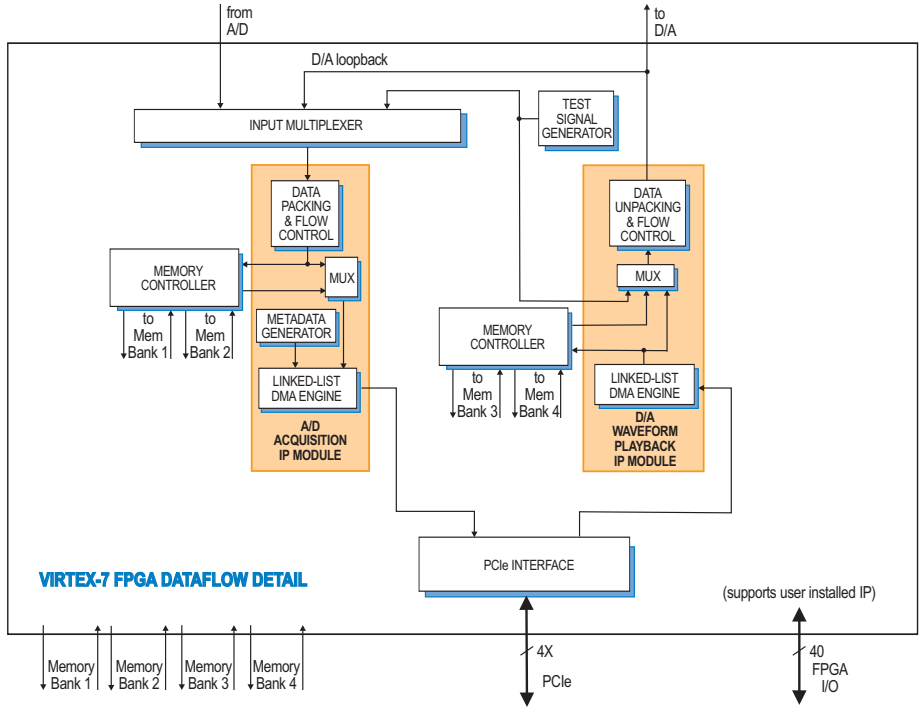
A/D Converter Stage

The front end accepts one or two analog HF or IF input on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to acept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors. ➤



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Models 72730, 73730 and 74730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - cPCI

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73730: 32 bits only.

Ordering Information

Model	Description
72730	1 GHz A/D and D/A, Virtex-7 FPGA - 6U cPCI
73730	1 GHz A/D and D/A, Virtex-7 FPGA - 3U cPCI
74730	Two 1 GHz A/D and D/A, Virtex-7 FPGA - 6U cPCI
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72730 or Model 73730: 1 A/D, 1 D/A
Model 74730: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converters (1 or 2)
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (1 or 2)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730

Memory Banks (1 or 2)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73730: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

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New!

Models 72741, 73741 and 74741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - cPCI

Model 74741 *Model 73741*

General Information

Models 72741, 73741 and 74741 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a cPCI carrier board.

Model 72741 is a 6U cPCI board while the Model 73741 is a 3U cPCI board; both are equipped with one Model 71741 XMC. Model 74741 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs.

In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

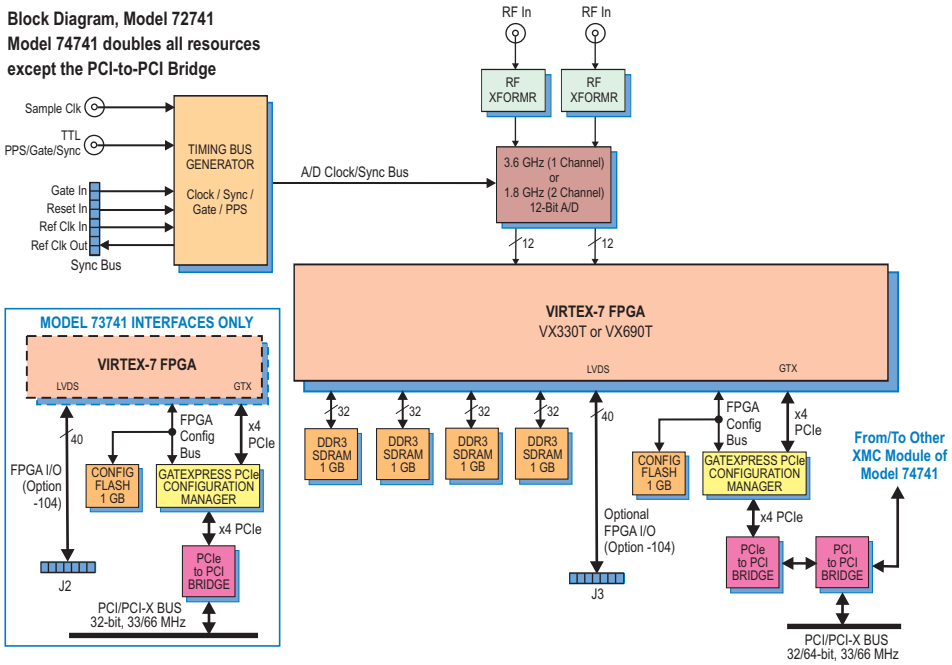
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Block Diagram, Model 72741
Model 74741 doubles all resources except the PCI-to-PCI Bridge



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Models 72741, 73741 and 74741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - cPCI

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/D, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

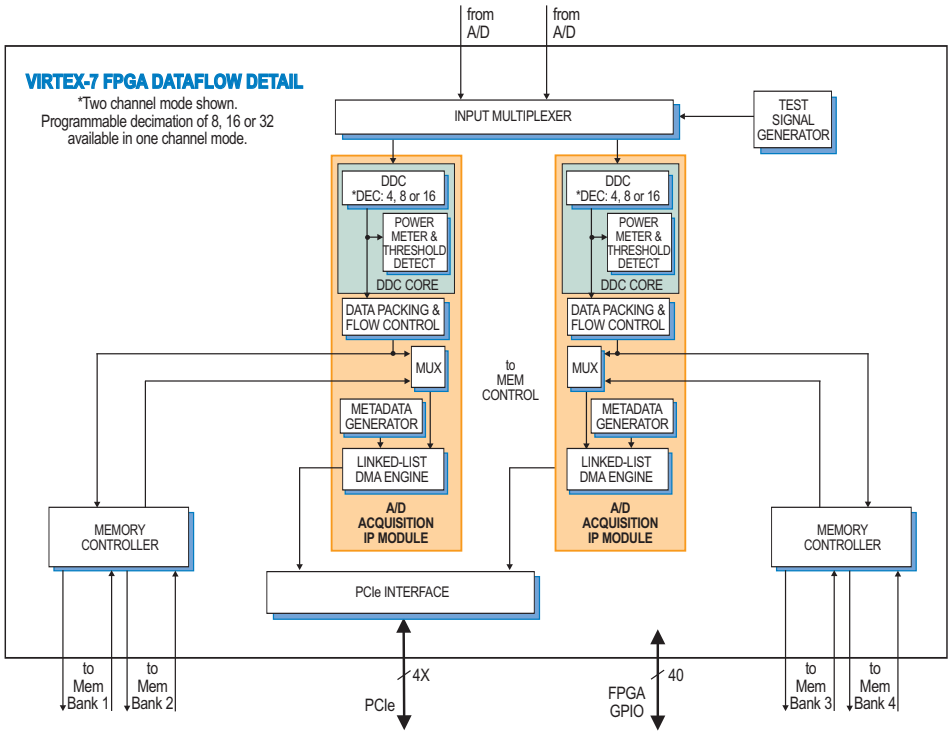
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored ➤



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Models 72741, 73741 and 74741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - cPCI

Memory Resources

The Onyx architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73741: 32 bits only.

Ordering Information

Model	Description
72741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U cPCI
73741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 3U cPCI
74741	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGAs - 6U cPCI

Options:

-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741

➤ on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two boards can be synchronized with a simple cable. For larger systems, multiple boards can be synchronized using the Models 7292, 7392 or 7492 high-speed sync boards to drive the sync bus.

Specifications

Model 72741 or Model 73741: One A/D
Model 74741: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741

Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73741: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

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New!

Models 72751, 73751 and 74751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - cPCI

Model 74751 *Model 73751*

Onyx
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds

General Information

Models 72650, 73650 and 74650 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a cPCI carrier board.

Model 72751 is a 6U cPCI board while the Model 73751 is a 3U cPCI board; both are equipped with one Model 71751 XMC. Model 74751 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

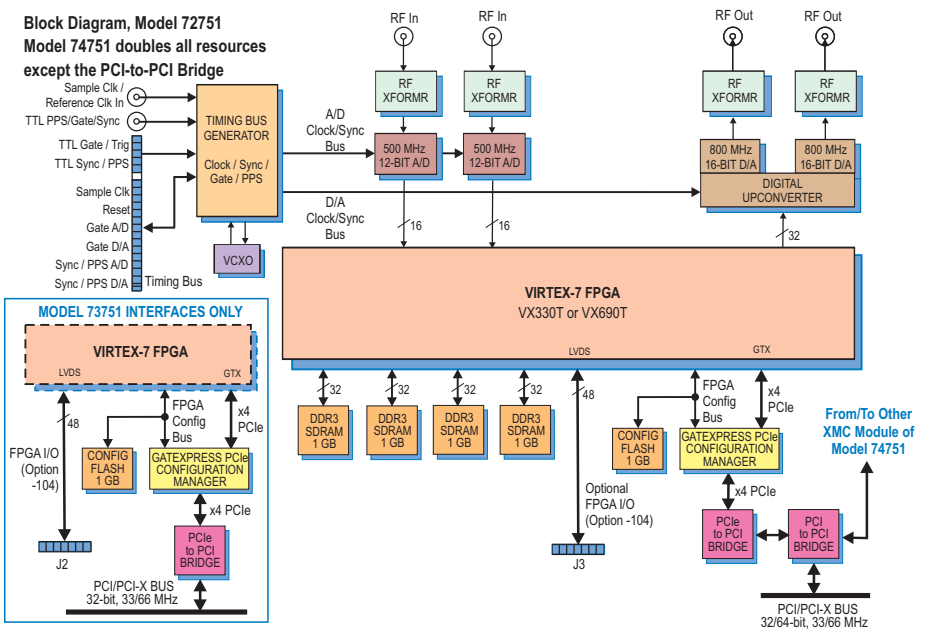
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751. ➤



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Models 72751, 73751 and 74751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - cPCI

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

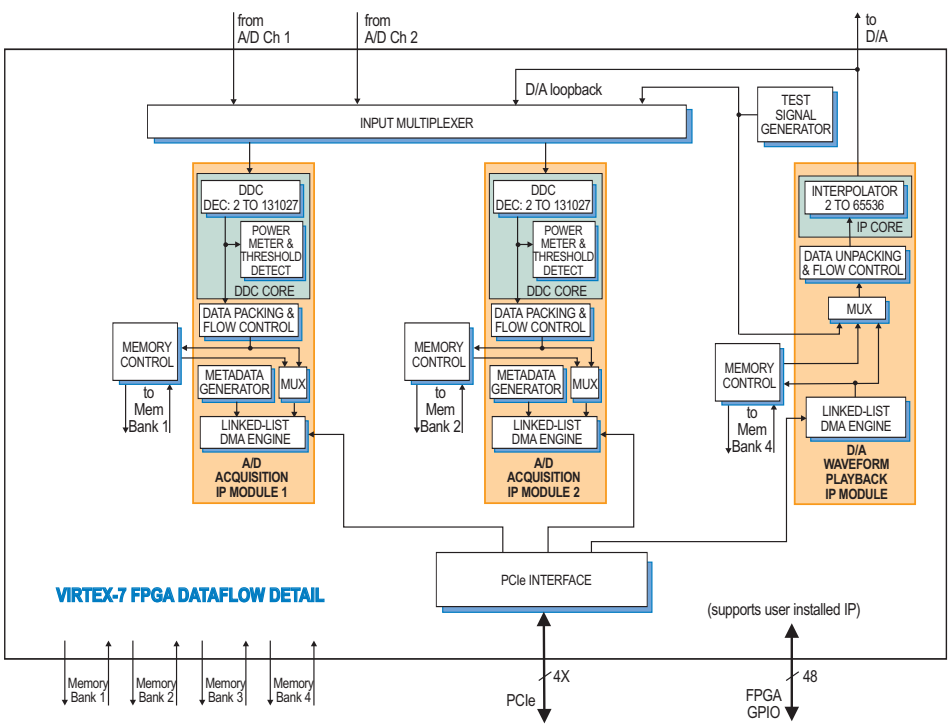
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, Texas Instruments ADS5474 400 MHz, 14-bit A/Ds may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept the baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog outputs are through front-panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73751: 32 bits only. ➤

Models 72751, 73751 and 74751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - cPCI

➤ Specifications

Model 72751 or Model 73751: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

Model 74751: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014) (2 or4)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters (2 or 4)
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2) 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 LVDS pairs between the FPGA and the J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751

Memory (1 or 2)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73751: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U cPCI
73751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U cPCI
74751	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs - 6U cPCI
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751

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Models 72760, 73760 and 74760

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - cPCI

Model 74760 *Model 73760*

General Information

Models 72760, 73760 and 74760 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a cPCI carrier board.

Model 72760 is a 6U cPCI board while the Model 73760 is a 3U cPCI board; both are equipped with one Model 71760 XMC. Model 74760 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

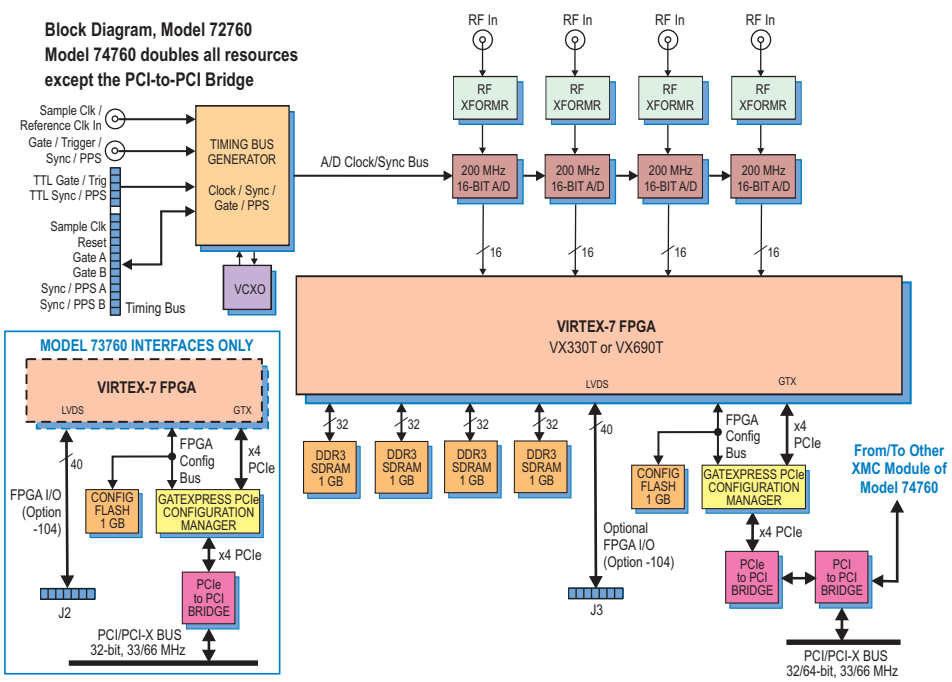
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

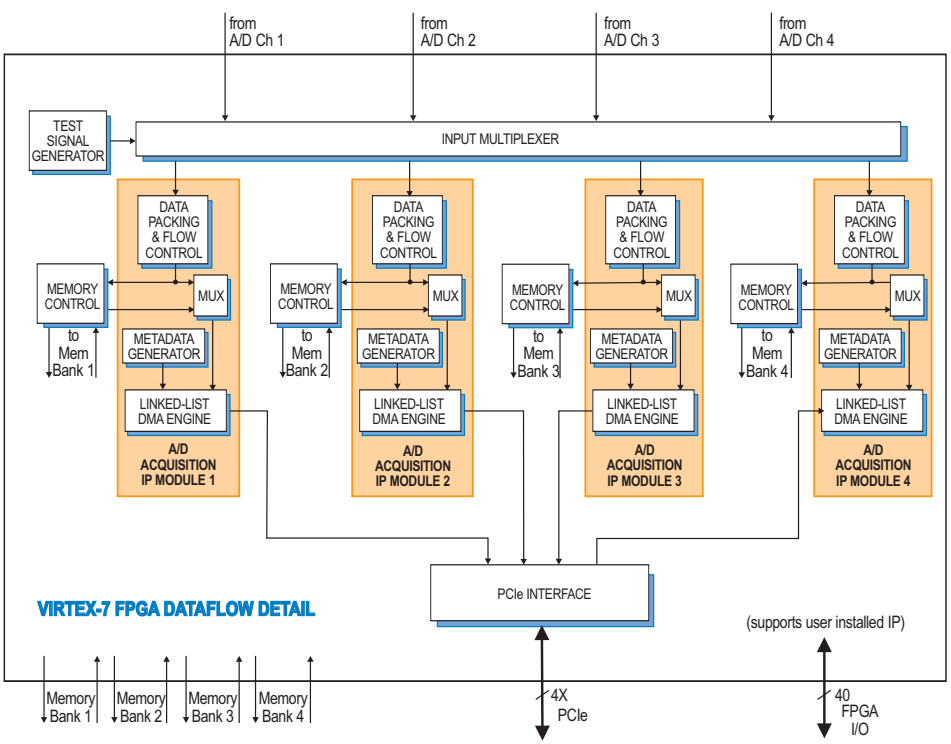
The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources. ➤

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - cPCI

Ordering Information

Model	Description
72760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U cPCI
73760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U cPCI
74760	8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U cPCI
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760

➤ Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73760: 32 bits only.

Specifications

Model 72760 or Model 73760: 4 A/Ds
Model 74760: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources: (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2)
26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760
Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73760: 32 bits only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

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New!

Models 72761 73761 and 74761

4- or 8-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - cPCI

Model 74761 Model 73761

General Information

Models 72761, 73761 and 74761 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71761 XMC modules mounted on a cPCI carrier board.

Model 72761 is a 6U cPCI board while the Model 73761 is a 3U cPCI board; both are equipped with one Model 71761 XMC. Model 74761 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, programmable DDCs and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

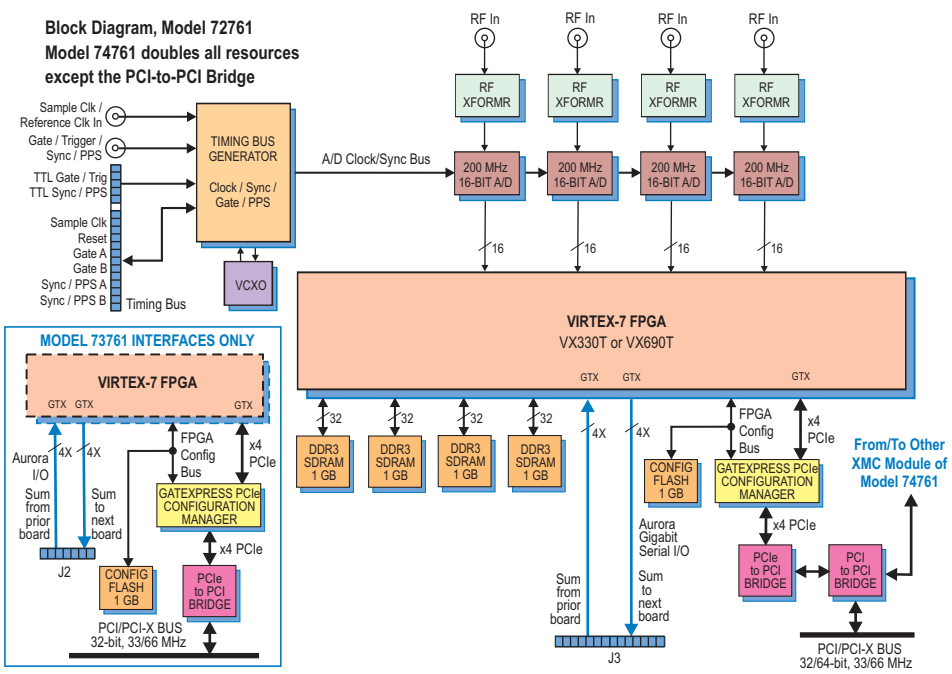
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- Multiboard programmable beamformer
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization



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4- or 8-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, these models feature a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

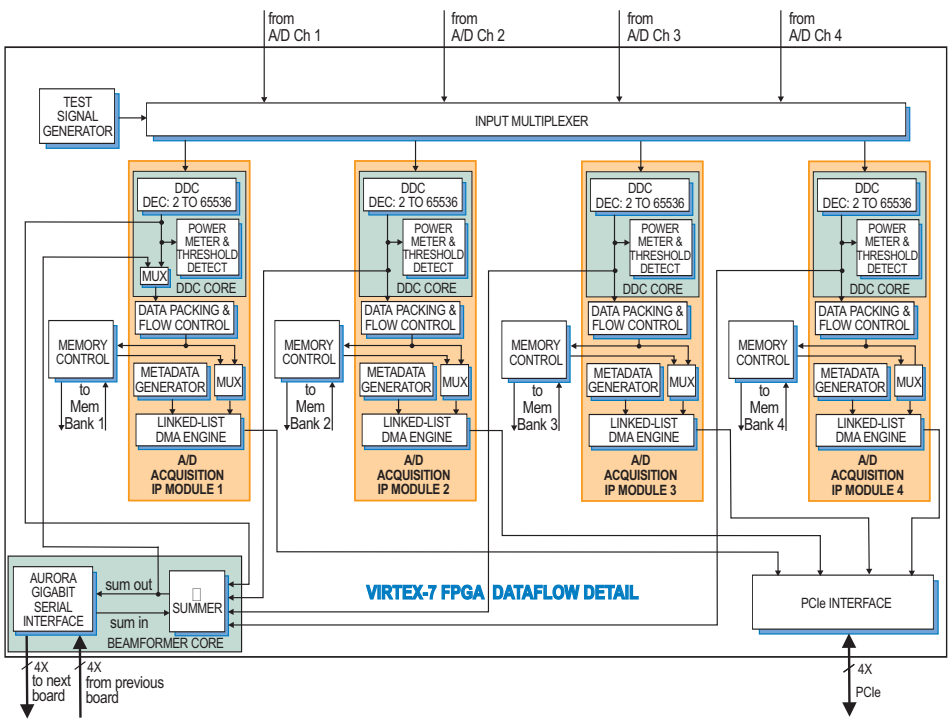
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73761: 32 bits only. ➤

4- or 8-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - cPCI

➤ Specifications

Model 72761 or Model 73761: 4 A/Ds,
Model 74761: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources (1 or 2)
- On-board clock synthesizer

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2) 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Memory Banks (1 or 2)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
  Model 73761: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72761	4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 6U cPCI
73761	4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U cPCI
74771	8-Channel 200 MHz A/D with DDCs, Virtex-7 FPGAs - 6U cPCI
Option:	
-076	XC7VX690T-2 FPGA

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New!

Models 72791, 73791 and 74791

1 or 2 L-Band RF Tuners, 2- or 4-Channel 500 MHz A/Ds, Virtex-7 FPGAs - cPCI

Model 74791 *Model 73791*

General Information

Models 72791, 73791 and 74791 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71791 XMC modules mounted on a cPCI carrier board.

Model 72791 is a 6U cPCI board while the Model 73791 is a 3U cPCI board; both are equipped with one Model 71791 XMC. Model 74791 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds, two or four DDCs and four or eight banks of memory, one or two general purpose connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features one or two Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The factory-installed functions include two or four A/D acquisition IP modules, four or eight DDR3 memory controllers, two or four DDCs, RF tuner controllers, clock and synchronization generators, and one or two test signal generators.

Thus, these models can operate as complete turnkey solutions with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory- installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

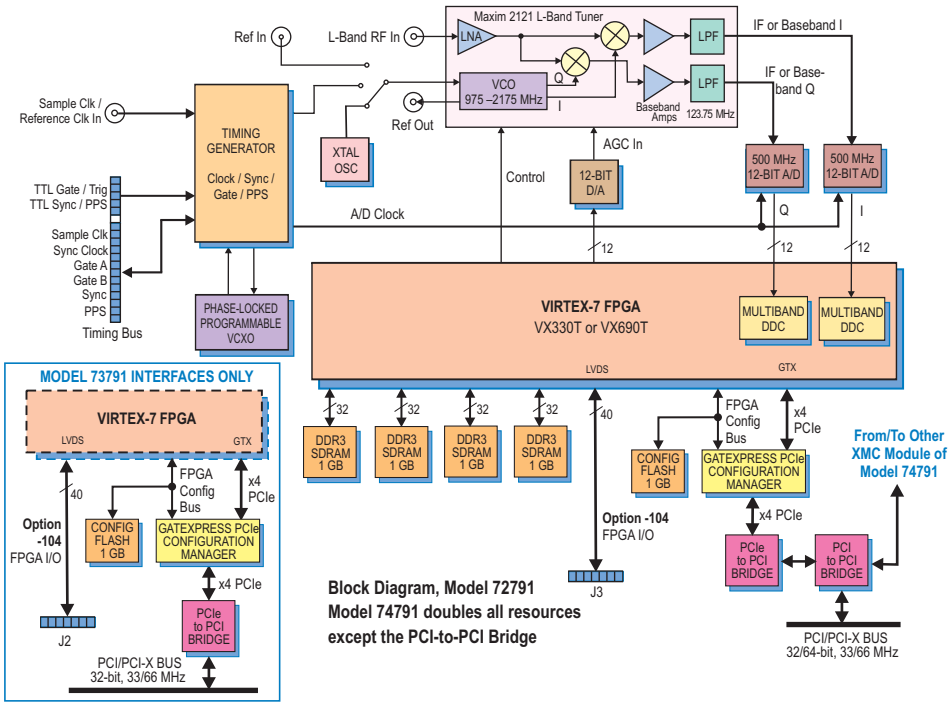
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs handle L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog down-converters provide IF or I+Q baseband signals at frequencies up to 123 MHz
- Two or four 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two or four FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



Block Diagram, Model 72791
Model 74791 doubles all resources except the PCI-to-PCI Bridge

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Models 72791, 73791 and 74791

1 or 2 L-Band RF Tuners, 2- or 4-Channel 500 MHz A/Ds, Virtex-7 FPGAs - cPCI

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

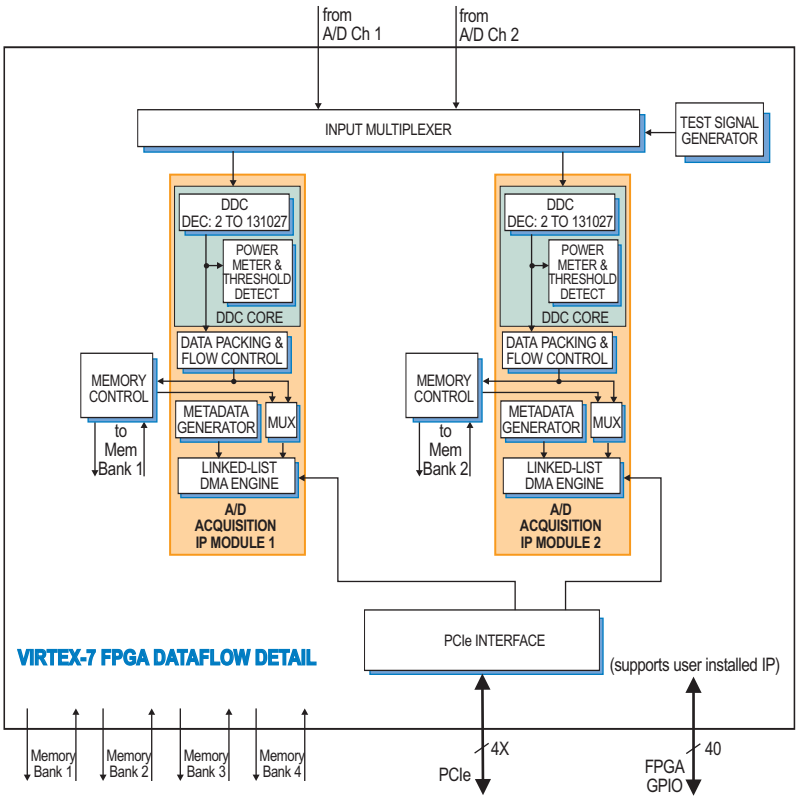
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The analog tuner outputs are digitized by two or four Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two or four independent A/D and DDC channels are now available for digitizing and downconverting signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

One or two internal timing generators provide all timing, gating, triggering and synchronization functions required by the A/D converters. They also serve as optional sources for the L-Band tuner references.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent 1 GB DDR3 SDRAMs for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be used to support custom user-installed IP within the FPGA .

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73791: 32 bits only. ➤

Models 72791, 73791 and 74791

1 or 2 L-Band RF Tuners, 2- or 4-Channel 500 MHz A/Ds, Virtex-7 FPGAs - cPCI

➤ Specifications

Model 72791 or Model 73791: 1 L-band Tuner, 2 A/Ds, 2 DDCs, 1 FPGA
Model 74751: 2 L-Band Tuners, 4 A/Ds, 4 DDCs, 2 FPGAs

Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuner (1 or 2)
Type: Maxim MAX2121
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 10 MHz to 500 MHz
Resolution: 12 bits
Option -014: 400 MHz, 14-bit A/Ds

Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer

A/D Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus (1 or 2)
26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (2 or 4)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791

Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73791: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 6U cPCI
73791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U cPCI
74791	2 L-Band RF Tuners with 4-Channel 500 MHz A/D with DDCs and two Virtex-7 FPGAs - 6U cPCI
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS I/O between the FPGA and J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791

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New!

Models 72131 73131 & 74131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - cPCI

Model 74131 *Model 73131*

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports one or two Xilinx Kintex UltraScale FPGAs
- Eight or 16 200 MHz 16-bit A/Ds
- Eight or 16 multiband DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized versions available

General Information

Models 72131, 73131 and 74131 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71131 XMC modules mounted on a cPCI carrier board. Model 72131 is a 6U board while Model 73131 is a 3U board; both have one Model 71131 module. Model 74131 is equipped with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections and the option for a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

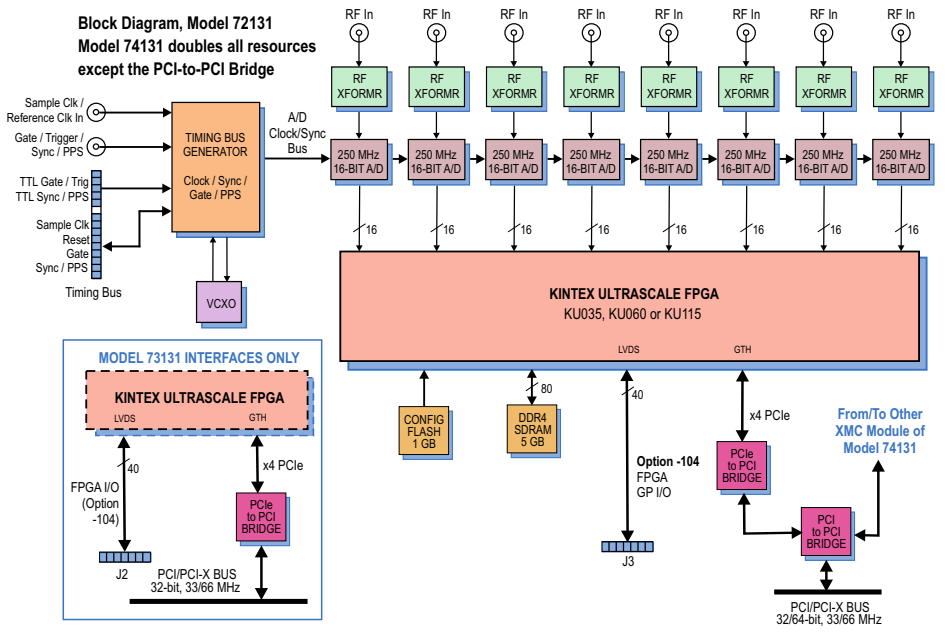
Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, ➤



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Models 72131 73131 & 74131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or a test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eightA/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73131; J3 connector, Model 72131; J3 and J5 connectors, Model 74131.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

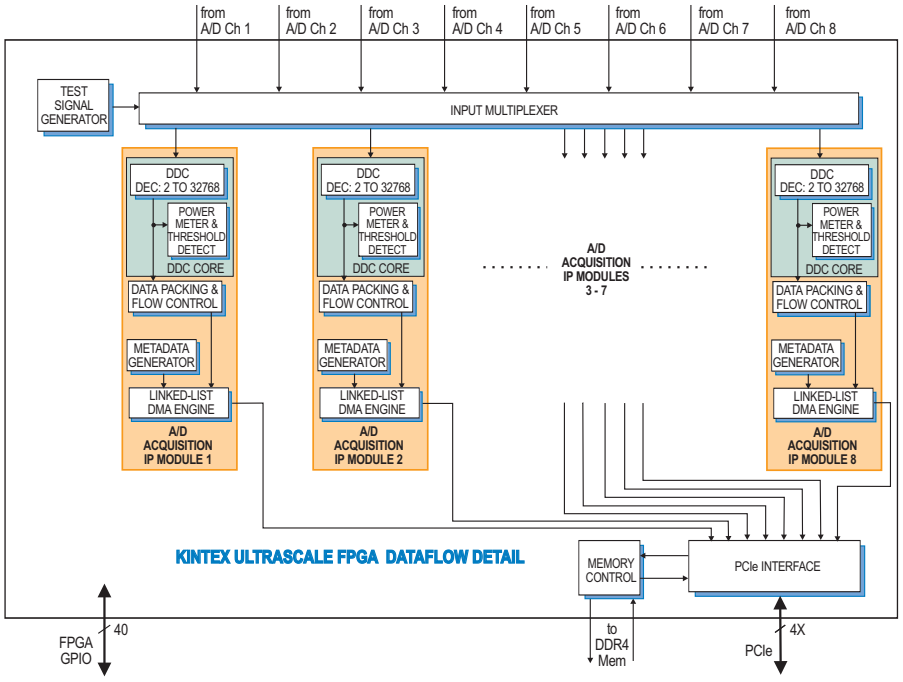
Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73131: 32 bits only. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 72131 73131 & 74131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - cPCI

➤ Specifications

Models 72131 and 73131: 8 A/Ds
Model 74131: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8 or 16)
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters (8 or 16)
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** LVDS I/O between the FPGA and J2 connector, Model 73131; J3 connector, Model 72131; J3 and J5 connectors, Model 74131

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB Models 72131 and 73131; 10 GB Model 74131
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73131: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI
73131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI
74131	16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U cPCI
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

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New!

Models 72132 73132 & 74132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

Model 74132 *Model 73132*

JADE

NAVIGATOR Design Suite

General Information

Models 72132, 73132 and 74132 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71132 XMC modules mounted on a cPCI carrier board. Model 72132 is a 6U board while Model 73132 is a 3U board; both have one Model 71132 module. Model 74132 is equipped with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

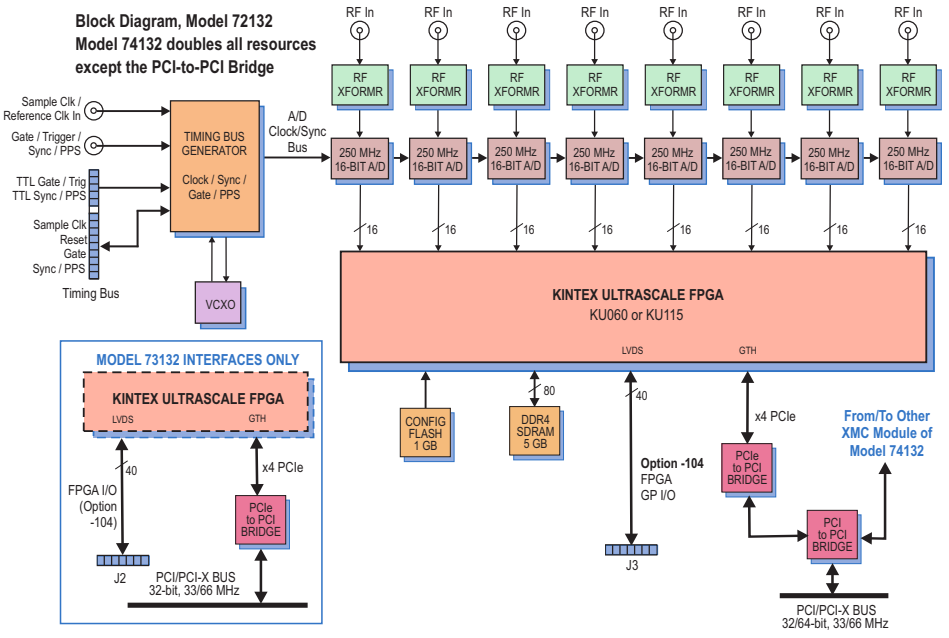
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤

Features

- Ideal radar and software radio interface solution
- Supports one or two Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 wideband DDCs (digital downconverters)
- 64 or 128 multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available



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Models 72132 73132 & 74132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or one or two test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downnonversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132.

A/D Converter Stage

The front end accepts eight or 16 analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four or eight TI ADS42LB69 dual 250 MHz, 16-bit A/D s.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

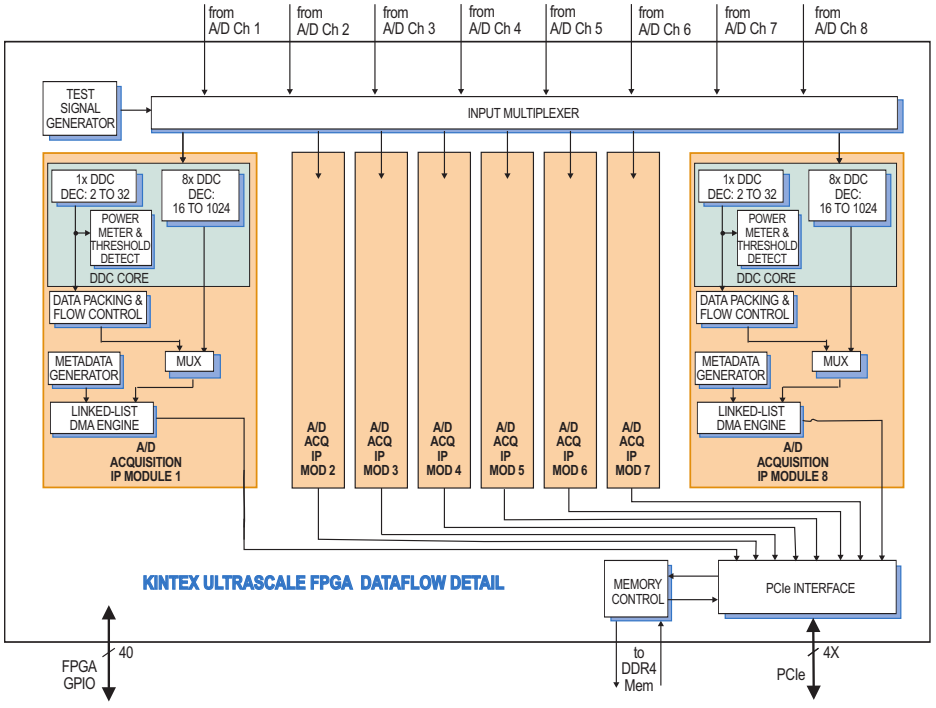
Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73132: 32 bits only. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 72132 73132 & 74132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

➤ Specifications

Models 72132 and 73132: 8 A/Ds
Model 74132: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8 or 16)
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters (8 or 16)
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (64 or 128)
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s,idependent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** LVDS I/O between the FPGA and J2 connector, Model 73132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB Models 72132 and 73132; 10 GB Model 74132
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz; Model 73132: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: **6U board**: 6.299 in x 9.173 in (160.00 mm x 233.00 mm)
3U board 3.937 in x 6.299 in (100.00 mm x 160.00 mm)

Ordering Information

Model	Description
72132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI
73132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI
74132	16-Channel 250 MHz A/D with DDCs and two Kintex UltraScale FPGAs - 6U cPCI

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

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New!

Models 72141, 73141 and 74141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

Model 74141 *Model 73141*

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex Ultra-Scale FPGAs
- One or two-channel mode with one or two 6.4 GHz, 12-bit A/Ds
- Two or four-channel mode with two or four 3.2 GHz, 12-bit A/Ds
- Two or four-channel mode with two or four 6.4 GHz, 14-bit D/As
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization\
- Optional LVDS connections to the FPGA for custom I/O

General Information

Models 72141, 73141and 74141 are members of the Jade™ family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a cPCI carrier board. Model 72141 is a 6U cPCI board while the Model 73141 is a 3U cPCI board; both are equipped with one Model 71141 XMC. Model 74141 is a 6U cPCI board with two XMC modules rather than one.

They includet two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. These models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include two or four A/D acquisition IP modules.

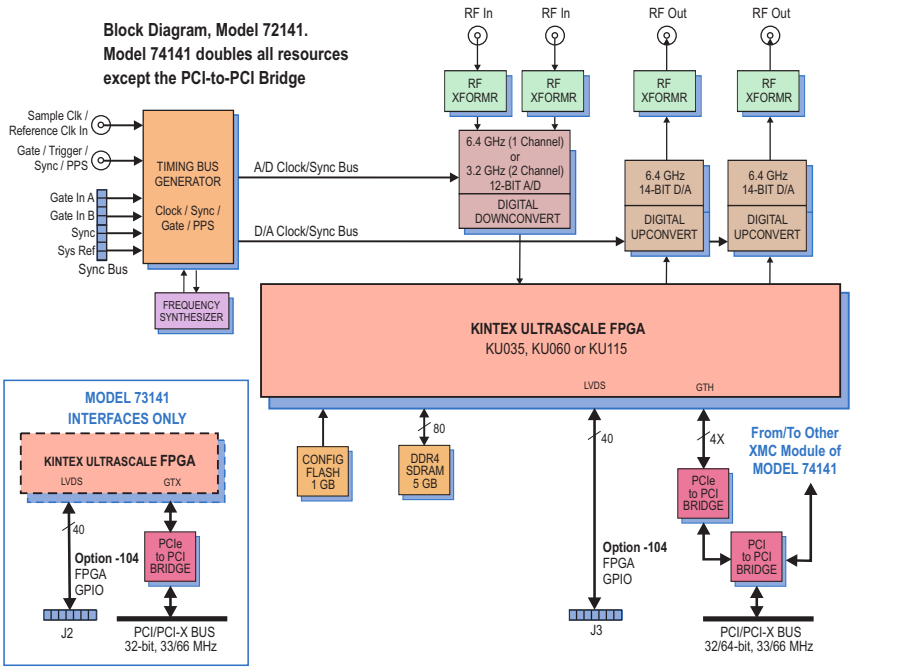
Each of the acquisition IP modules contains a programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. ➤



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Models 72141, 73141 and 74141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either on-board memory or off-board host memory.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 (or J2 connector, Model 73141) for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADC12D1800 12-bit A/Ds. The converters operate in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

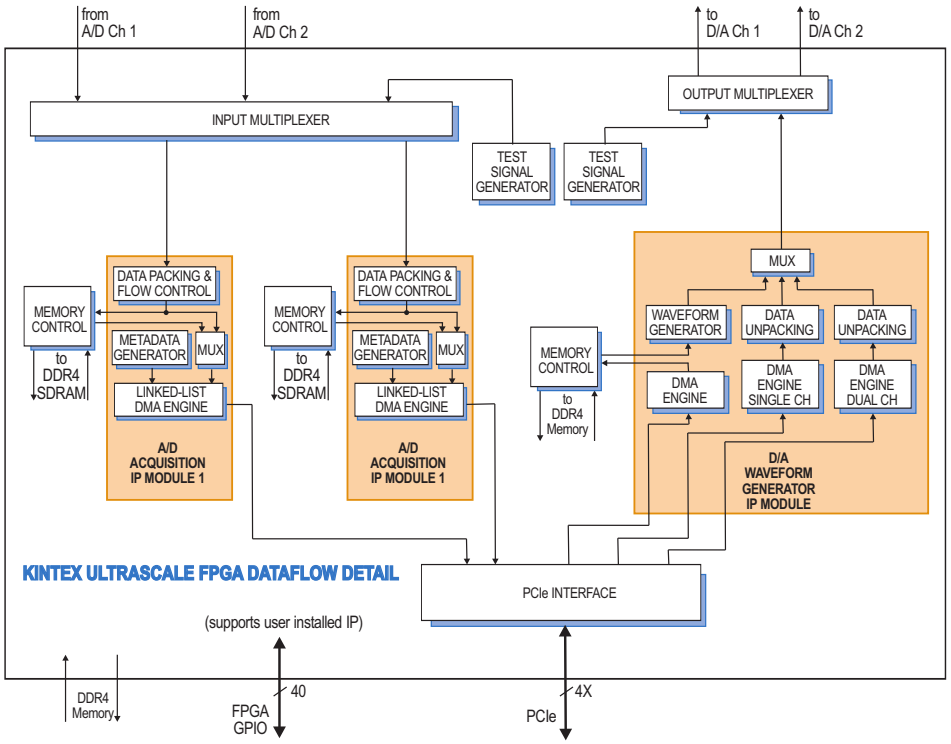
A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7292 high-speed sync boards to drive the sync bus.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core(s) within the FPGA(s) can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73141: 32 bits only. ➤



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Models 72141, 73141 and 74141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

Specifications

Model 72141 or Model 73141: Two A/Ds
Model 74141: Four A/Ds
Model 72141 or Model 73141: Two D/As
Model 74141: Four D/As
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter (2 or 4)
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters (2 or 4)
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes ync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74141
Memory (1 or 2)
Type: DDR4 SDRAM
Size: GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73141: 32 bits only
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)
3U board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

Ordering Information

Model	Description
72141	1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI
73141	1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI
74141	2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and two Kintex UltraScale FPGAs - 6U cPCI
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74841
-702	Air cooled, Level L2

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Models 72821 73821 and 74821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

Model 74821 *Model 73821*

JADE NAVIGATOR Design Suite

General Information

Models 72821, 73821 and 74821 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71821 XMC modules mounted on a cPCI carrier board. Model 72821 is a 6U cPCI board while the Model 73821 is a 3U cPCI board; both are equipped with one Model 71821 XMC. Model 74821 is a 6U cPCI board with two XMC modules rather than one.

They include three or six A/Ds, complete multiboard clock and sync sections, large DDR4 memory, three or six DDCs, one or two DUCs and two or four D/As. In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The factory-installed functions for these models include three or six A/D acquisition and one or two waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

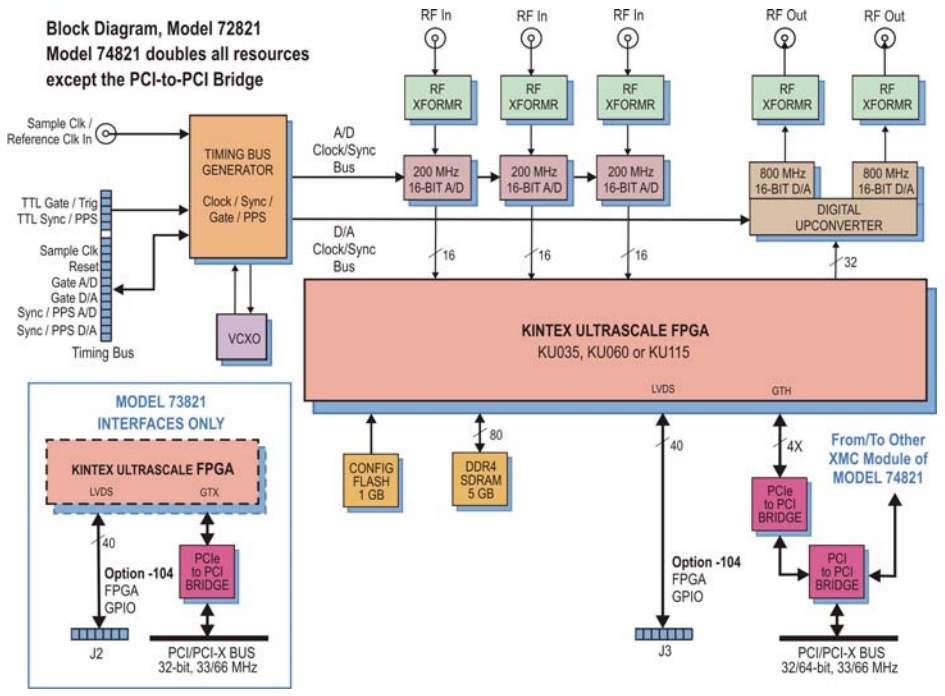
Additional IP includes: three or six powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; programmable interpolators, and a PCI-Xinterface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available



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Models 72821 73821 and 74821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from three A/Ds, or the test signal generators.

Each acquisition module has a DMA engine for easily moving A/D data through the PCI-X interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition rate etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

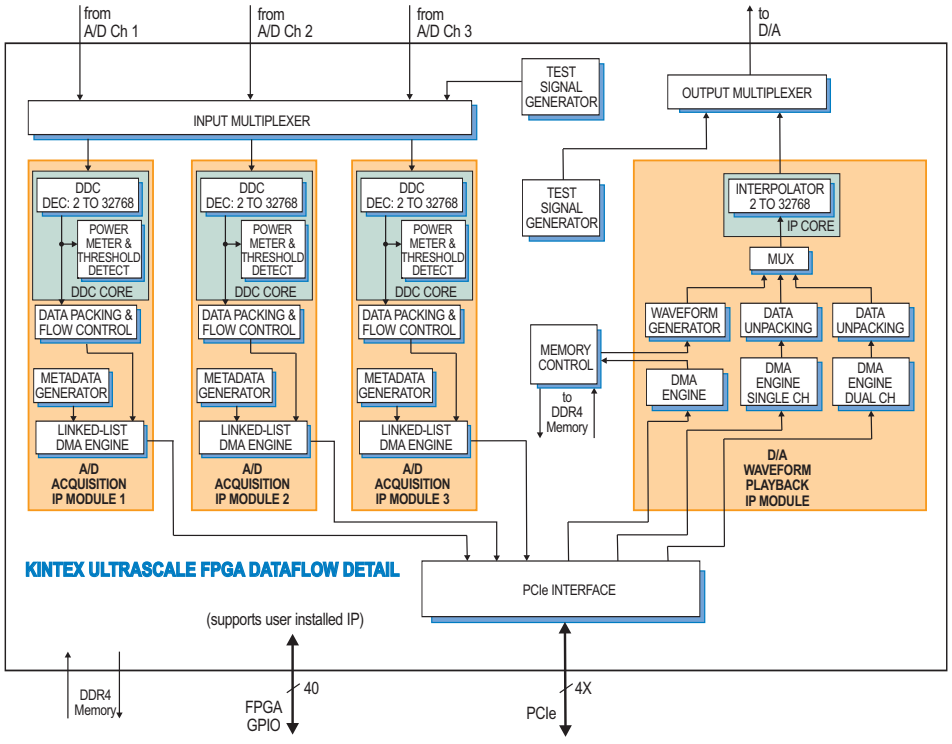
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73821; J3 connector, Model 72821; J3 and J5 connectors, Model 74821.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources. ➤



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➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73821: 32 bits only. ➤

Models 72821 73821 and 74821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

Ordering Information

Model	Description
72821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX
73821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX
74821	6-Channel 200 MHz A/D with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGAs - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged version

➤ Specifications

Model 72821 or Model 73821: 3 A/Ds, 1 DUC, 2 D/As

Model 74721: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (3 or 6)
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (1 or 2)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core (1 or 2)
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73821; J3 connector, Model 72821; J3 and J5 connectors, Model 74821

Memory (1 or 2)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73821: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 6U board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)
3U board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

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New!

Models 72841, 73841 and 74841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

Model 74841 *Model 73841*

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex Ultra-Scale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization\
- Optional LVDS connections to the FPGA for custom I/O

General Information

Models 72841, 73841and 74841 are members of the Jade™ family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a cPCI carrier board. Model 72841 is a 6U cPCI board while the Model 73841 is a 3U cPCI board; both are equipped with one Model 71841 XMC. Model 74841 is a 6U cPCI board with two XMC modules rather than one.

They include one or two A/Ds, programmable DDCs, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

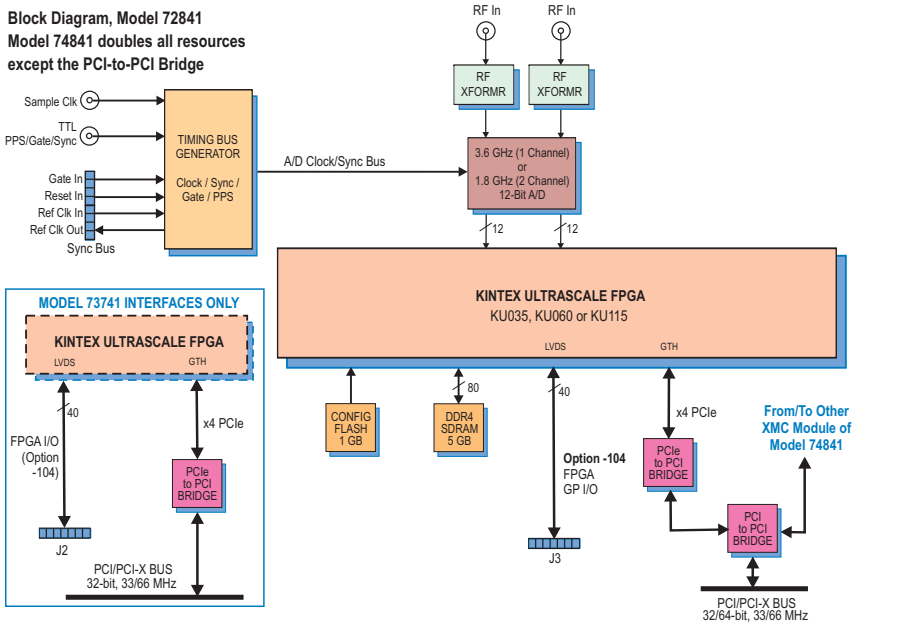
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. ➤



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Models 72841, 73841 and 74841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 (or J2 connector, Model 73841) for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

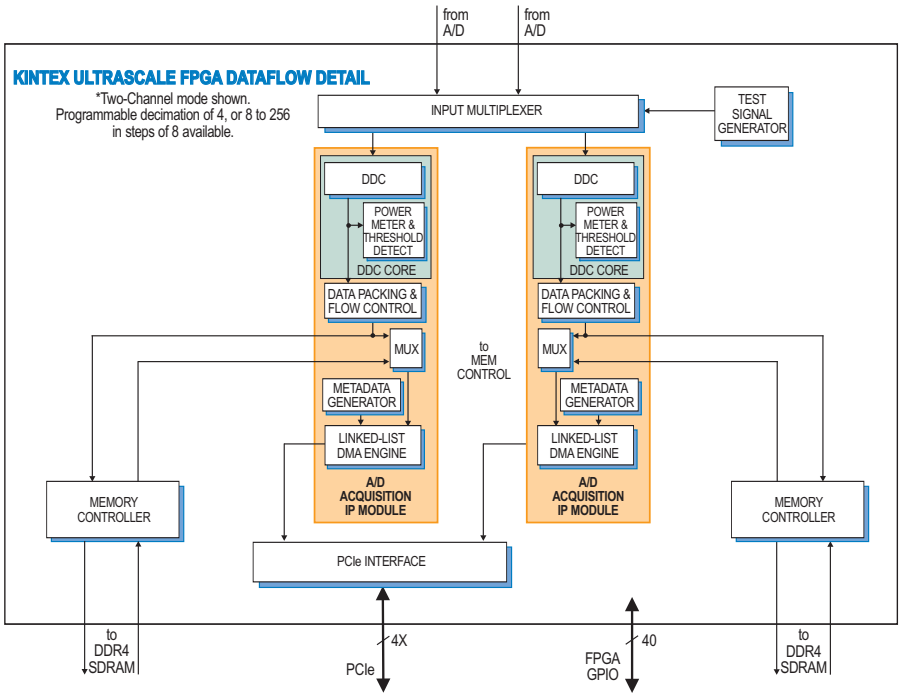
The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high- speed sync boards to drive the sync bus. ➤



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1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

Ordering Information

Model	Description
72841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI
73841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 3U cPCI
74841	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841
-702	Air cooled, Level L2

➤ Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73841: 32 bits only.

Specifications

Model 72841 or Model 73841: One A/D
Model 74841: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841

Memory Banks (1 or 2)
Type: DDR4 SDRAM
Size: One or two banks, 5 GB each
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73741: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Standard 6U or 3U cPCI board

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New!

Models 72851 73851 and 74851

2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

Model 74851 *Model 73851*

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUC (digital upconverter)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized version available

General Information

Models 72851, 73851 and 74851 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71851 XMC modules mounted on a cPCI carrier board. Model 72851 is a 6U cPCI board while the Model 73851 is a 3U cPCI board; both are equipped with one Model 71851 XMC. Model 74851 is a 6U cPCI board with two XMC modules rather than one.

They include two or four A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As. In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

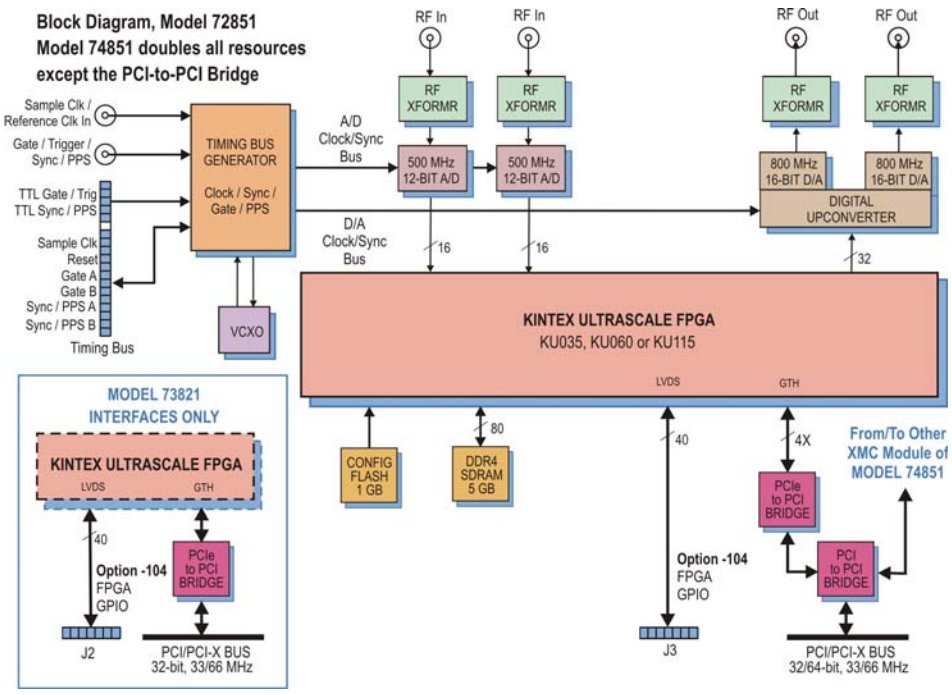
The factory-installed functions of these models include two or four A/D acquisition and two or four waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: two or four powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for data clocking and synchronization functions; test signal generators; programmable interpolators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions thereby saving the time of IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their ➤



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2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/As waveforms stored in either on-board memory or off-board host memory.

➤ own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

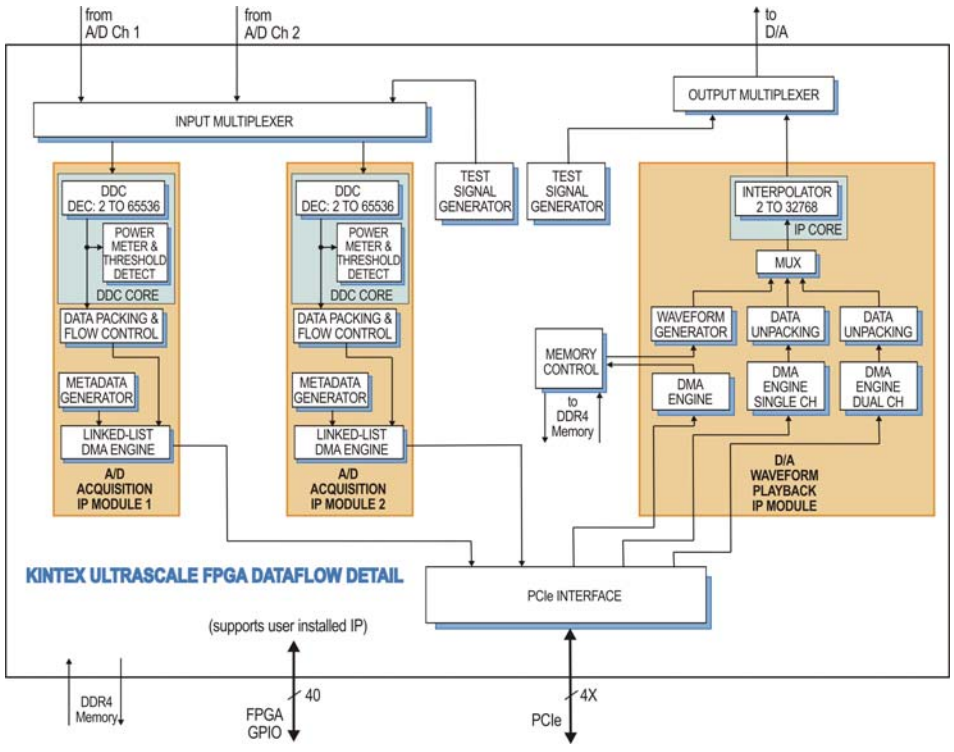
Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73851: 32 bits only. ➤

Models 72851 73851 and 74851

2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

➤ Specifications

Model72851: 2 A/Ds
Model 73851: 2 A/Ds
Model 74851: 4 A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters (2 or 4)
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core (1 or 2)
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851

Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73851: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in (233.35 mm x 170.61 mm)
3U Board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

Ordering Information

Model	Description
72851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U cPCI
73851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U cPCI
74851	4-Channel 500 MHz A/D with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGAs - 6U cPCI
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged version

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New!

Models 72861 73861 & 74861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - cPCI

Model 74861 *Model 73861*

General Information

Models 72861, 73861 and 74861 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71861 XMC modules mounted on a cPCI carrier board. Model 72861 is a 6U board while Model 73861 is a 3U board; both have one Model 71861 module. Model 74861 is equipped with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

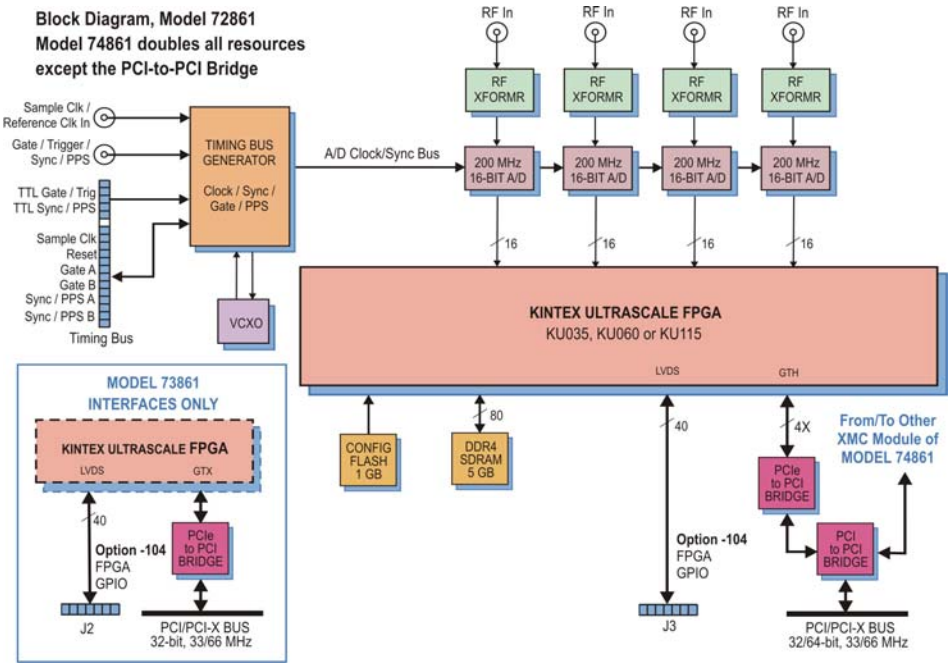
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available



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Models 72861 73861 & 74861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73861; J3 connector, Model 72861; J3 and J5 connectors, Model 74861.

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

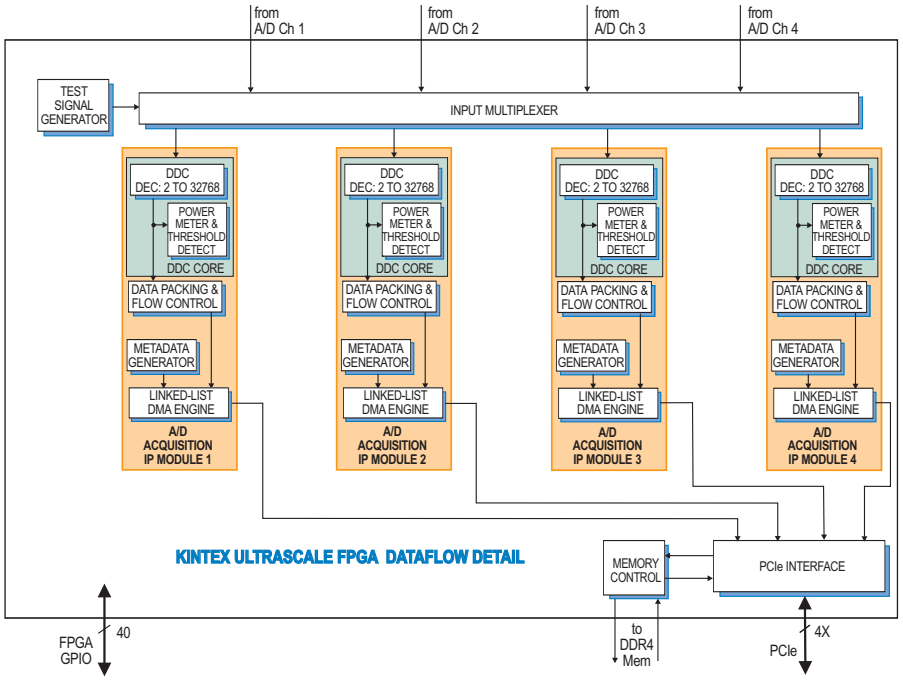
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Models 72861 73861 & 74861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73861: 32 bits only.

Specifications

Models 72861 and 73861: 4 A/Ds
Model 74861: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (4 or 8)
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** LVDS I/O between the FPGA and J2 connector, Model 73861; J3 connector, Model 72861; J3 and J5 connectors, Model 74861

Memory (1 or 2 banks)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB or 10 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73861: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: **6U** board 6.299 in x 9.173 in (160.00 mm x 233.00 mm)
3U board 3.937 in x 6.299 in (100.00 mm x 160.00 mm)

Ordering Information

Model	Description
72861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI
73861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI
74861	8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U cPCI
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73861; J3 connector, Model 72861; J3 and J5 connectors, Model 74861
- 702	Air cooled, Level L2

New!

Models 72862 73862 & 74862

4- or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

Model 74862 *Model 73862*

General Information

Models 72862, 73862 and 74862 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71862 XMC modules mounted on a cPCI carrier board. Model 72862 is a 6U board while Model 73862 is a 3U board; both have one Model 71862 module. Model 74862 is equipped with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

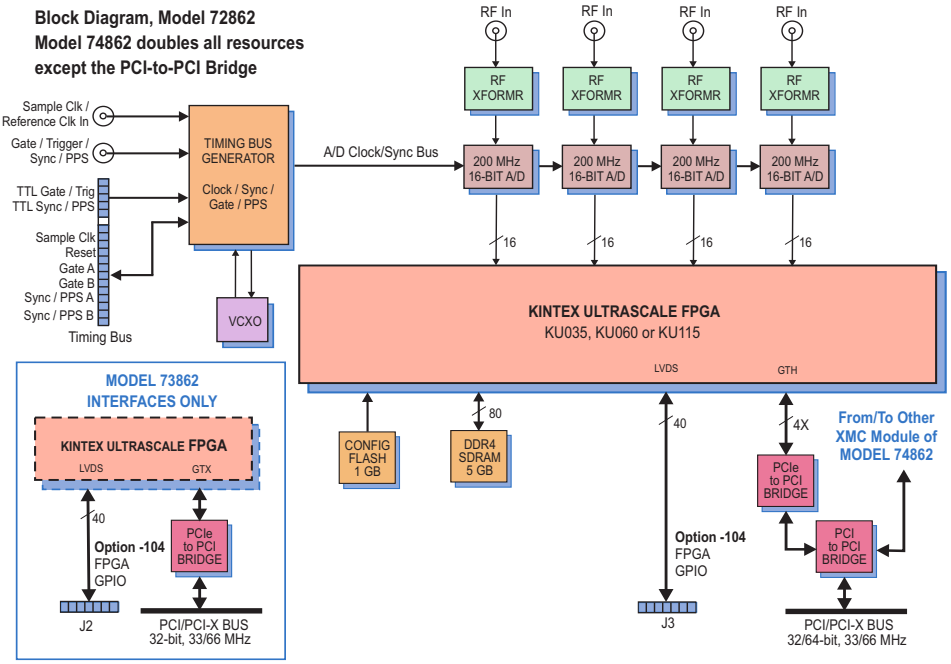
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight wideband DDCs and
- 32 or 64 multiband DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available



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www.pentek.com

Models 72862 73862 & 74862

4- or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862.

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

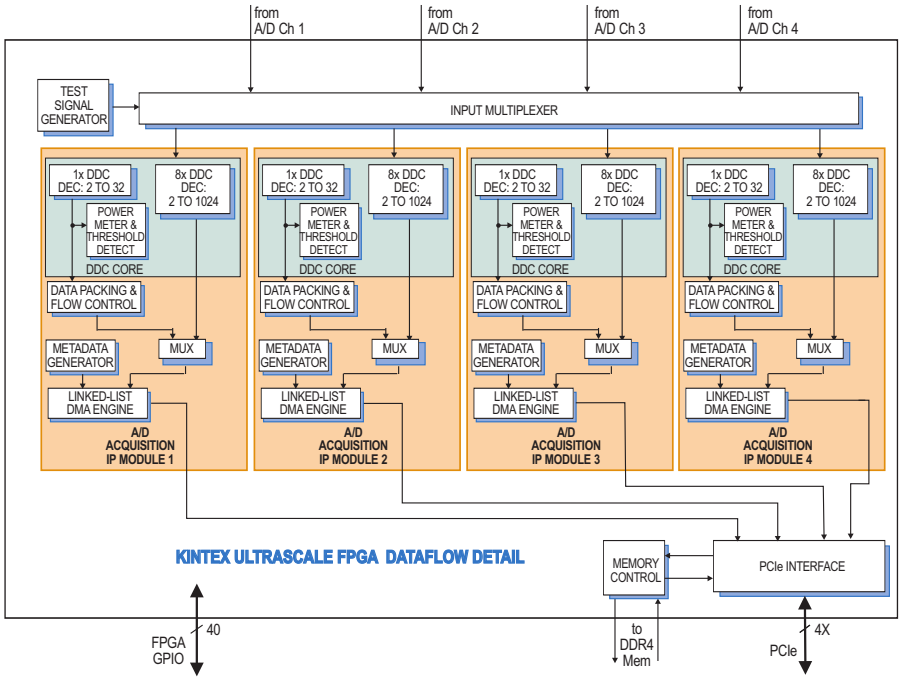
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 72862 73862 & 74862

4- or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73862: 32 bits only.

Specifications

Models 72861 and 73861: 4 A/Ds
Model 74861: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s,idependent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** LVDS I/O between the FPGA and J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862

Memory (1 or 2 banks)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB or 10 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73862: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: **6U** board 6.299 in x 9.173 in (160.00 mm x 233.00 mm)
3U board 3.937 in x 6.299 in (100.00 mm x 160.00 mm)

Ordering Information

Model	Description
72862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U cPCI
73862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 3U cPCI
74862	8-Channel 200 MHz A/D with multiband DDCs and two Kintex UltraScale FPGAs - 6U cPCI
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862)
- 702	Air cooled, Level L2

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New!

Models 72800 73800 and 74800

Kintex UltraScale FPGA Coprocessor - cPCI

Model 74800 *Model 73800*

JADE NAVIGATOR Design Suite

General Information

Models 72800, 73800 and 74800 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a cPCI carrier board. Model 72800 is a 6U cPCI board while the Model 73800 is a 3U cPCI board; both are equipped with one Model 71800 XMC. Model 74800 is a 6U cPCI board with two XMC modules rather than one.

In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

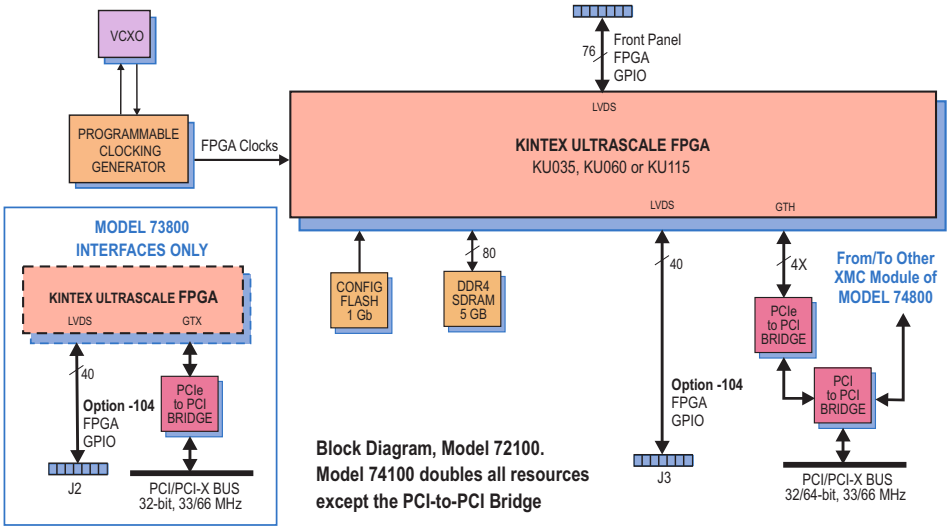
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73800; J3 connector, Model 72800; J3 and J5 connectors, Model 74800.➤

Features

- High-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- 5 or 10 GB of DDR4 SDRAM
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled version available



Block Diagram, Model 72100. Model 74100 doubles all resources except the PCI-to-PCI Bridge

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Models 72800 73800 and 74800

Kintex UltraScale FPGA Coprocessor - cPCI

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73800: 32 bits only.

Front-Panel Digital I/O Interface

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Memory Resources (1 or 2)

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

Specifications

Front Panel Digital I/O (1 or 2)
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 or 76 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73800; J3 connector, Model 72800; J3 and J5 connectors, Model 74800

Memory (1 or 2)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

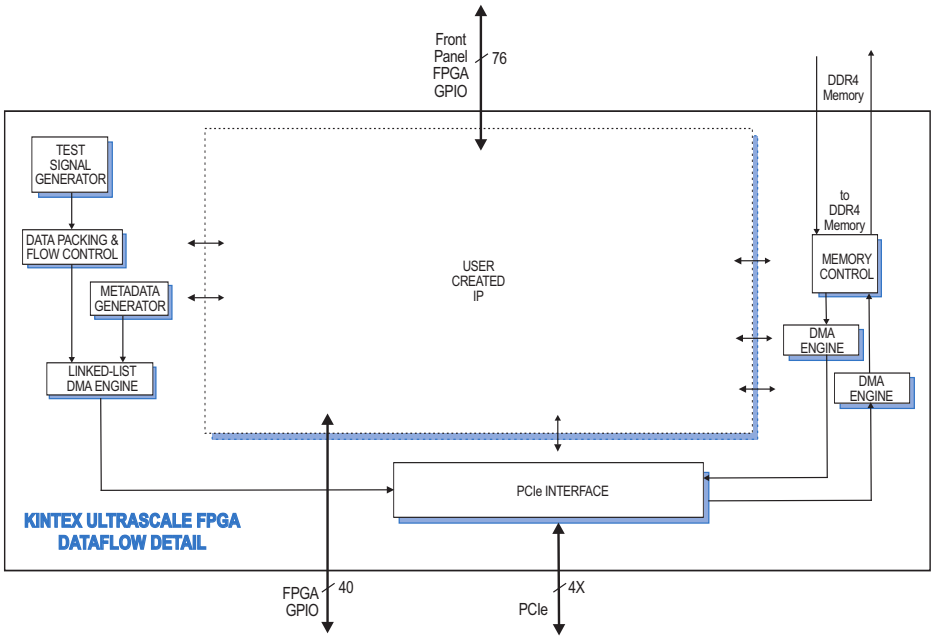
PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73800: 32 bits only

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: **6U Board** 9.187 in x 6.717 in (233.35 mm x 170.61 mm)
3U Board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



Ordering Information

Model	Description
72800	Kintex UltraScale FPGA Coprocessor - 6U cPCI
73800	Kintex UltraScale FPGA Coprocessor - 3U cPCI
74800	Kintex UltraScale FPGA Coprocessor - 6U cPCI

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged version

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Models 7220, 7420 and 7320

Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI

Model 7420 *Model 7320*

Bandit

ReadyFlow Board Support Package

Features

- Accept RF signals from 400 MHz to 4000 MHz
- Accept RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

General Information

These Bandit® models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded cPCI boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 7320 is a 3U cPCI booard while Model 7220 is a 6U cPCI board; both provide two channels, while Model 7420 is a double-density 6U cPCI board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

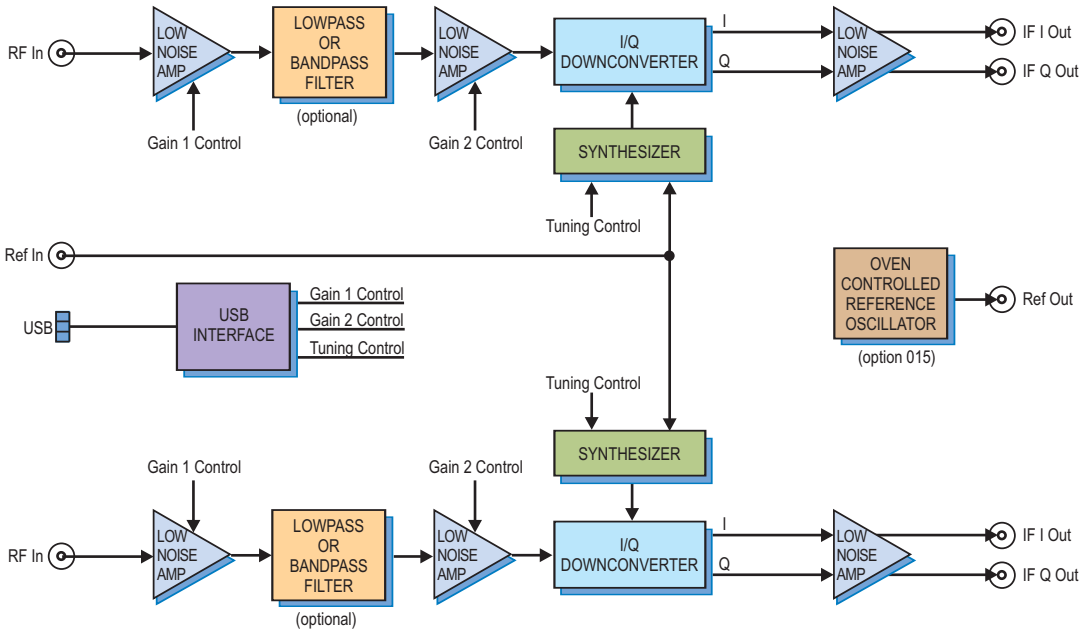
On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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Models 7220, 7420 and 7320

Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI

➤ Specifications

RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** –60 dBm to –20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

Phase Noise
- **1 kHz:** –90 dBc/Hz
- **100 kHz:** –110 dBc/Hz
- **1 MHz:** –130 dBc/Hz

Noise Figure (referred to input)
- **60 dB gain:** 2.6 dB

Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedence:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

Reference Output Signal
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm
- **Aging**
  - **Daily:** ±10 ppb/day
  - **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm
- **Phase Noise**
  - **1 Hz Offset:** –67 dBc/Hz
  - **10 Hz Offset:** –100 dBc/Hz
  - **100 Hz Offset:** –130 dBc/Hz
  - **1 KHz Offset:** –148 dBc/Hz
  - **10 KHz Offset:** –154 dBc/Hz
  - **100 KHz Offset:** –155 dBc/Hz

IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz), power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board

Ordering Information

Model	Description
7220	Bandit Two-Channel Analog RF Wideband Downconverter - 6U cPCI
7320	Bandit Two-Channel Analog RF Wideband Downconverter - 3U cPCI
7420	Bandit Four-Channel Analog RF Wideband Downconverter - 6U cPCI

Option	Description
-015	Oven Controlled Reference Oscillator
-145	1.45 GHz lowpass input filter
-280	2.80 GHz lowpass input filter

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RADAR & SDR I/O - x8 PCI Express

MODEL	DESCRIPTION
Cobalt 78620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - x8 PCIe
Cobalt 78621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - x8 PCIe
Cobalt 78624	Dual-Channel, 34-Signal Adaptive IF Relay - x8 PCIe
Cobalt 78630	1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe
Cobalt 78640	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - x8 PCIe
Cobalt 78641	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Wideband DDC, Virtex-6 FPGA - x8 PCIe
Cobalt 78650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - x8 PCIe
Cobalt 78651	2-Chan 500 MHz A/D with DDC, DUC with 2-Chan 800 MHz D/A, Virtex-6 FPGA - x8 PCIe
Cobalt 78660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - x8 PCIe
Cobalt 78661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe
Cobalt 78662	4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - x8 PCIe
Cobalt 78663	1100-Channel GSM Channelizer with Quad A/D - x8 PCIe
Cobalt 78664	4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - x8 PCIe
Cobalt 78670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe
Cobalt 78671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe
Cobalt 78690	L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe
Cobalt 7809	4-Channel SFP Transceiver PCIe Module for Cobalt Boards
Onyx 78720	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - x8 PCIe
Onyx 78721	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - x8 PCIe
Onyx 78730	1 GHz A/D and D/A, Virtex-7 FPGA - x8 PCIe
Onyx 78741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC,Virtex-7 FPGA - x8 PCIe
Onyx 78751	2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - x8 PCIe
Onyx 78760	4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - x8 PCIe
Onyx 78761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - x8 PCIe
Onyx 78791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - x8 PCIe
Jade 78131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe
Jade 78132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - x8 PCIe
Jade 78141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - x8 PCIe
Jade 78821	3-Channel 200 MHz A/D, DDC, DUC 2_Channel 800 MHz D/A, Kintex UltraScale FPGA - x8 PCIe
Jade 78841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - x8 PCIe
Jade 78851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - x8 PCIe
Jade 78861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - x8 PCIe
Jade 78862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - x8 PCIe
Jade 78800	Kintex UltraScale FPGA Coprocessor - x8 PC Ie
Bandit 7820	Two-Channel Analog RF Wideband Downconverter - PCIe
8266	PC Development System for PCIe Cobalt, Onyx, Flexor, and Jade boards
	Customer Information

RADAR & SDR I/O - PMC/XMC

Click Here for the PRODUCT SELECTOR

RADAR & SDR I/O - CompactPCI

RADAR & SDR I/O - 3U VPX - FORMAT 1

RADAR & SDR I/O - AMC

RADAR & SDR I/O - 3U VPX - FORMAT 2

RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated: March 2018

Model 78620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - x8 PCIe

General Information

Model 78620 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78620 includes optional general-purpose and gigabit serial card edge connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

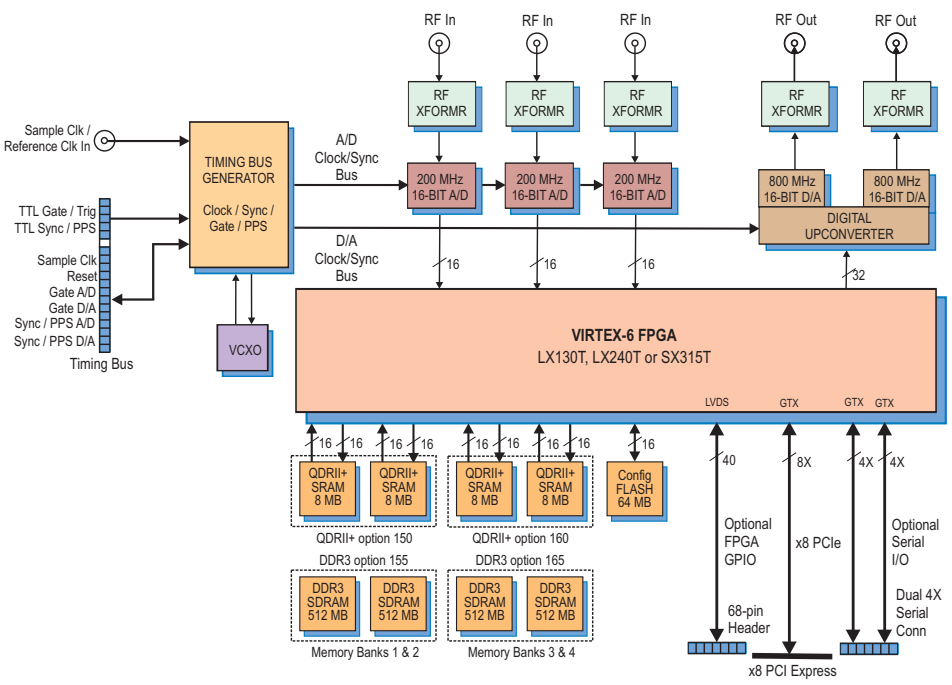
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

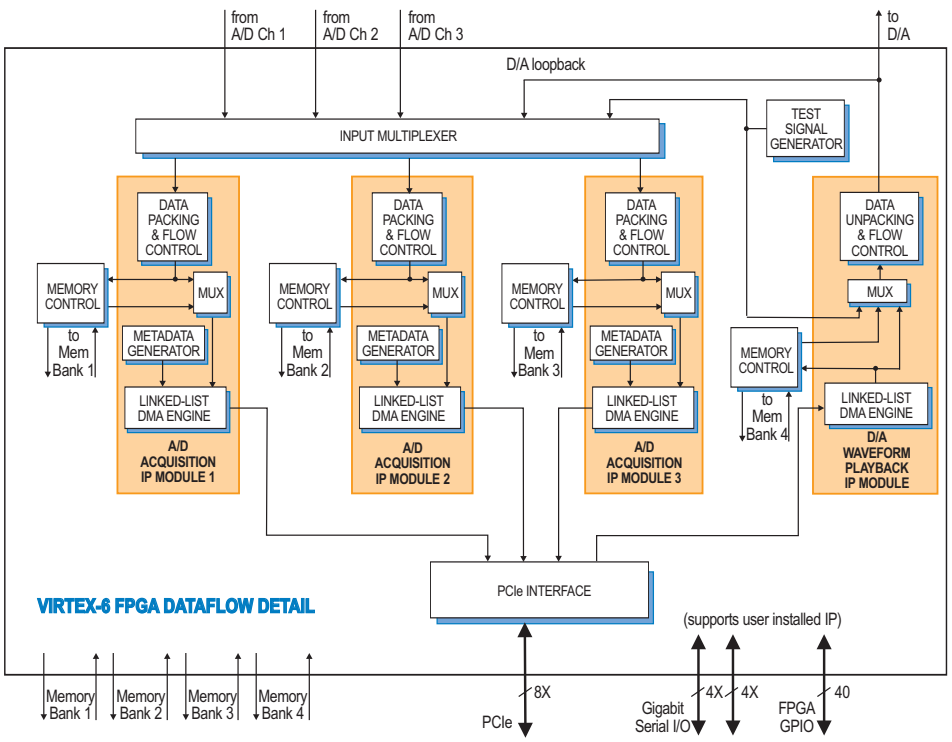
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System. See 8266 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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Model 78621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

General Information

Model 78621 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turn-key solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78621 includes an optional general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

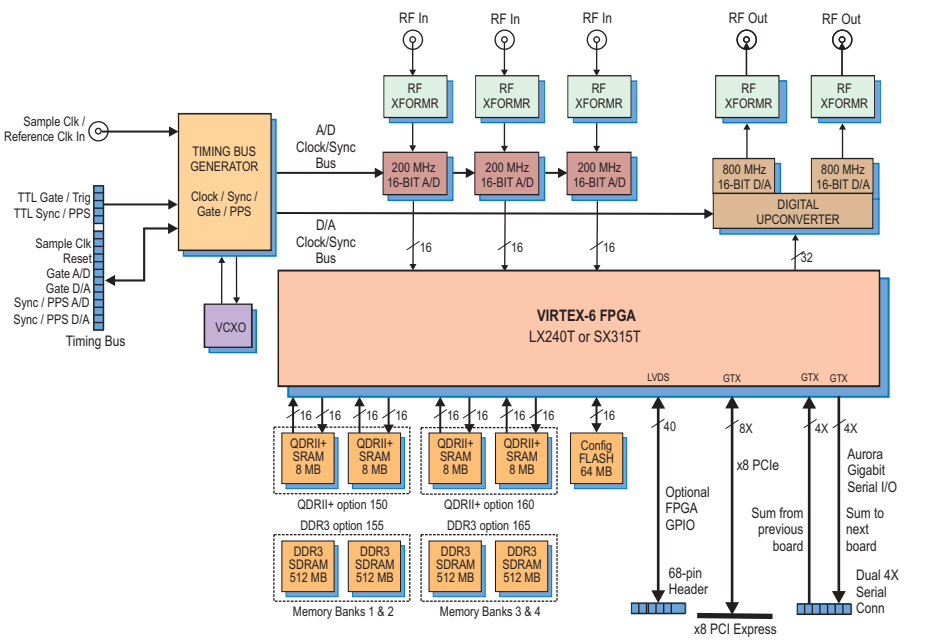
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

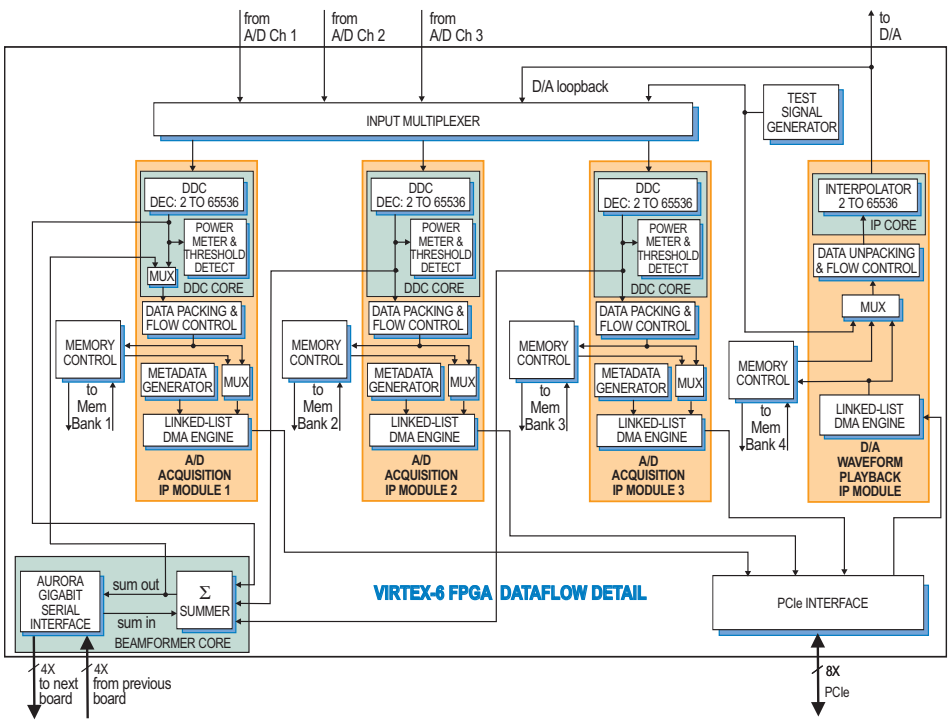
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 78621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to crate a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 78621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

Options:

-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78624

Dual-Channel, 34-Signal Adaptive IF Relay - x8 PCIe

Cobalt

Features

- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/As
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

General Information

Model 78624 is a member of the Cobalt® family of high-performance PCI Express boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 78624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 78624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

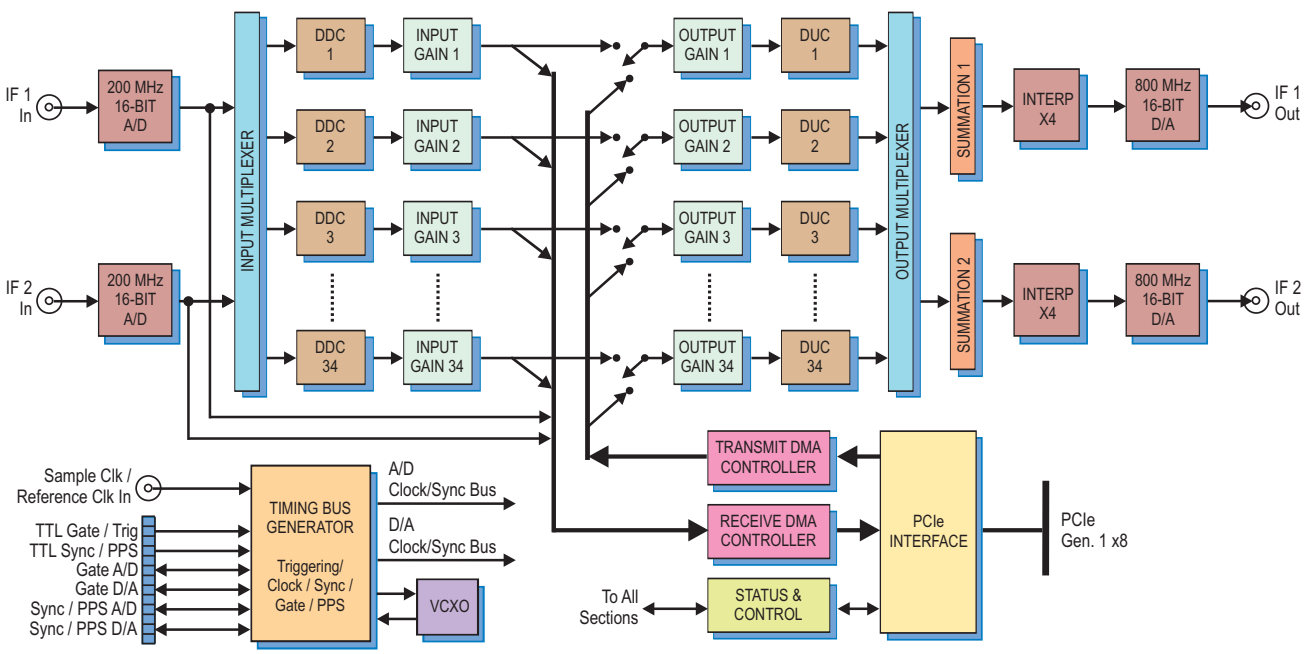
Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 78624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two summation blocks, each ➤



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➤associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 78624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 78624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 78624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz. ➤

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78624's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

The Model 78624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

Model 78624 — Dual-Channel, 34-Signal Adaptive IF Relay - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78624	Dual-Channel 34-Signal Adaptive IF Relay - PCIe

Options:

-064	XC6VSX315T (required)
-730	2-slot heatsink

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
- **Quantity:** 34
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Required:** Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8

Environmental
- **Standard:**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78630

1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

General Information

Model 78630 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

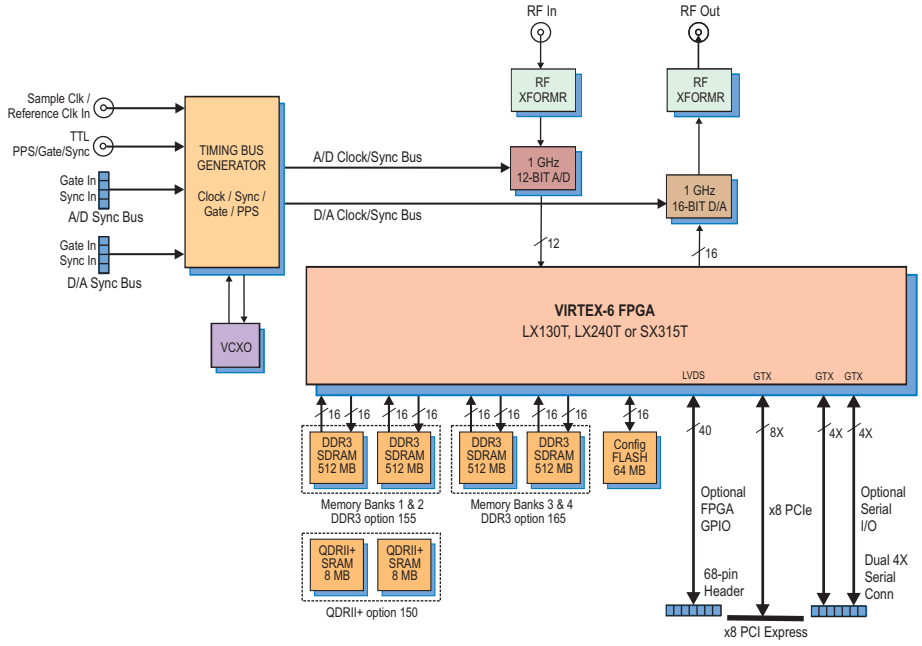
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78630

1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Module

The 78630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

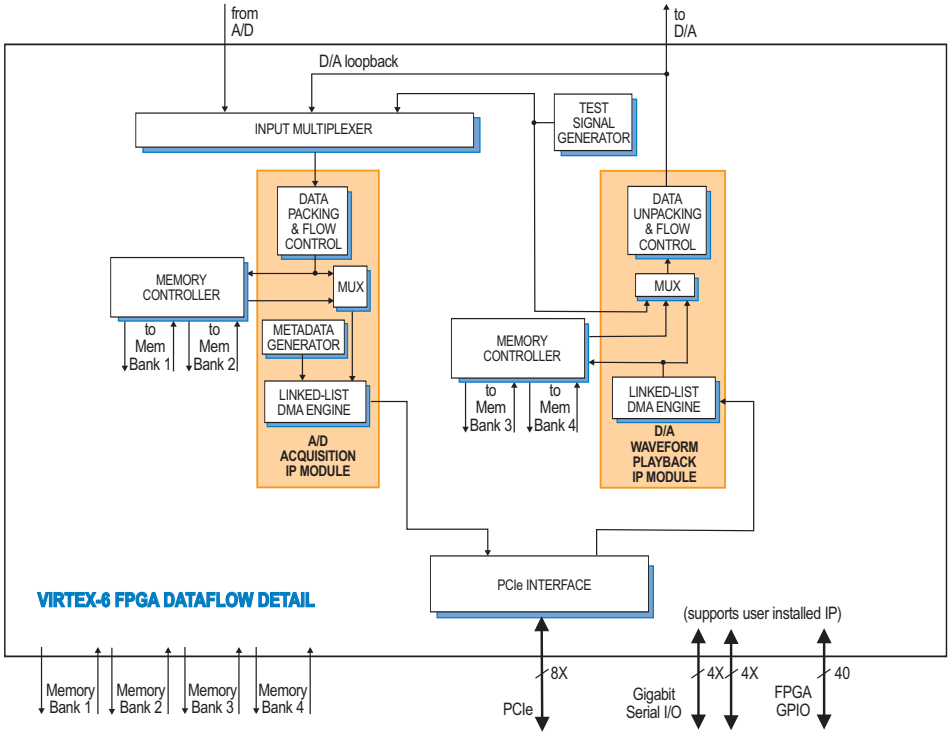
A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7892 and Model 9192 Cobalt Synchronizers can drive multiple 78630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 78630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78630

1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
78630	1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen.1: x4 or x8
Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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Model 78640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

General Information

Model 78640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 78640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78640 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

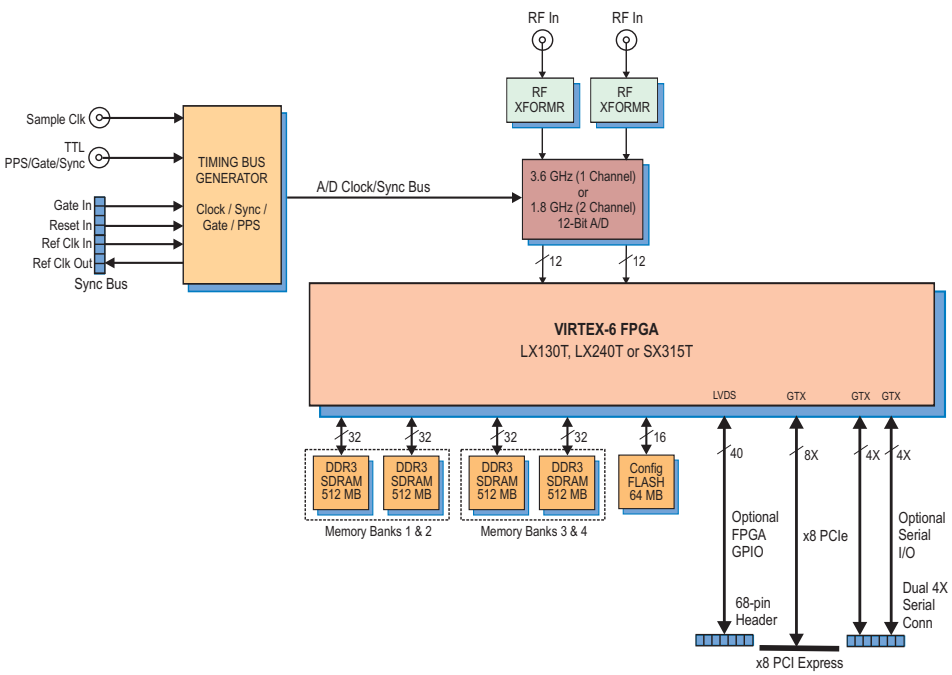
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 78640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 78640s can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The 78640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

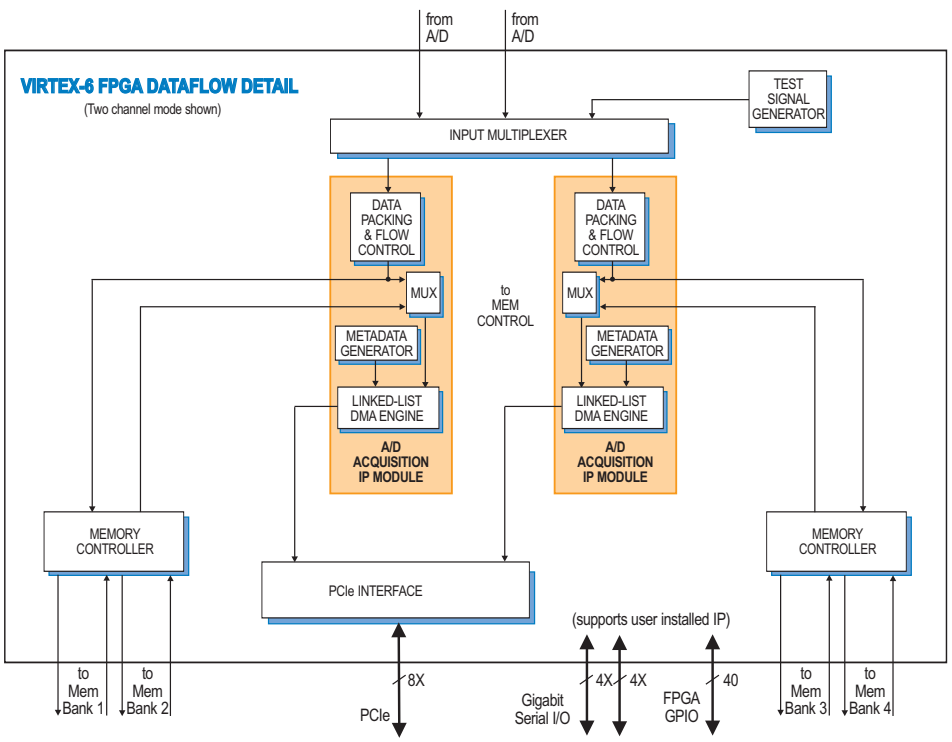
The Model 78640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Module

The 78640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 XC6VSX315T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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Model 78641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - x8 PCIe

General Information

Model 78641 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78641 includes an optional connection to the Virtex-6 FPGA for custom I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

A/D Converter Stage

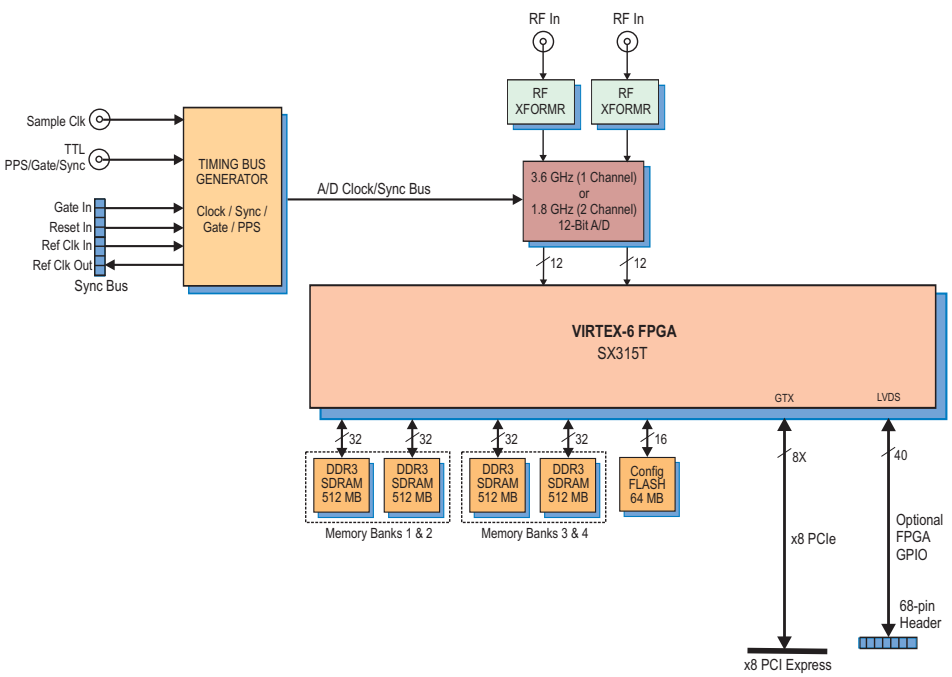
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources. ➤

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Module

The 78641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

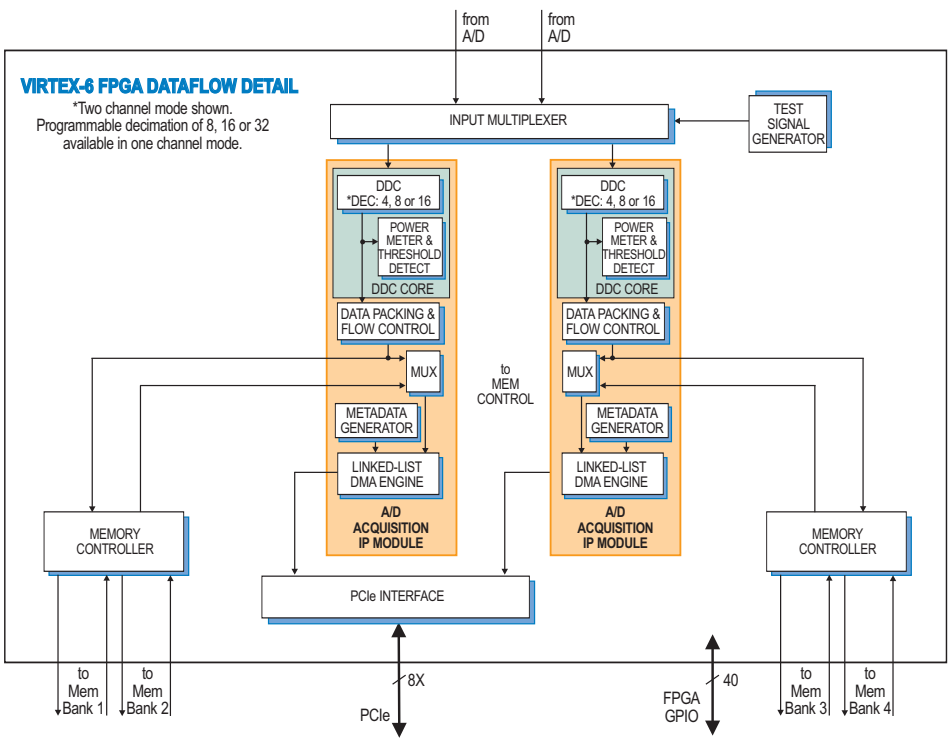
➤ Clocking and Synchronization

The 78641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 78641's can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The 78640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Model 78641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - x8 PCIe

➤ PCI Express Interface

The Model 78641 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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Model 78650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - x8 PCIe

General Information

Model 78650 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78650 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

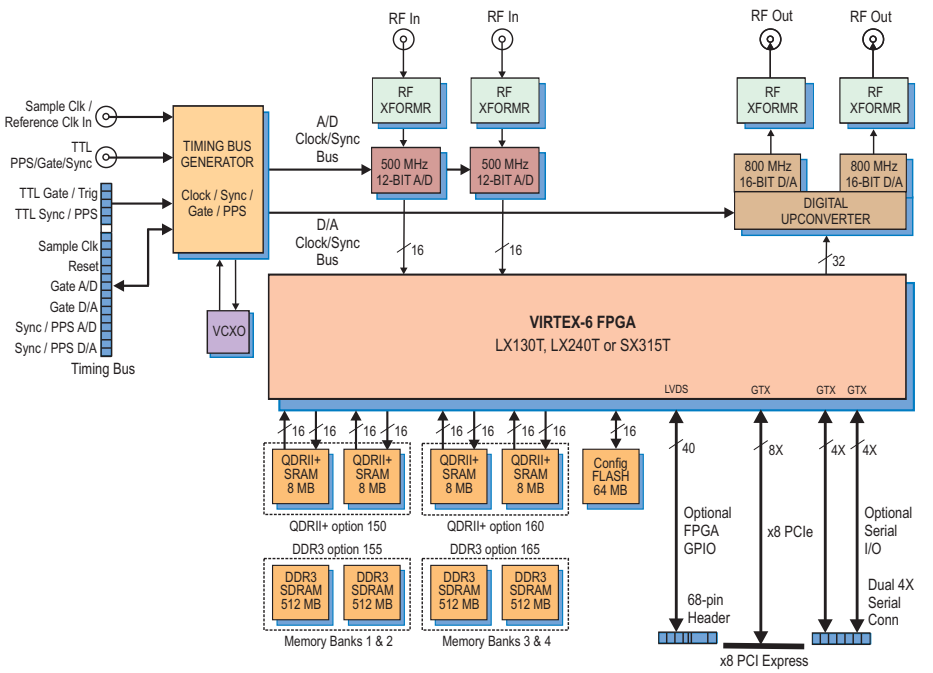
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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www.pentek.com

A/D Acquisition IP Modules

The 78650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

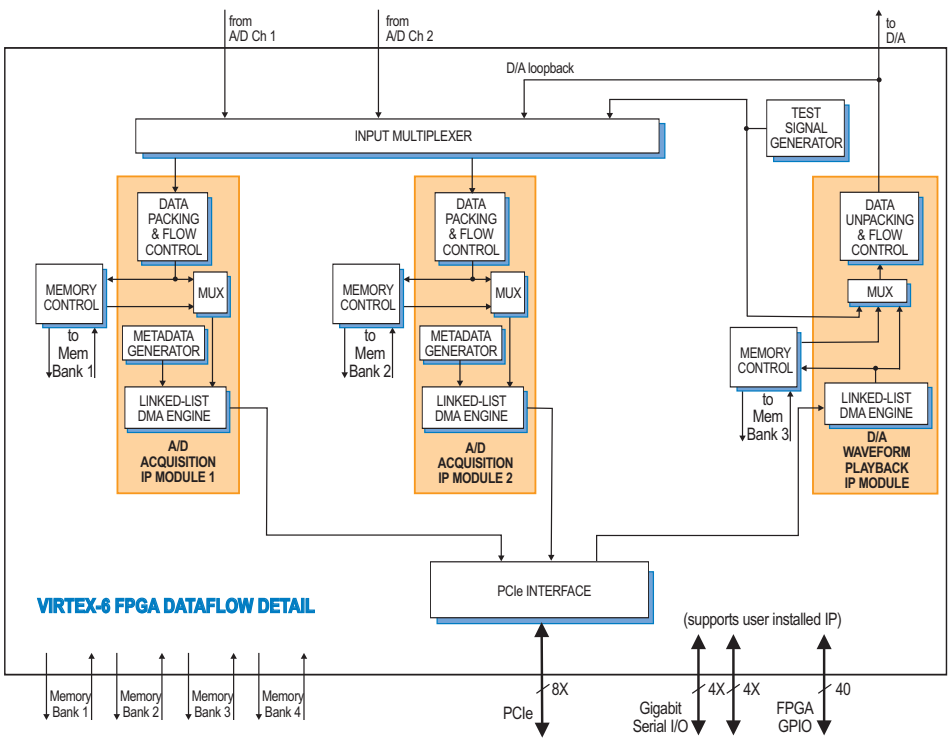
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
78650	Two 500 MHz A/Ds, one DUC, two 800 MHz D/As with Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen.1: x4 or x8 Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

General Information

Model 78651 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 78651 includes two A/Ds, two D/As and four banks of memory. It features native support for PCI Express Gen 2.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78651 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core.

The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

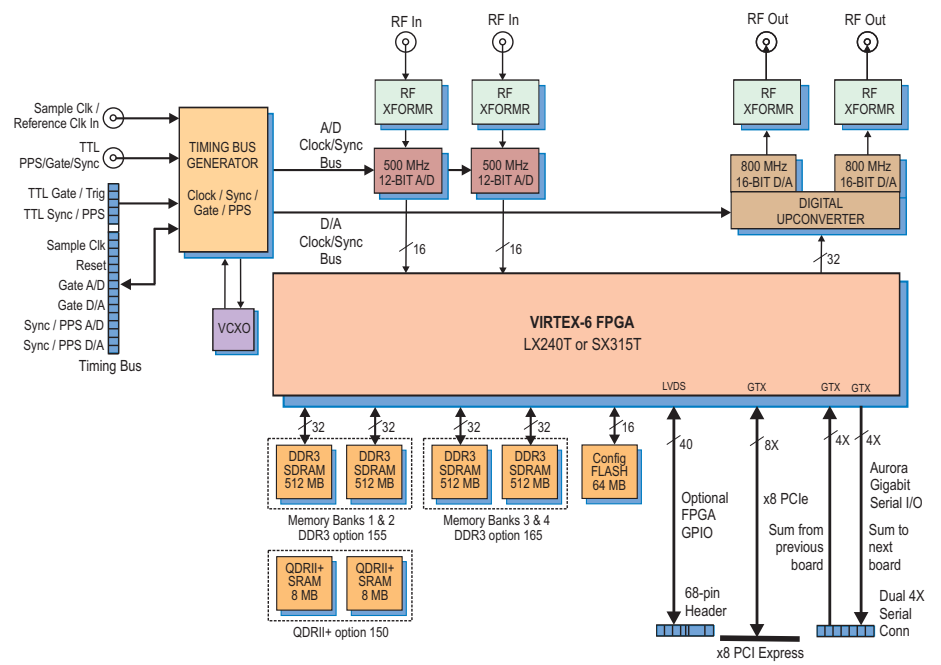
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- PCI Express (Gen. 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

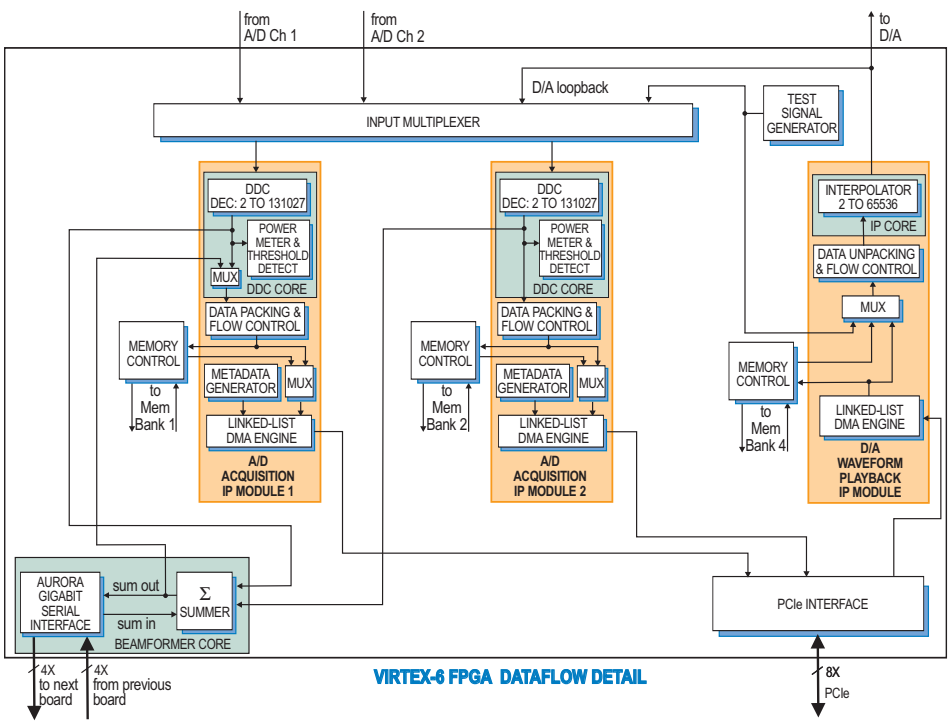
A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78651's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 78651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



VIRTEX-6 FPGA DATAFLOW DETAIL

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through a 68-pin DIL connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via via a dual 4X connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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Model 78660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - x8 PCIe

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78660 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78660 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory- installed functions and enable the 78660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

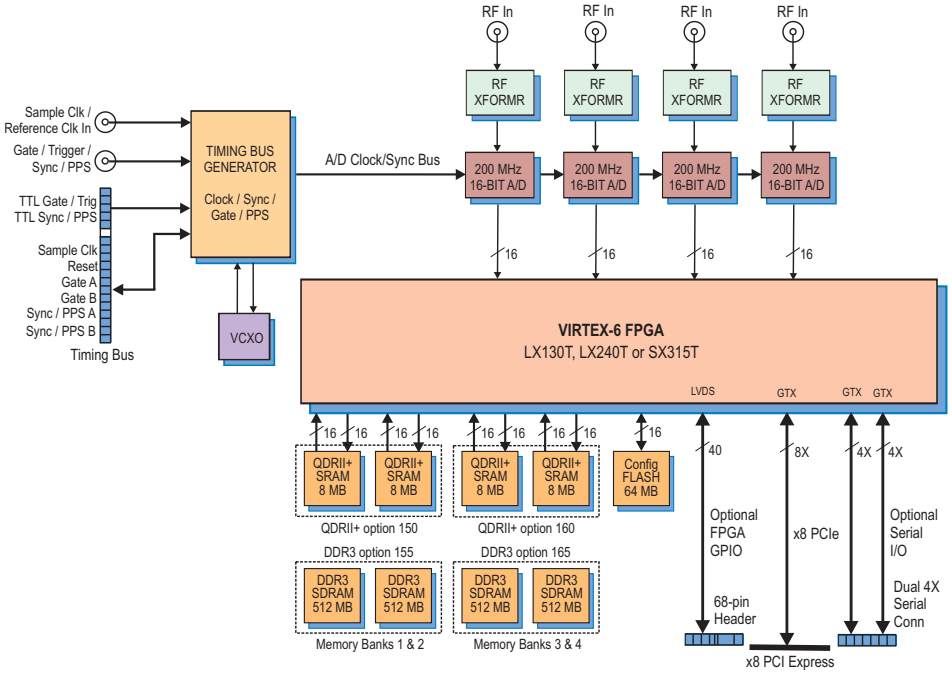
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤



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4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - x8 PCIe

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

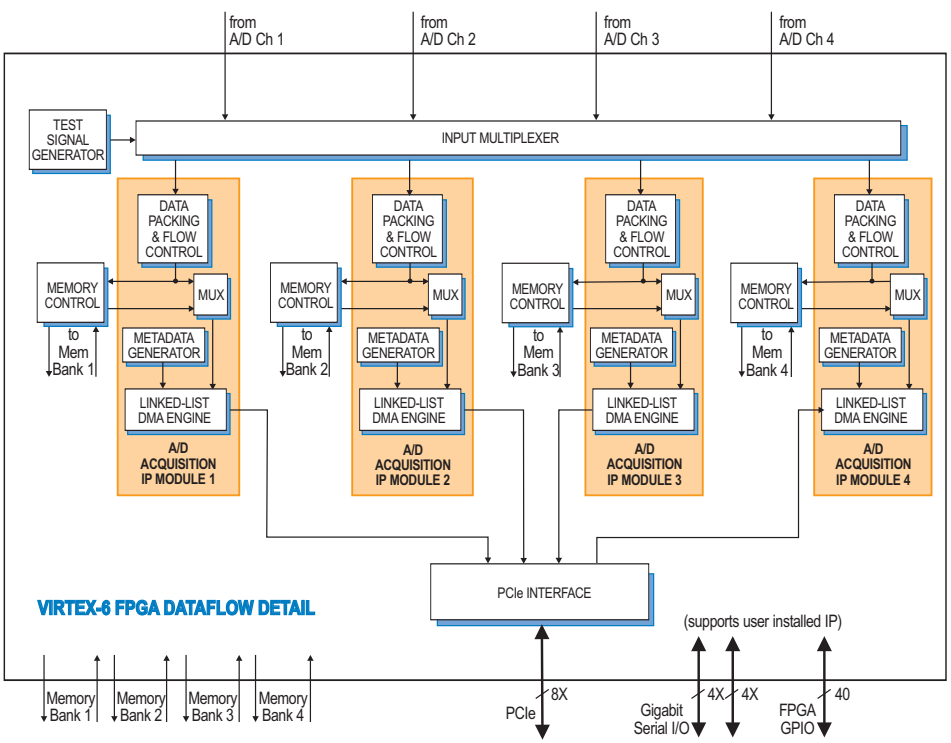
The Model 78660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Modules

The 78660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 78660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - x8 PCIe

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78660	4-Channel 200 MHz A/D with Virtex-6 FPGA - PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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Model 78661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe

General Information

Model 78661 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78661 includes an optional general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable the 78661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

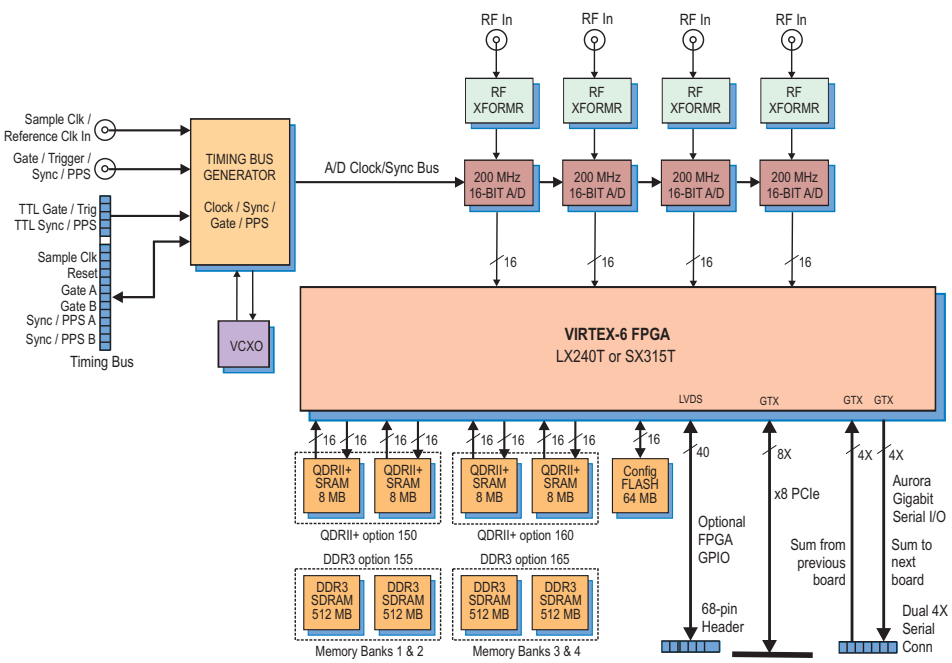
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

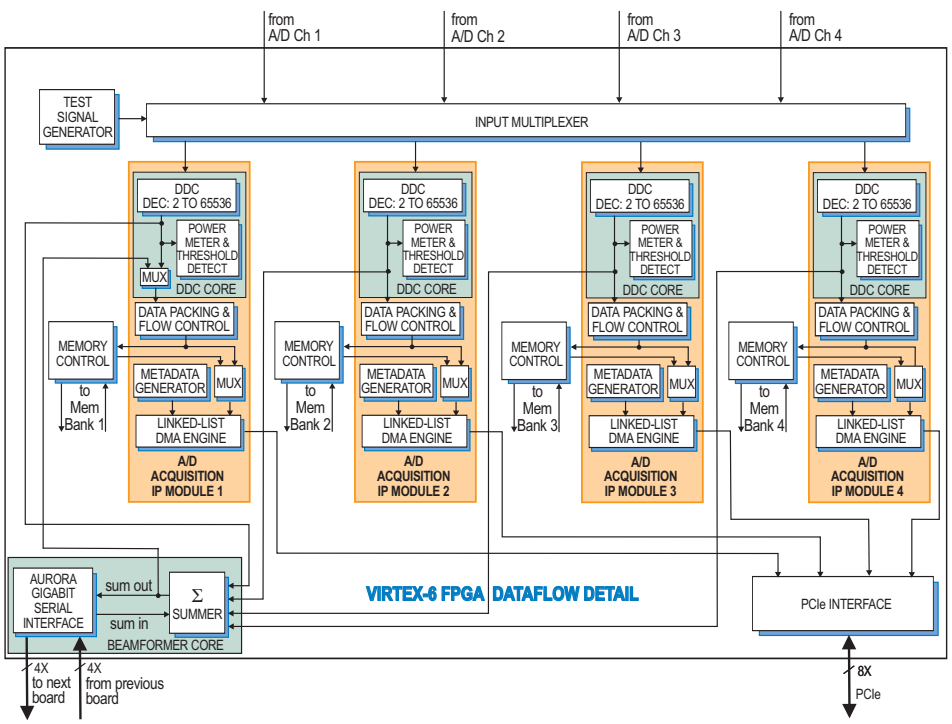
➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ➤



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Model 78661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe

PCI Express Interface

The Model 78661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe Links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78621	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78661's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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Model 78662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe

General Information

Model 78662 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78662 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 78662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

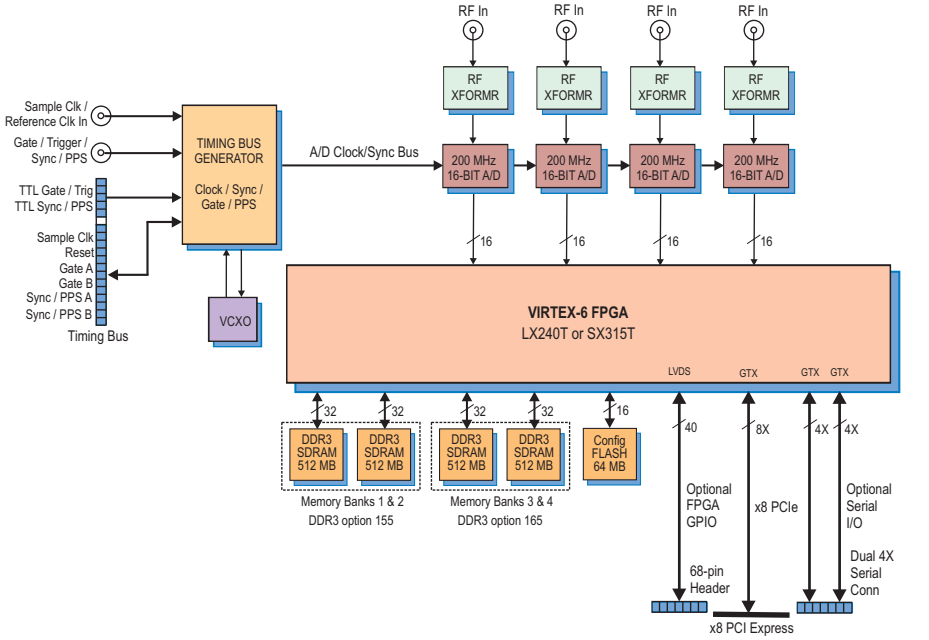
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable serial gigabit interfaces
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe

A/D Acquisition IP Modules

The 78662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

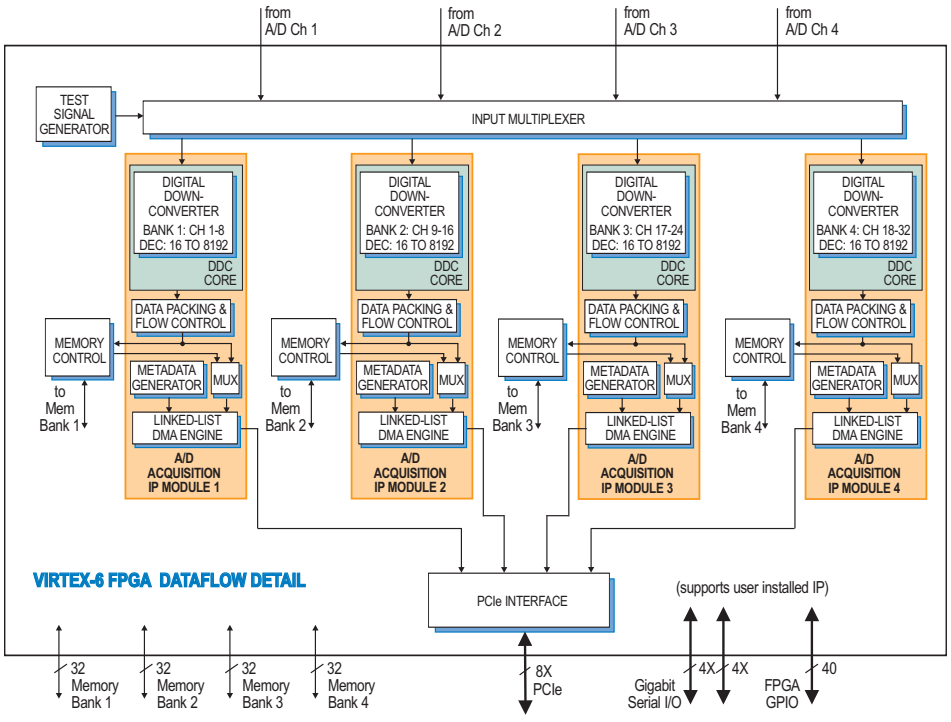
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
78662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78663

1100-Channel GSM Channelizer with Quad A/D - x8 PCIe

Cobalt

ReadyFlow Board Support Package

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

General Information

Model 78663 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 78663 is a complete, full-featured subsystem, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

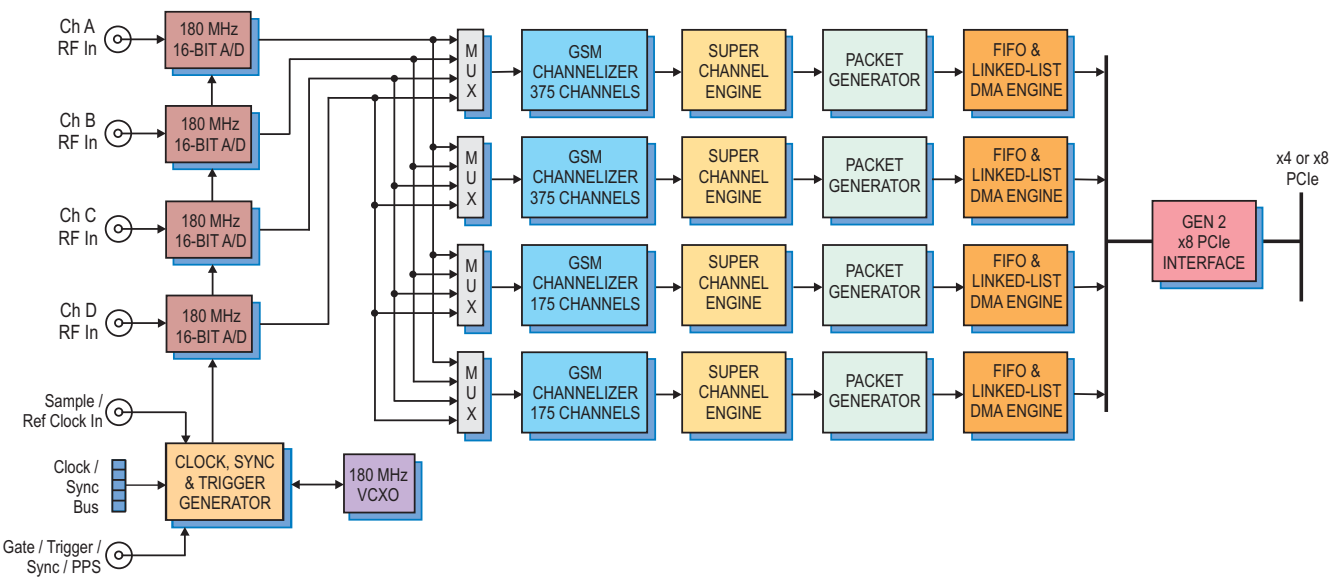
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 78663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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➤ The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 78663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 78663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI Express Interface

The Model 78663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 78663 and host. ➤

Model 78663 — 1100-Channel GSM Channelizer with Quad A/D - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s:** Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: $-f_s/4$ (-270.8333 kHz)
  - Second: 0 Hz
  - Third: $+f_s/4$ (+270.8333 kHz)
  - Fourth: $+f_s/2$ (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 x 7.13 in.

Ordering Information

Model	Description
78663	1100-Channel GSM Channelizer with Quad A/D- PCIe

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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New!

Model 78664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - x8 PCIe

General Information

Model 78664 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution. The 78664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78664 includes an optional general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable the 78664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

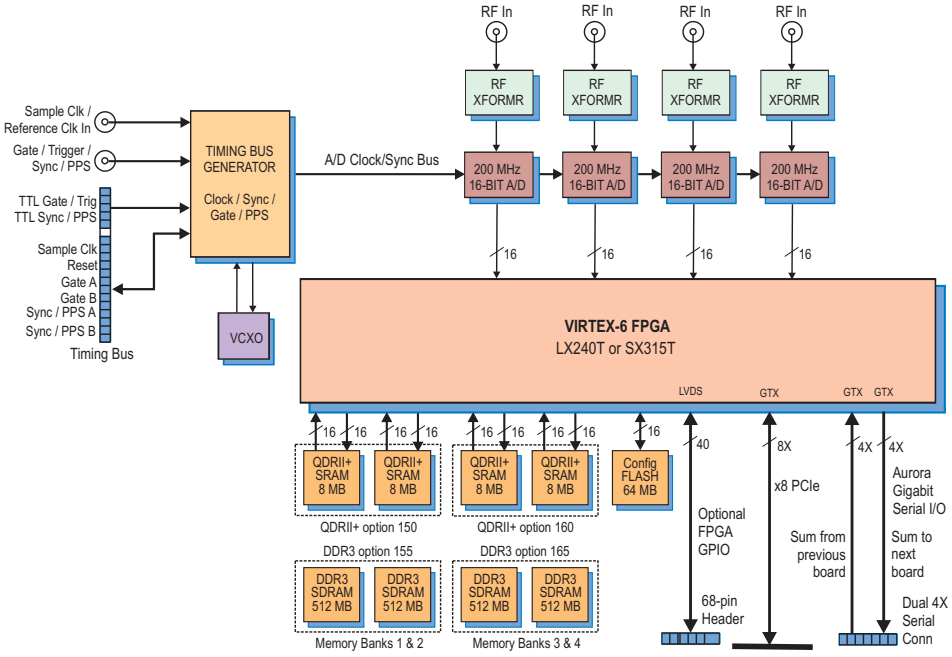
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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A/D Acquisition IP Modules

The 78664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78664 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

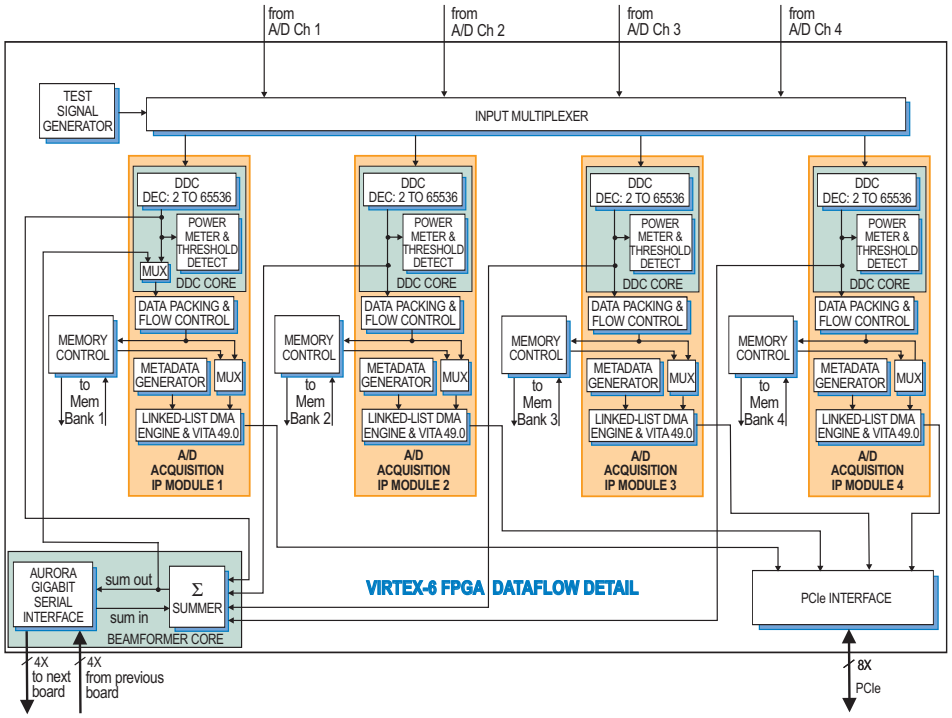
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78664's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 78664 supports fully the VITA 49.0 specification. ➤



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➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78664's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe Links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 78664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - x8 PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

➤

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe

General Information

Model 78670 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78670 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

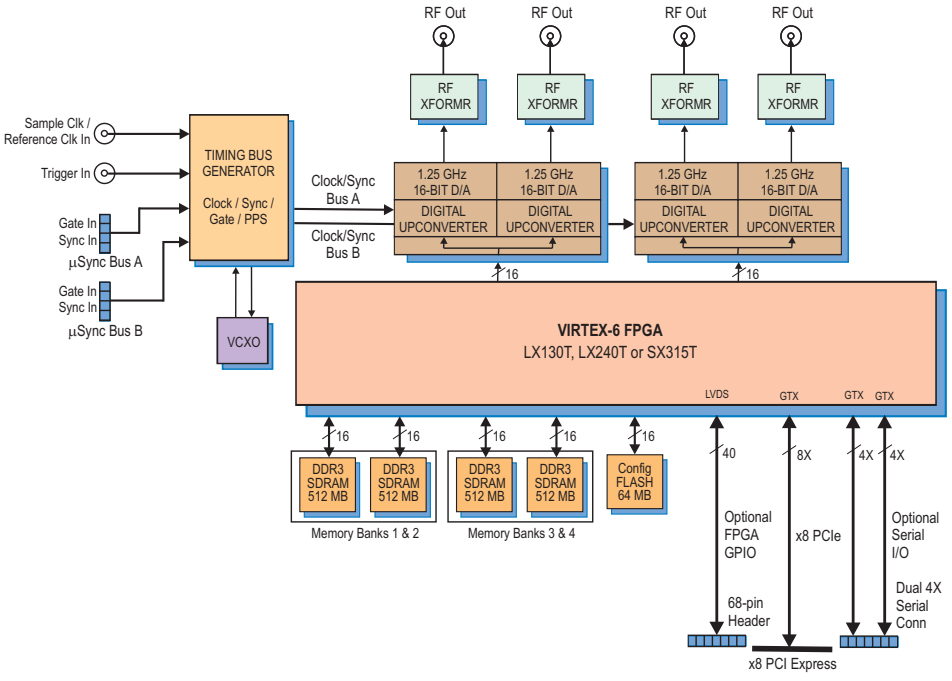
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7892 or 9192 Cobalt Synchronizers can drive multiple 78670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 78670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

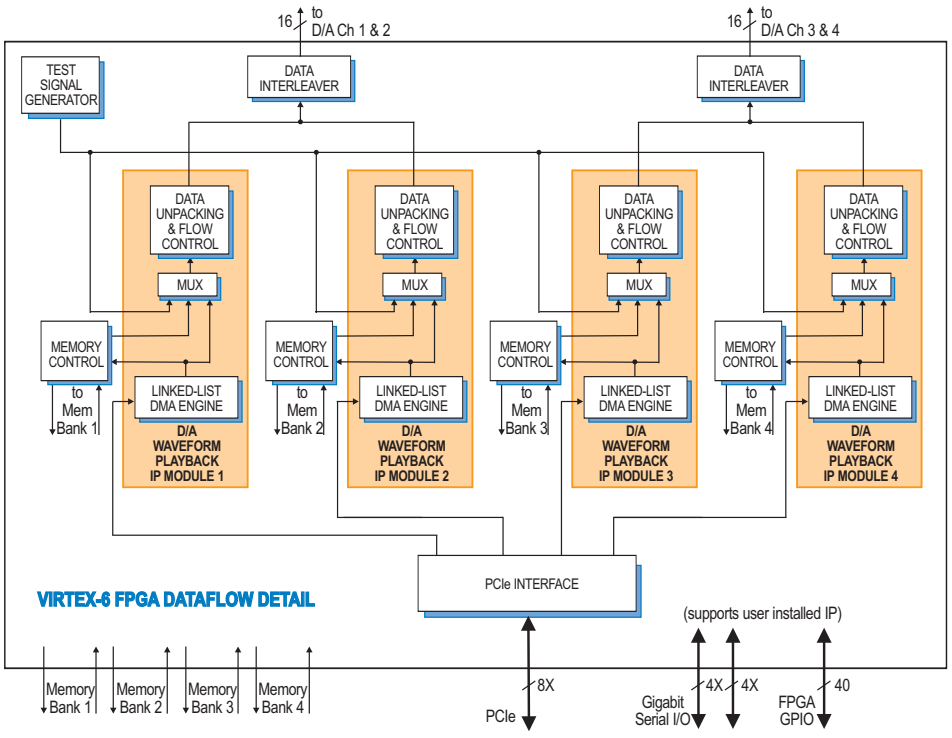
The Model 78670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

D/A Waveform Playback IP Module

The Model 78670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78670 — 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Model 78671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

General Information

Model 78671 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

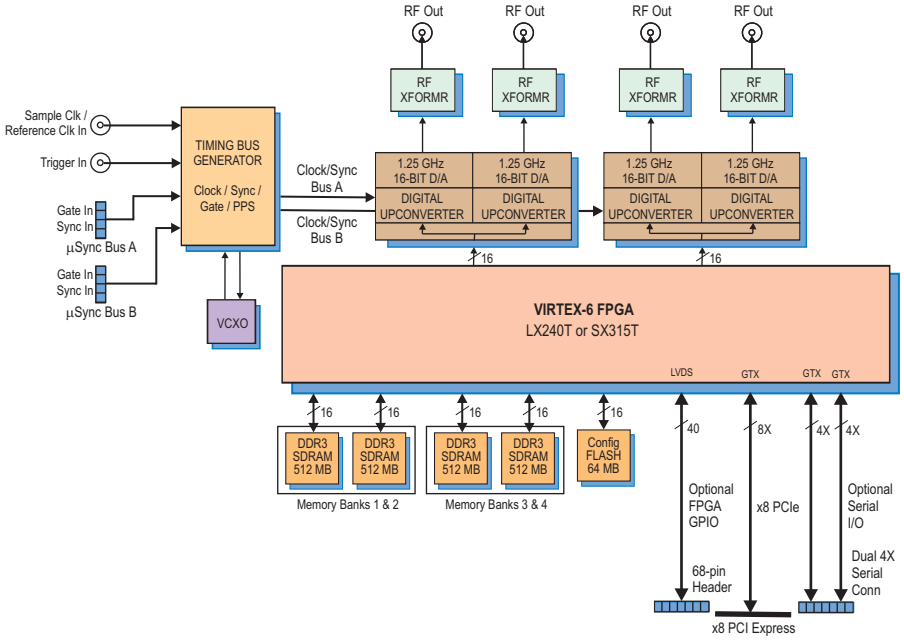
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 78671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user-selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 78671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7892 or 9192 Cobalt Synchronizers can drive multiple 78671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 78671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

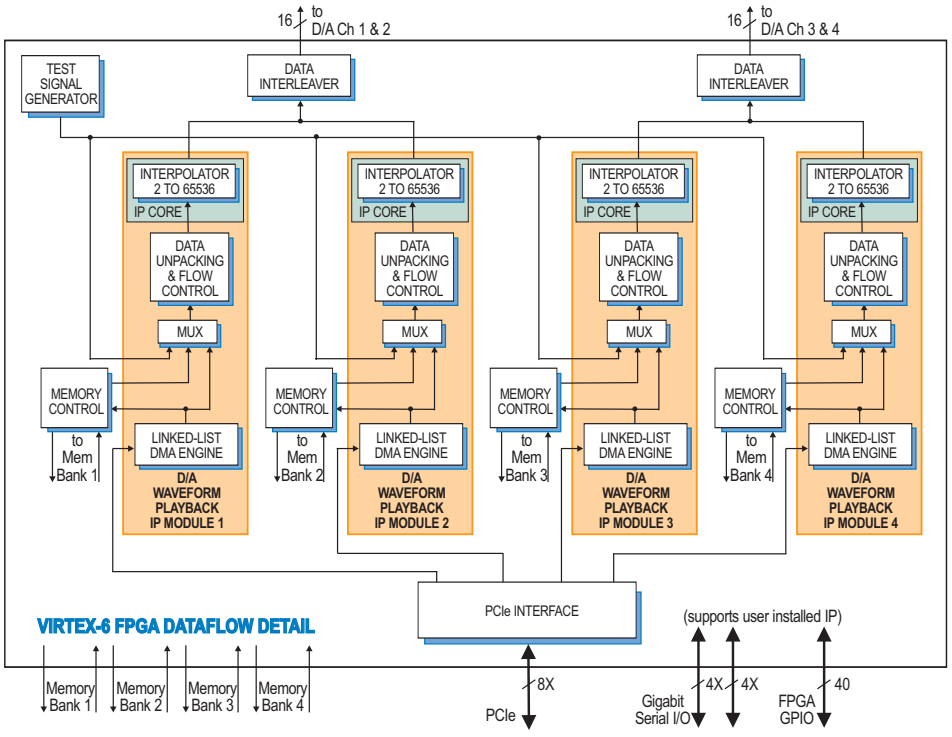
D/A Waveform Playback IP Module

The Model 78671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Model 78671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
78671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ PCI Express Interface

The Model 78671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array:
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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Model 78690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe

General Information

Model 78690 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78690 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

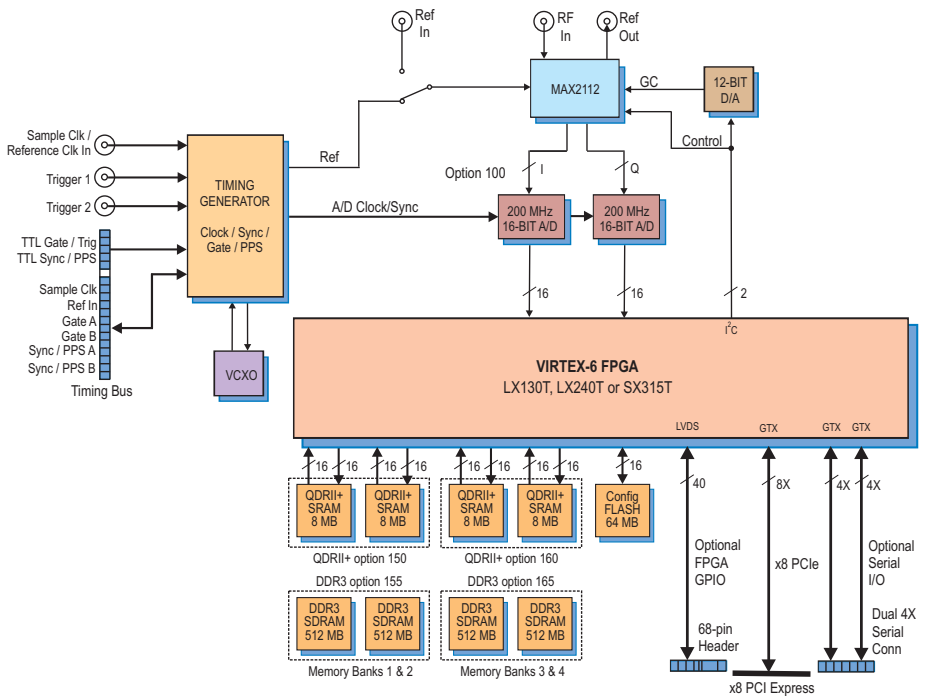
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe

➤ RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

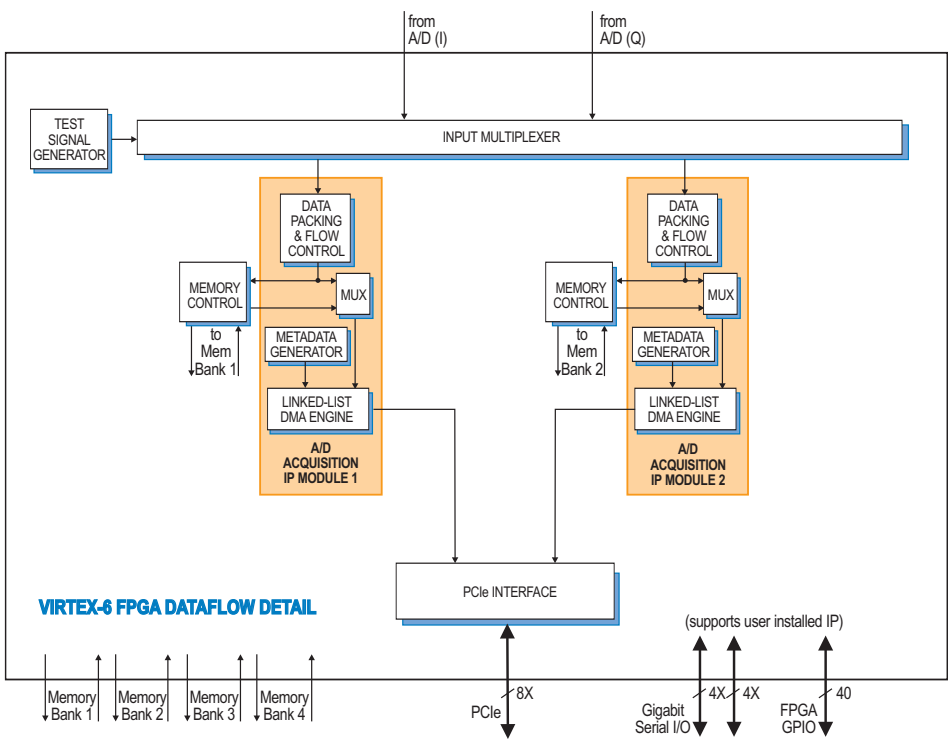
The 78690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤

A/D Acquisition IP Modules

The 78690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

PCI Express Interface

The Model 78690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- ***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2 x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - PCIe
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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Model 7809

4-Channel SFP Transceiver PCIe Module for Cobalt Boards

Features

- Compatible with Pentek 786xx PCI Express Cobalt boards
- Extends range of gigabit serial I/O links
- Four SFP modules drive cable lengths up to 10 km
- Support for both optical and copper cables
- Single-mode and multi-mode fibre optical
- Data rates to 5 Gbits/sec
- Payload data rates to 500 MB/sec for each cable

General Information

Model 7809 is a PCIe module that provides gigabit serial transceiver network cable links for Pentek's Cobalt® family of high performance 786xx PCIe boards based on the Xilinx Virtex-6 FPGA.

The 7809 and the Cobalt board are installed in adjacent slots in a PCIe motherboard or backplane and joined with a gigabit serial flex circuit cable.

The 7809 takes advantage of the small form-factor pluggable (SFP) or Mini-GBIC standard, supporting a variety of hot-pluggable transceiver modules for optical and copper network cables. Up to four modules can be installed.

Since the 7809 is protocol transparent, it is compatible with many protocols including Serial FPDP, PCIe, Xilinx Aurora, Serial-RapidIO, Gigabit Ethernet, SONET, Fibre Channel, and others.

The Cobalt Connection

The 786xx series PCIe Cobalt boards feature two optional 4X gigabit serial connectors along the top edge of the circuit board. These two 4X ports are wired directly to P16 of the XMC module.

The 7809 circuit board has one 4X gigabit serial connector along its top edge. A short flex circuit cable is installed between the 7809 4X connector and one of the two Cobalt 4X connectors.

This provides a full-duplex 4X gigabit serial path between the modules that can operate at serial bit rates to 5 GHz. A second 7809 can be installed adjacent to the Cobalt board to support a second 4X transceiver link.

Each of the four gigabit serial links within a 4X port consists of a transmit pair and a receive pair connected to one SFP module through an equalizer circuit to improve transceiver performance. The Virtex-6 FPGA in the Cobalt module is used to implement the required protocol engine for the P16 4X links to the 7809.

Some Cobalt boards (such as the 78621 and 78661) are equipped with factory-installed FPGA IP supporting Xilinx Aurora links for cascade beamforming summation across multiple boards.

Pentek's GateFlow FPGA Design Kit allows users to implement custom protocols for other applications. GateFlow is compatible with the Xilinx ISE Foundation Tool Suite, and includes a complete project file and VHDL source code.

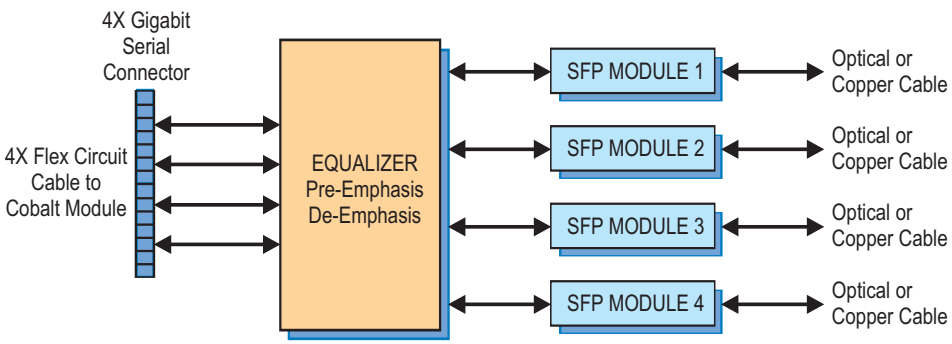
SFP Modules

SFP transceiver modules support a variety of different transmitter and receiver types. These modules simply plug into the SFP sockets so they can be easily installed or replaced by users.

Users can choose the appropriate transceiver for each link to support the required distance and data rates. Both single-mode and multi-mode optical fibre devices are available for cable interconnection distances up to 550 m and 10 km, respectively.

Pentek offers the 7809 with options for either two or four 850 nm multi-mode fibre optical SFP modules installed.

Each 7809 is supplied with the gigabit serial flex circuit cable assembly for connection to a suitably equipped 786xx series PCIe Cobalt module.



Ordering Information

Model Description

7809	4-Channel SFP Transceiver PCIe Module

Options:

-002	Two 850 nm multi-mode fiber optical channel SFPs (500 m distance)
-004	Four 850 nm multi-mode fiber optical channel SFPs (500 m distance)

Contact Pentek for availability of other interfaces

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - x8 PCIe

General Information

Model 78720 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78720 includes optional general-purpose and gigabit-serial card edge connectors for application-specific I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

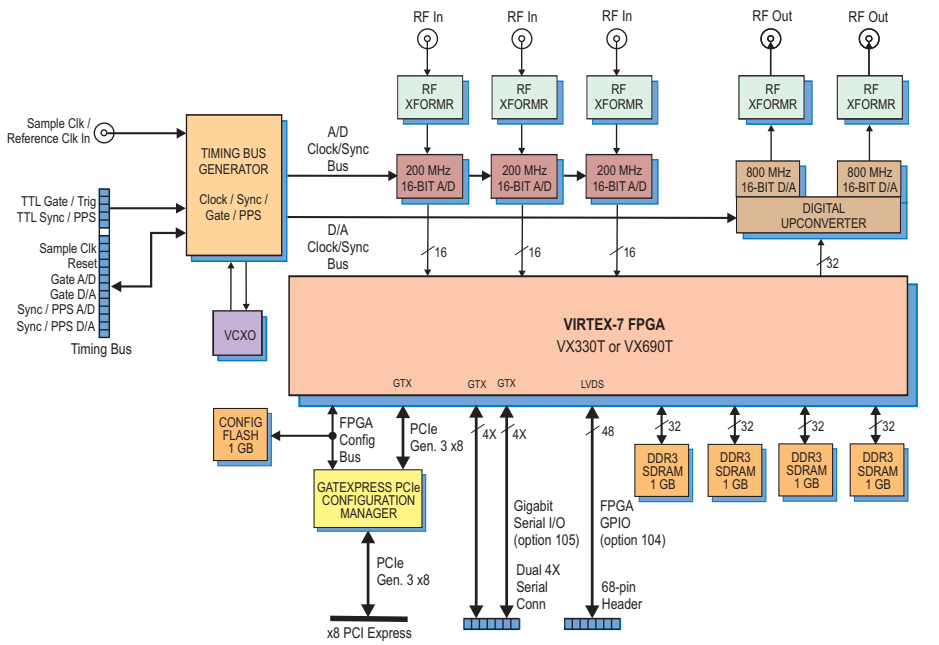
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

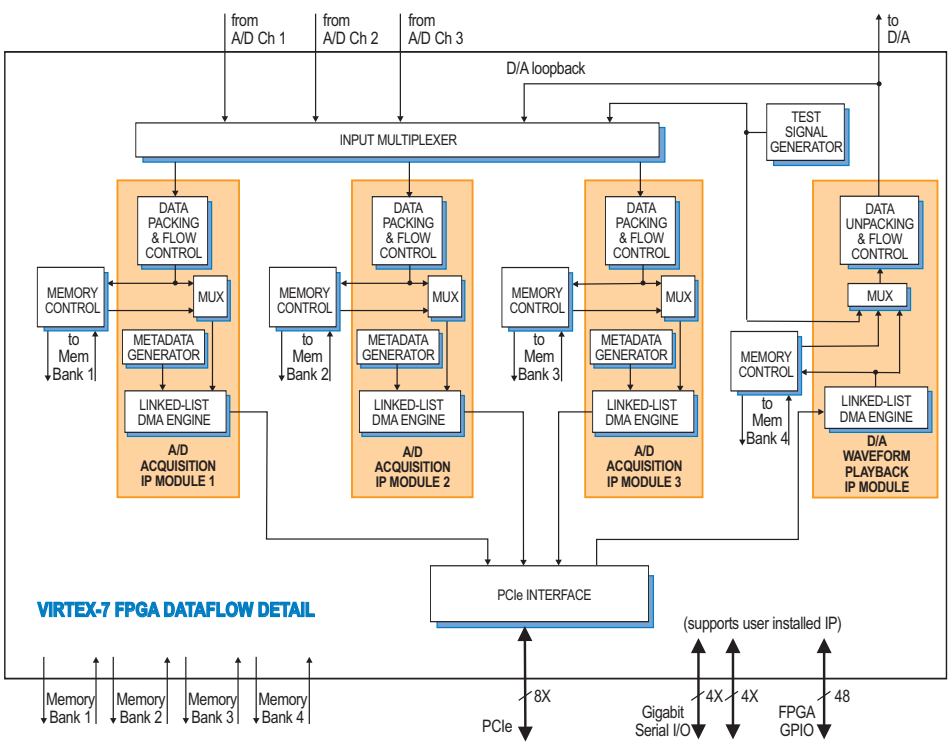
A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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Model 78720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - x8 PCIe

Memory Resources

The 78720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
78720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - PCIe
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

PCI Express Interface

The Model 78720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

Onyx
GateXpress
GateFlow
ReadyFlow
Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 78721 is a member of the Onyx® family of high performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78721 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

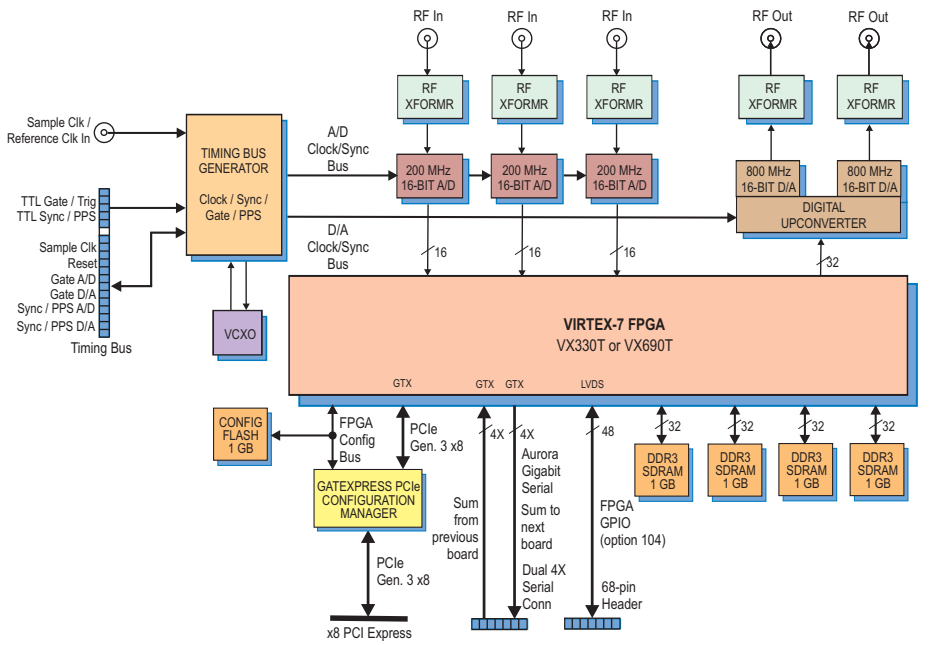
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

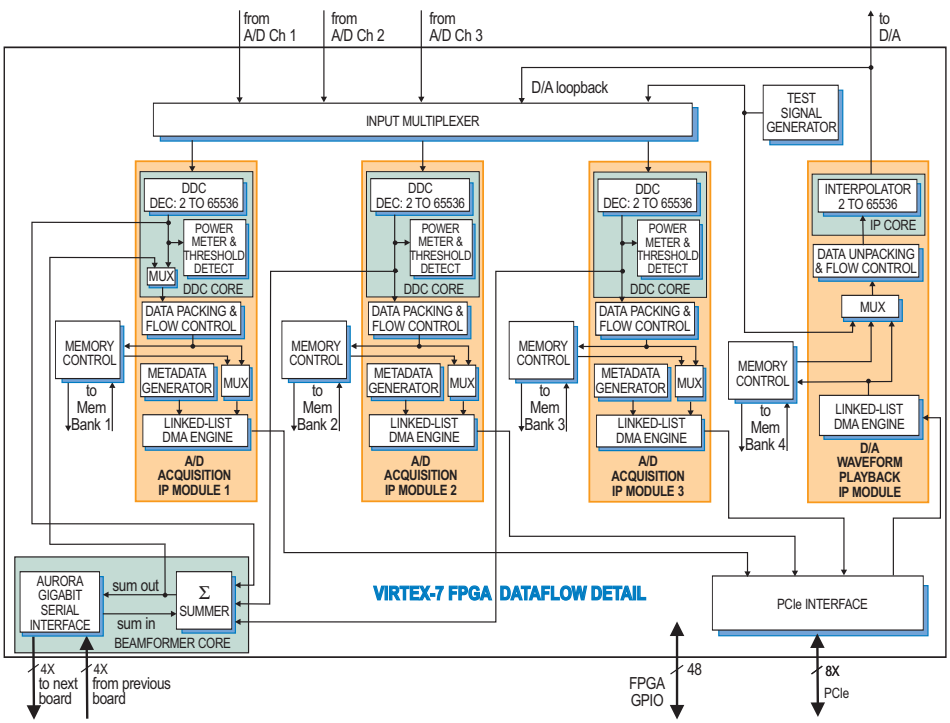
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78721's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 78721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78721's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
76721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Memory Resources

The 78721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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Model 78730

1 GHz A/D and 1 GHz D/A with Virtex-7 FPGA - x8 PCIe

General Information

Model 78730 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78730 includes optional general-purpose and gigabit serial card connectors for application specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

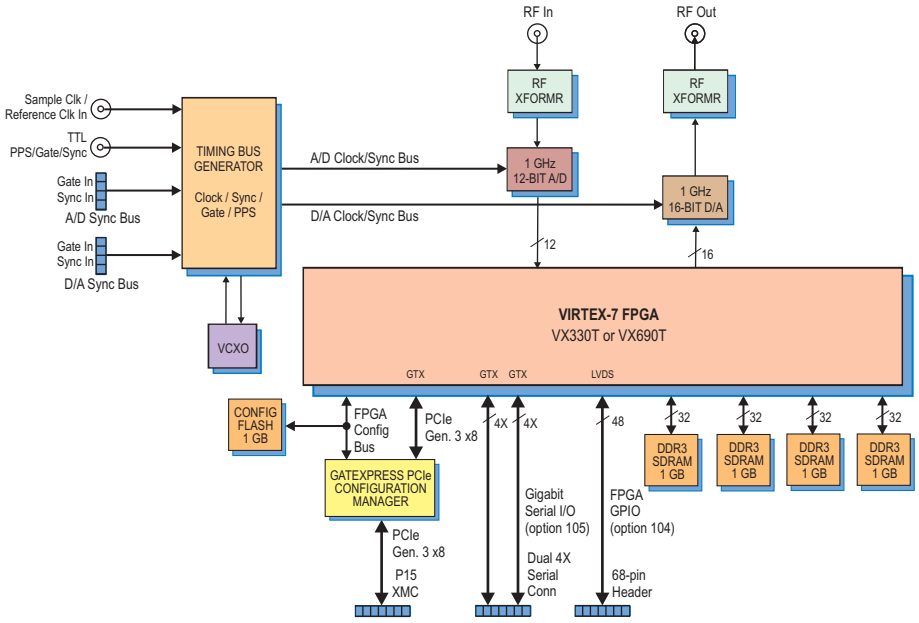
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O



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1 GHz A/D and 1 GHz D/A with Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Module

The 78730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

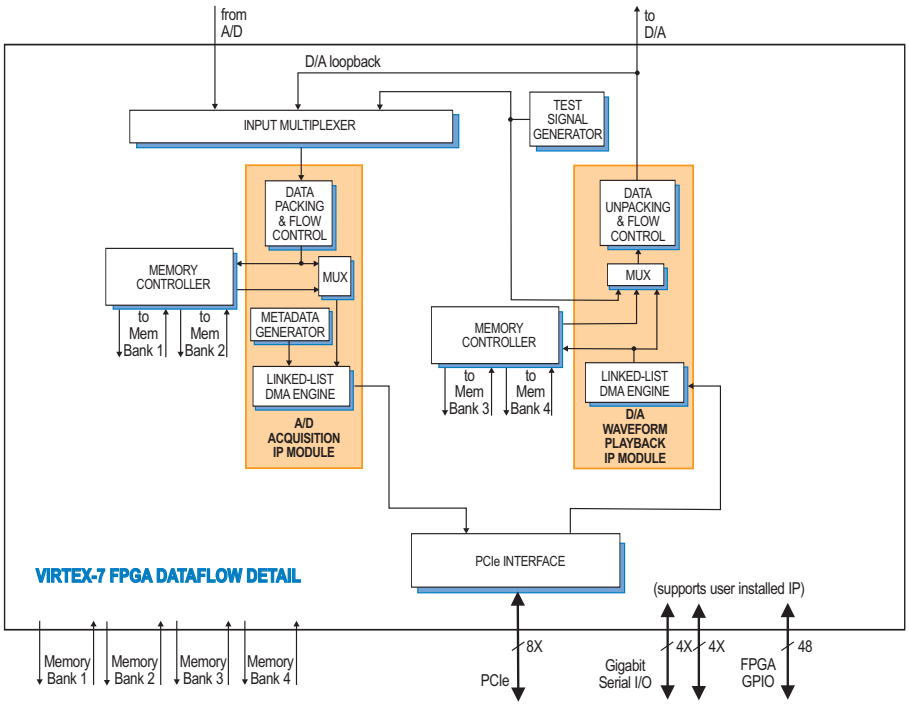
A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤



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Model 78730

1 GHz A/D and 1 GHz D/A with Virtex-7 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78730	1 GHz A/D and D/A, Virtex-7 FPGA - x8 PCIe
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 7892 and Model 9192 Cobalt Synchronizers can drive multiple 78730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 78730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

New!

Model 78741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

General Information

Model 78741 is a member of the Onyx® family of high-performance PCIe modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

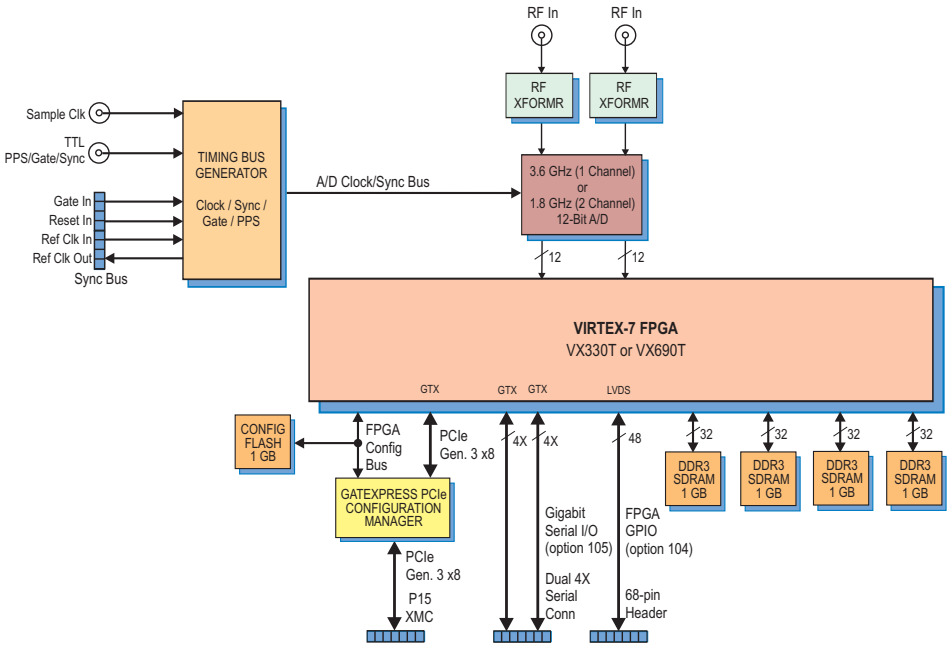
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Module

The 78741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

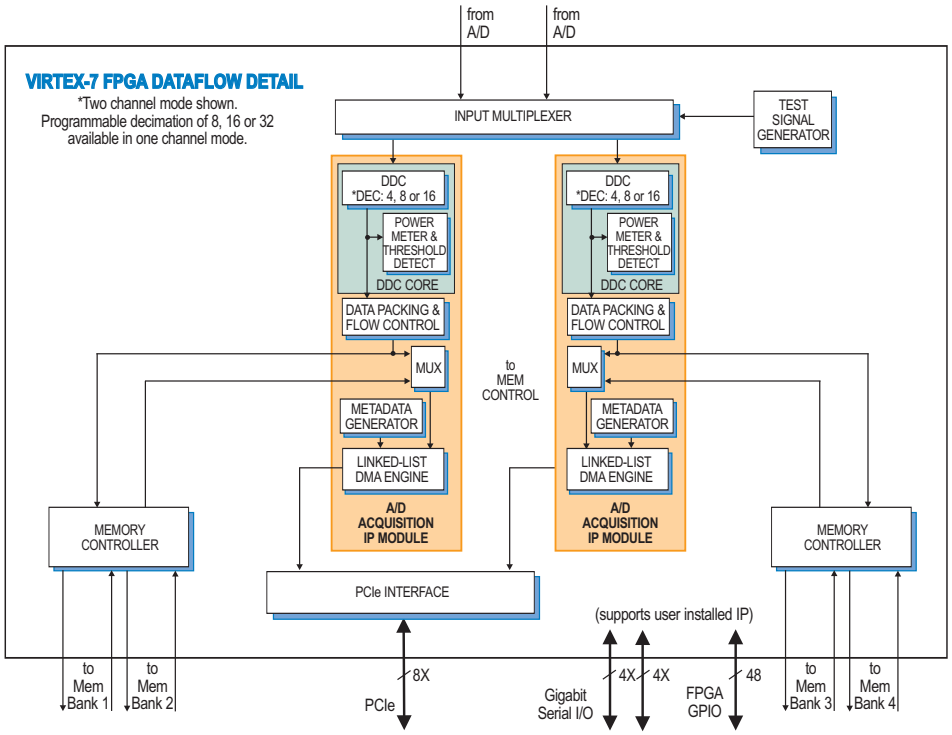
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

Memory Resources

The 78741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

PCI Express Interface

The Model 78741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board

Clocking and Synchronization

The 78741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 78741's can be synchronized with a simple cable. For larger systems, multiple 78741's can be synchronized using the Model 7892 high-speed sync board to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - x8 PCIe

Onyx

GateXpress

GateFlow

ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds

General Information

Model 78751 is a member of the Onyx® family of high performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78751 includes a general purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

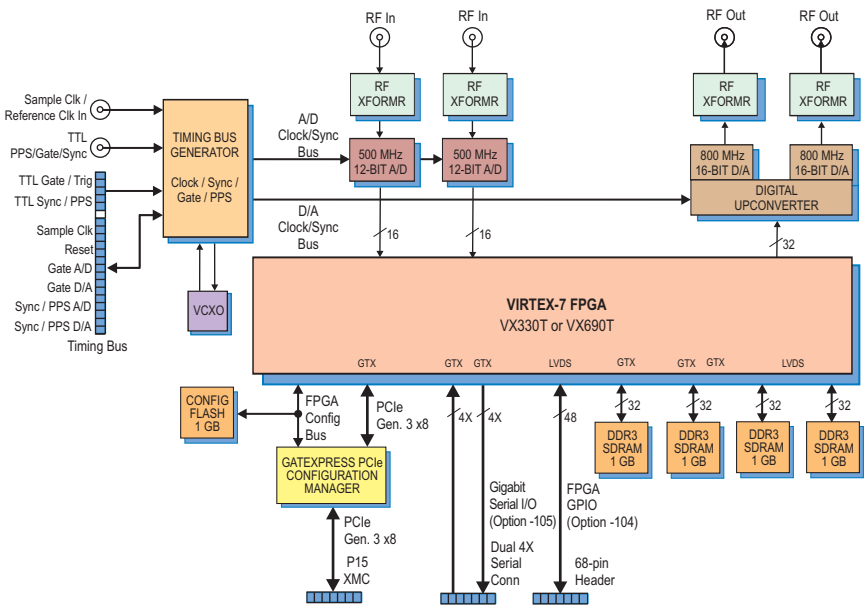
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA to two gigabit serial connectors along the top edge of the board. ➤



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Model 78751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 78751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

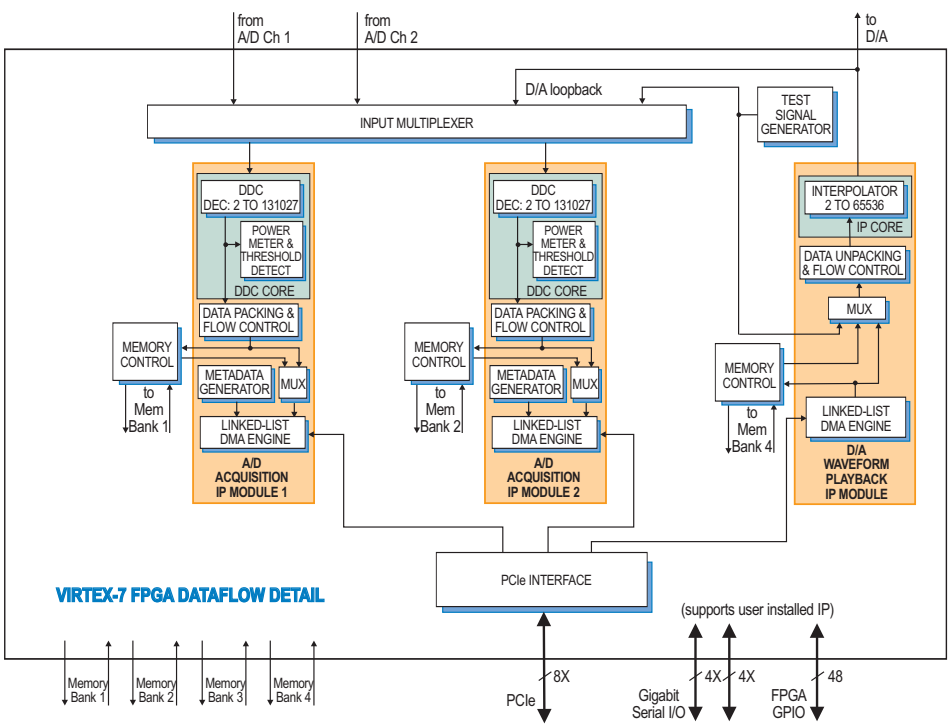
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 71751's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 71751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
71751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 78760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

General Information

Model 78760 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78760 includes optional general-purpose and gigabit-serial connectors for application-specific I/O protocols.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

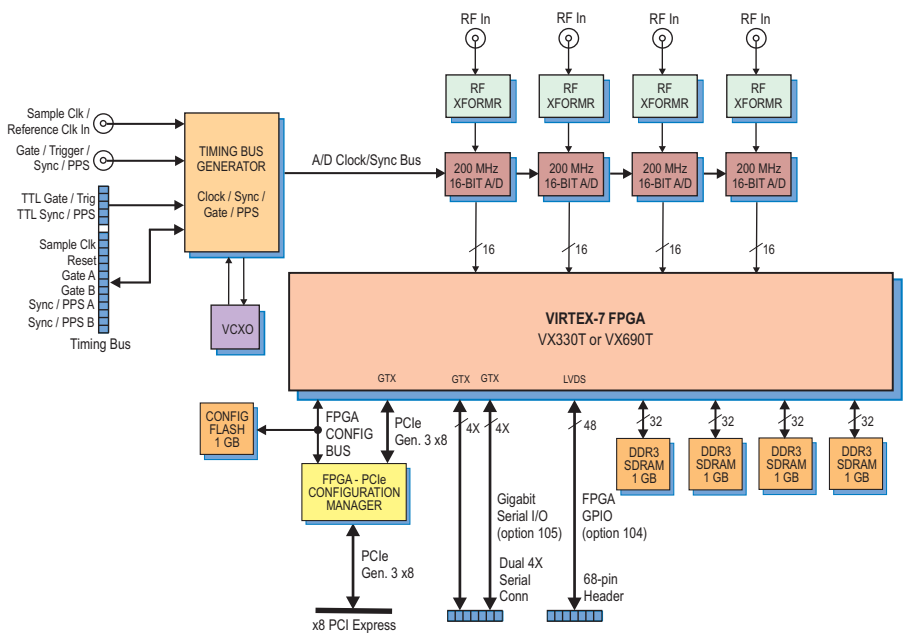
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Advanced reconfigurability features
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

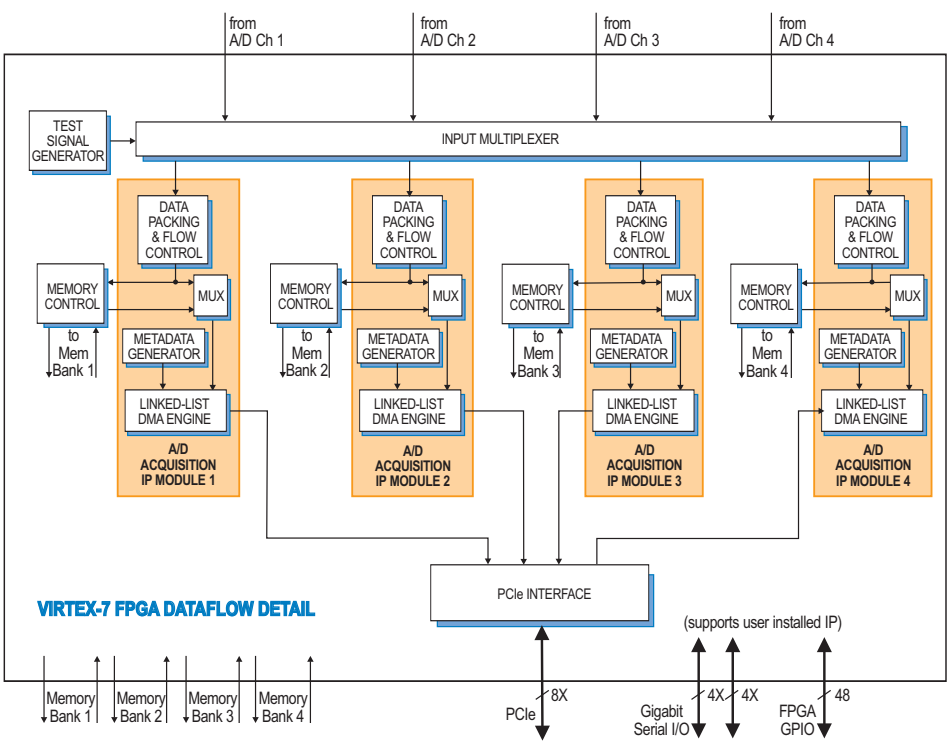
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an ➤

A/D Acquisition IP Modules

The 78760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 78760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

➤ external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78760's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8 Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78760	4-Channel 200 MHz A/D with Virtex-7 FPGA - x8 PCIe
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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New!

Model 78761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

Onyx

GateXpress

GateFlow

ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 78761 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78761 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

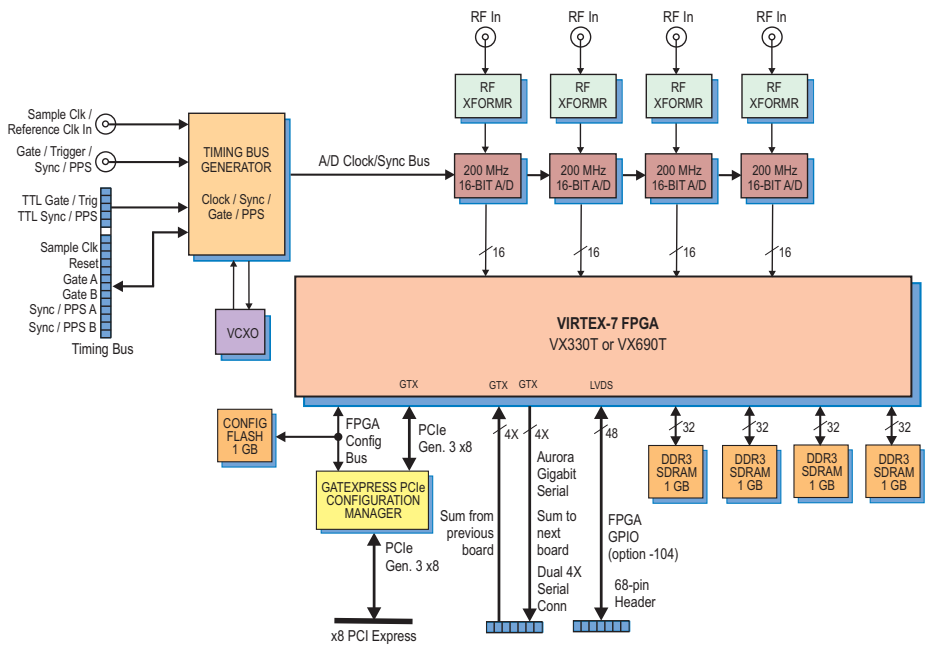
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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Model 78761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 78761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

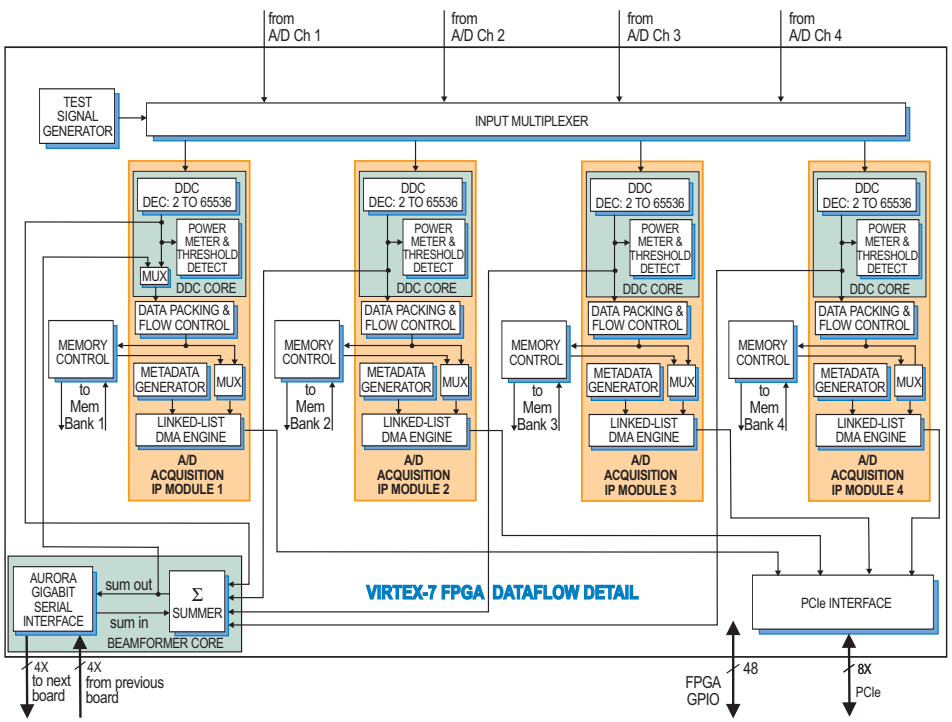
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78761's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 78761 — 4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model	Description
78761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through 68-pin ribbon cable connector

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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New!

Model 78791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - x8 PCIe

Onyx
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 78791 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78791 includes general purpose and gigabit serial connectors for application-specific I/O .

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 78791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 78791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

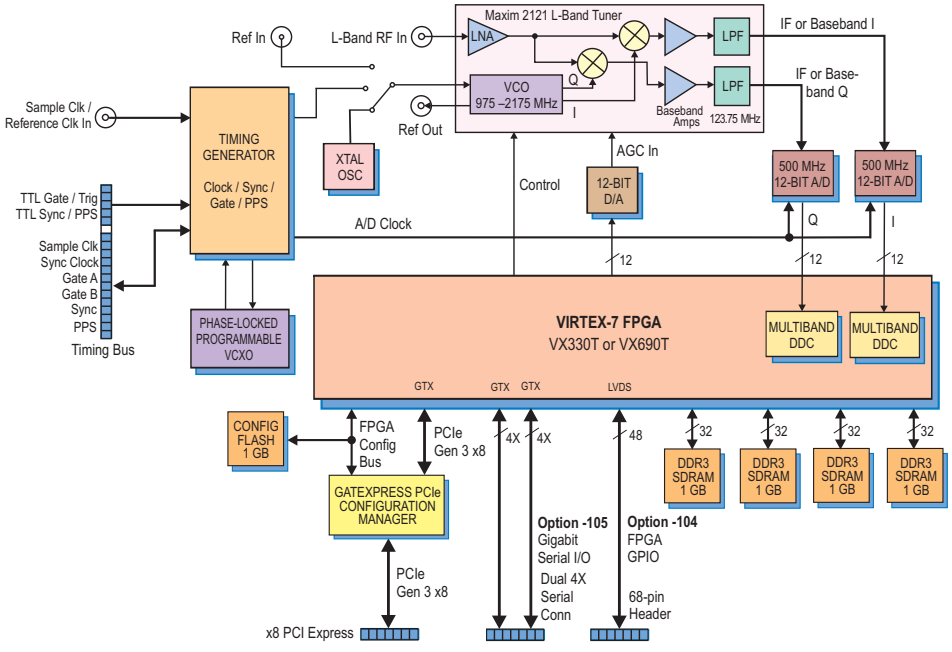
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA to two gigabit serial connectors along the top edge of the board. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

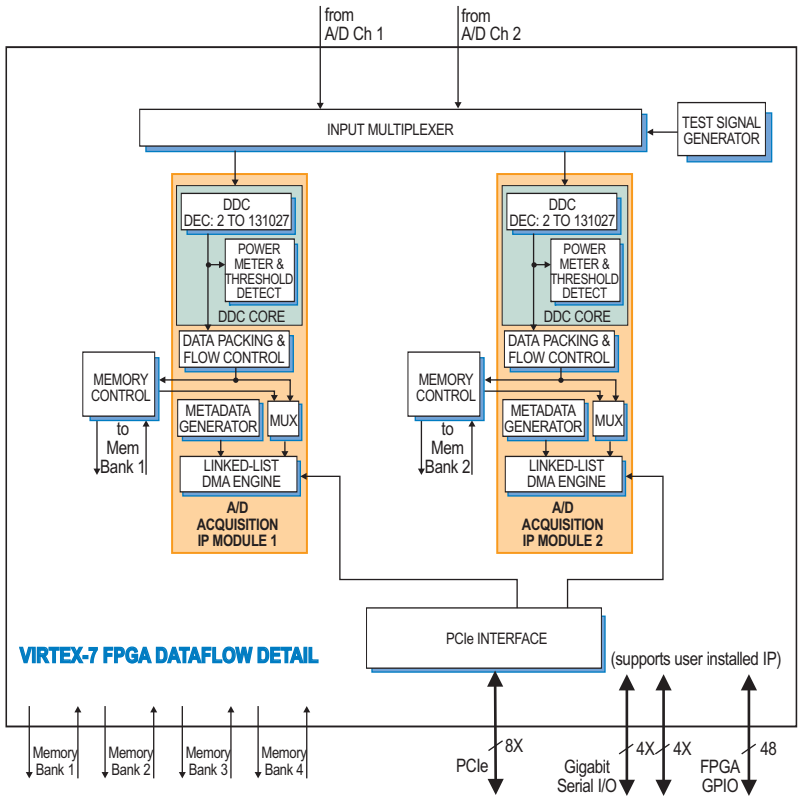
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA .

PCI Express Interface

The Model 78791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 78791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
78791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - x8 PCIe
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through 68-pin ribbon cable connector
-105	Gigabit serial FPGA I/O through two 4X top edge connectors

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** –97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** 3 dB cutoff frequency: 123.75 MHz

A/D Converters
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe

JADE

NAVIGATOR Design Suite

General Information

Model 78131 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

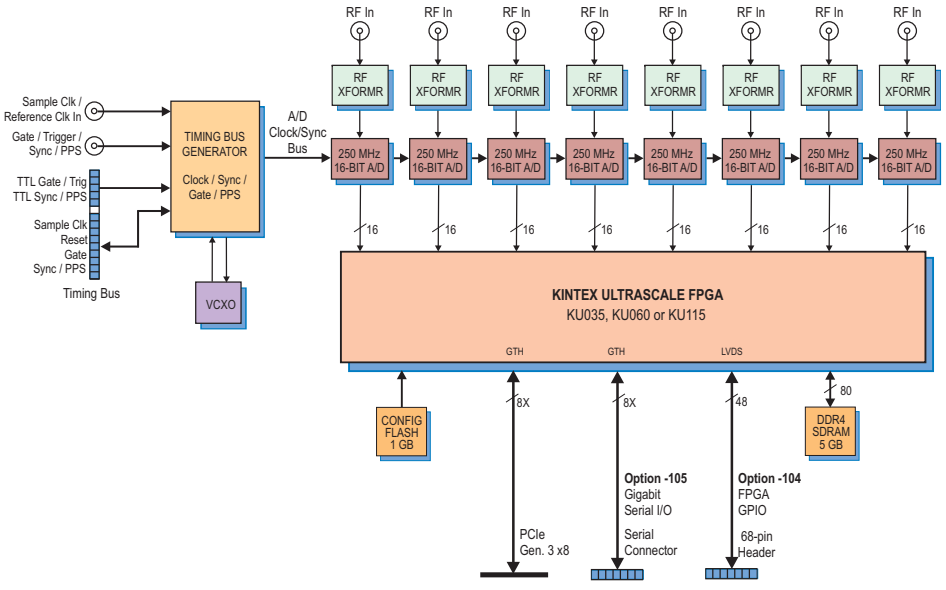
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Modules

The 78131 features eightA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to an 8X gigabit serial connector along the top edge of the PCIe board.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

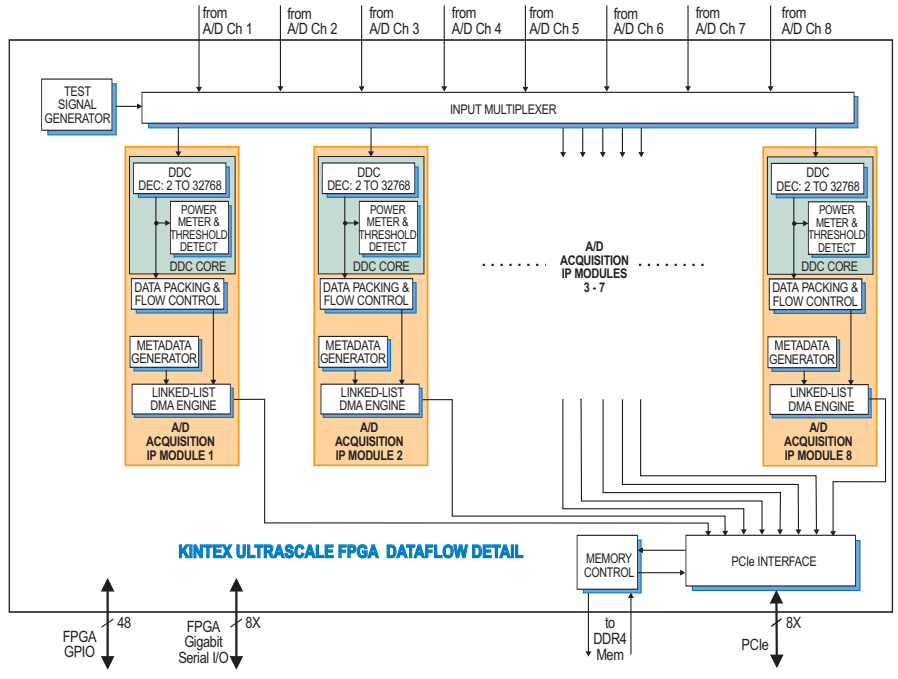
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 78131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Model 78131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
78131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 78131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105** connects one 8X gigabit serial link from the FPGA to an 8X gigabit serial connector along the top edge of the PCIe board.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - x8 PCIe

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available

General Information

Model 78132 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

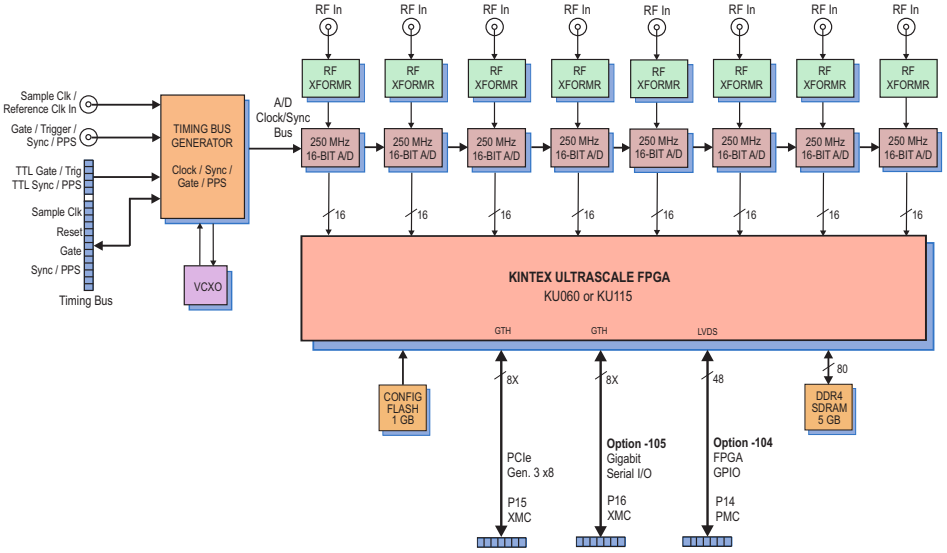
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78132 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible down-conversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with eight full duplex gigabit links to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

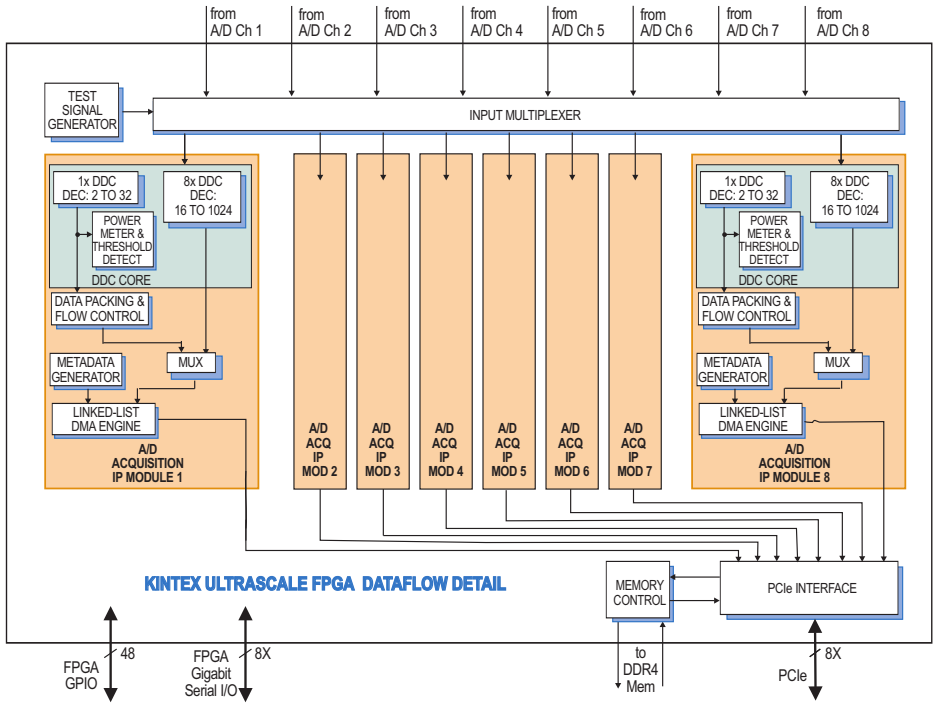
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected b oards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - x8 PCIe

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
78132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 78132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Eight banks, 8 channels per bank
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

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New

Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

JADE

NAVIGATOR Design Suite

General Information

Model 78141 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

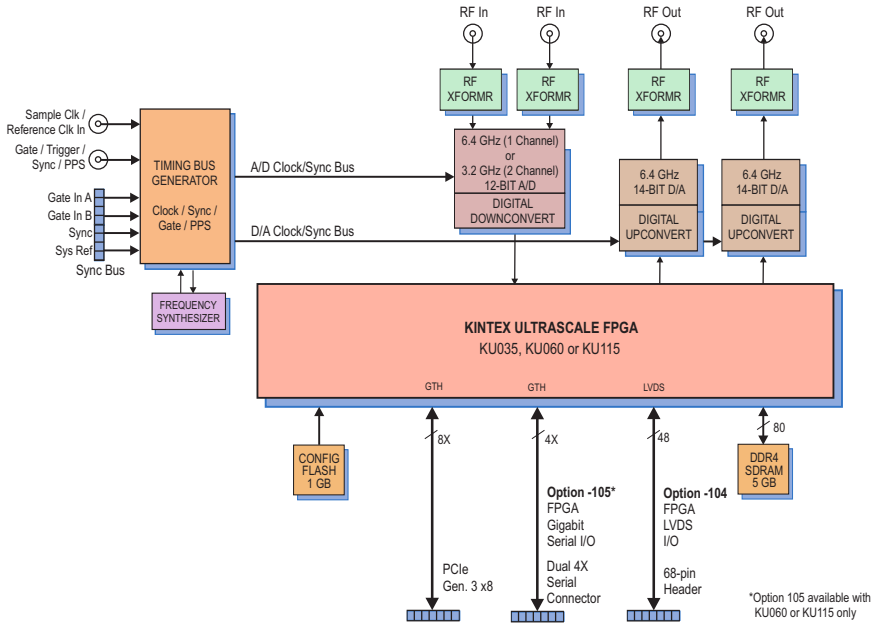
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Module

The 78141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 78141 factory installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 78141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

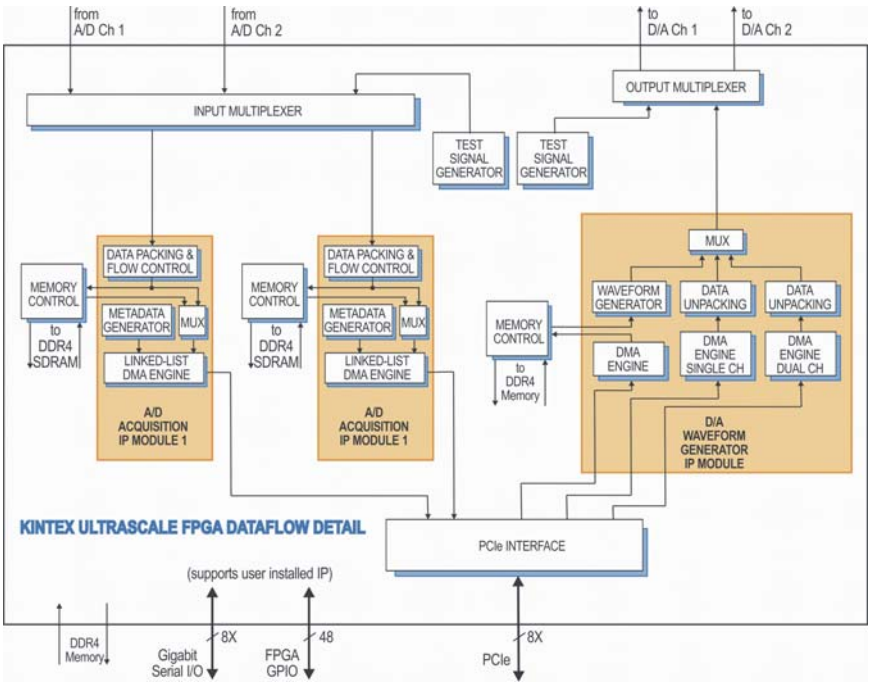
PCI Express Interface

The Model 78141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 78141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7892 high- speed sync board can be used to drive the sync bus to synchronize multichannel systems. ➤



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to support serial protocols.

Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O
- **Option -105 (only available with option -084 or -087):** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

Ordering Information

Model	Description
78141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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New!

Model 78821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available

General Information

Model 78821 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 78821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

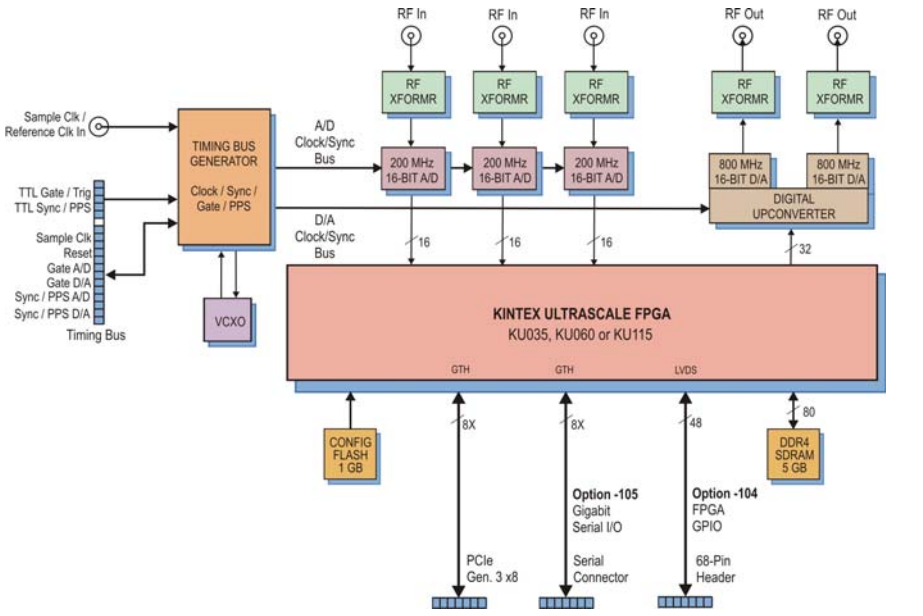
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 78821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 78821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

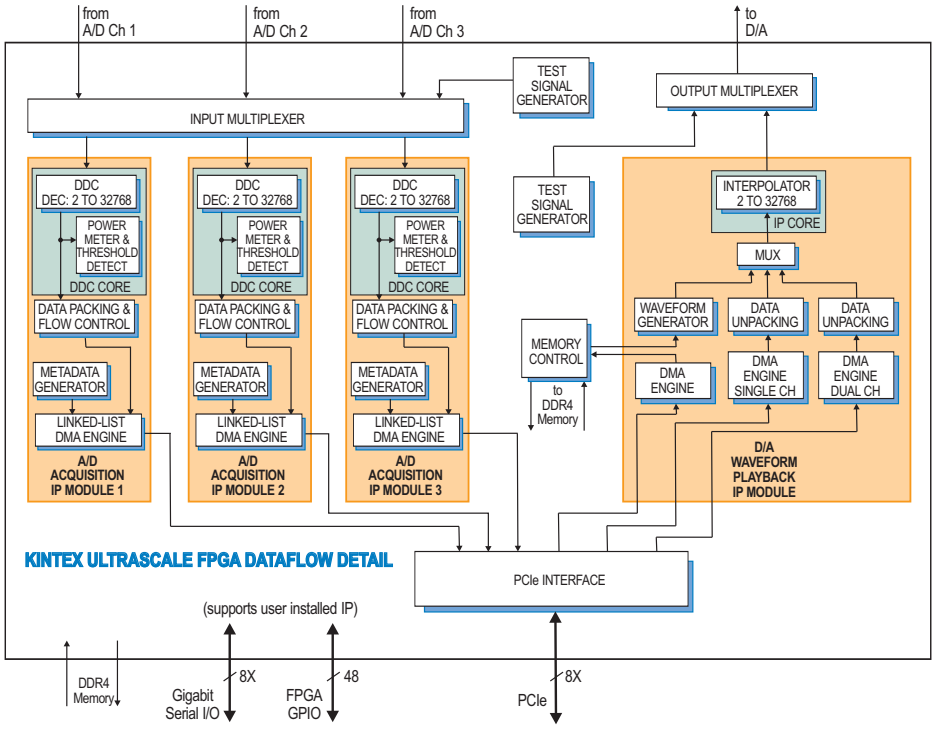
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 78821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
78821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - x8 PCIe
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged versions

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

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New!

Model 78841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - PCIe

JADE

NAVIGATOR Design Suite

General Information

Model 78841 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

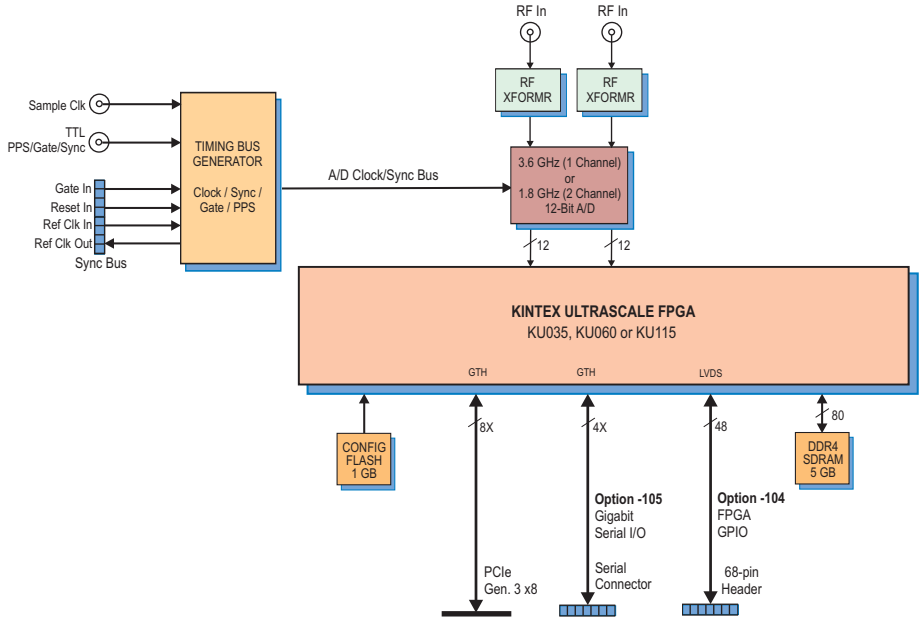
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O



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Model 78841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Module

The 78841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

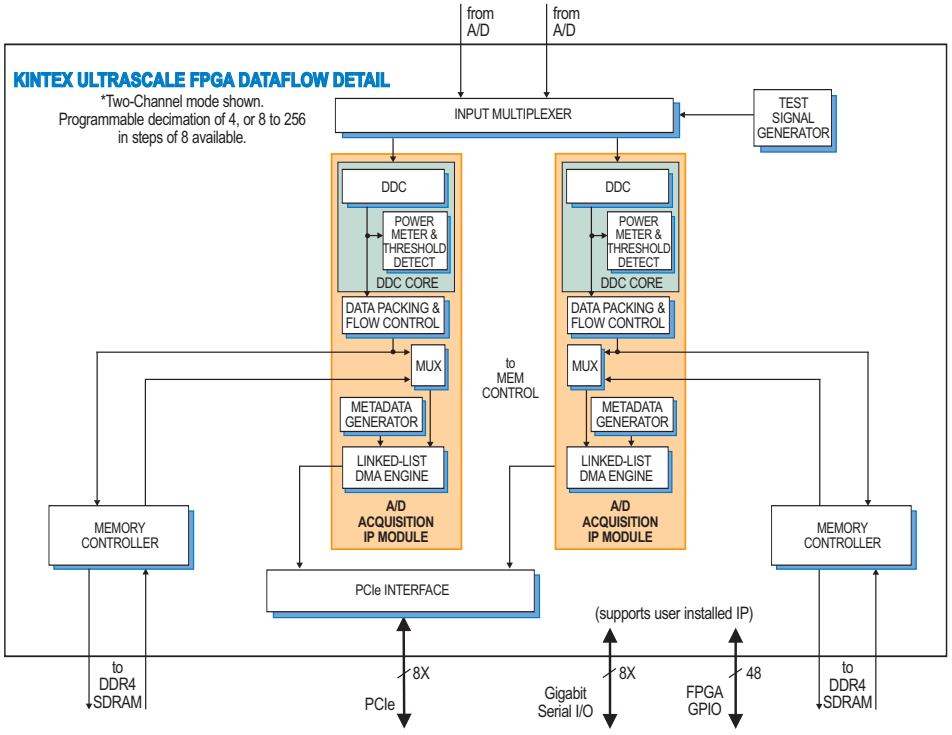
Option -105 connects one 8X gigabit serial link from the FPGA to an 8X gigabit serial connector along the top edge of the PCIe board.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources. ➤



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Model 78841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - PCIe

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
78841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - x8 PCIe
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2

➤ Memory Resources

The 78861 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 78841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 78841's can be synchronized with a simple cable. For larger systems, multiple 78841's can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input Level:** may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Single-channel mode:** decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** the DDC can be bypassed completely
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs a connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs a connector for one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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New!

Model 78851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized version available

General Information

Model 78851 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

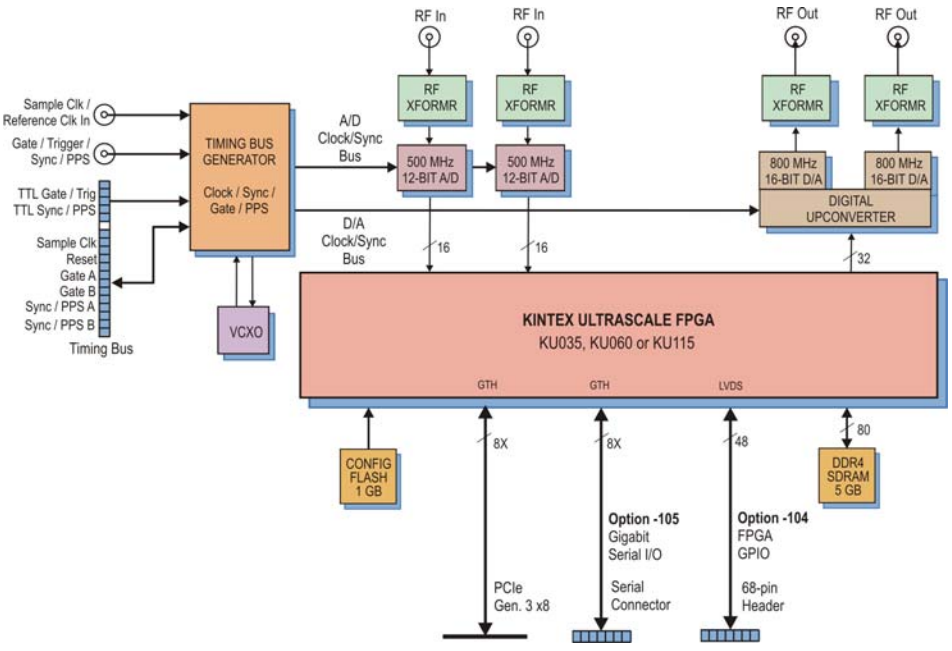
The 78851 factory-installed functions include two A/D acquisition and a waveform playback IP modules for simplifying data capture and playback, and data transfer between the board an a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 78851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Model 78851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 78851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

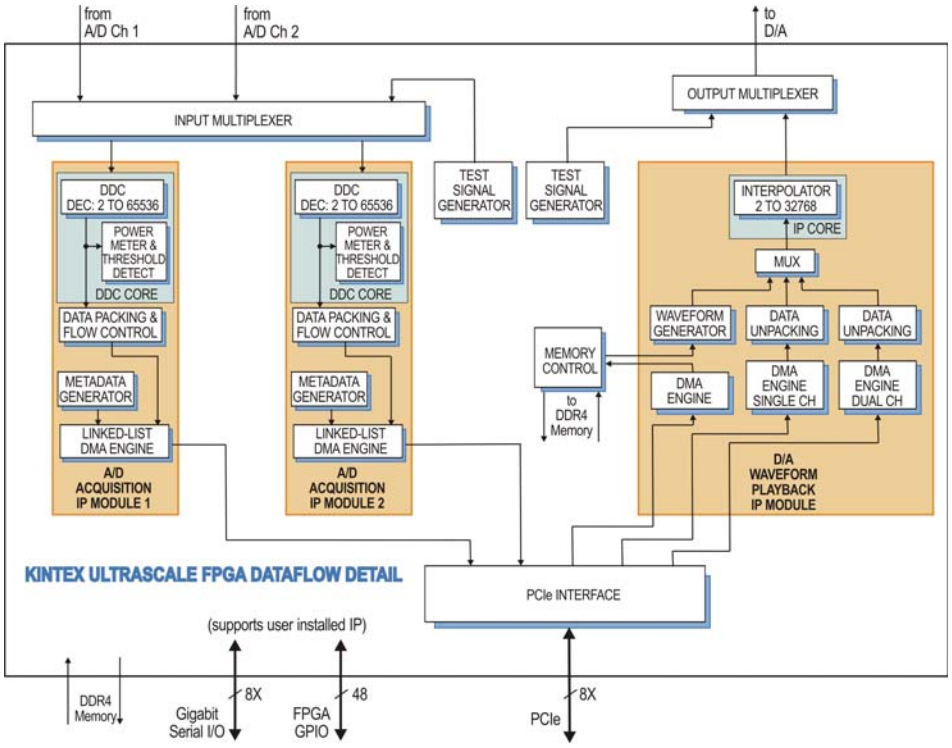
Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources. ➤



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2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 78851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
71851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - x8 PCIe
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged version

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

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New!

Model 78861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe

JADE

NAVIGATOR Design Suite

General Information

Model 78861 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

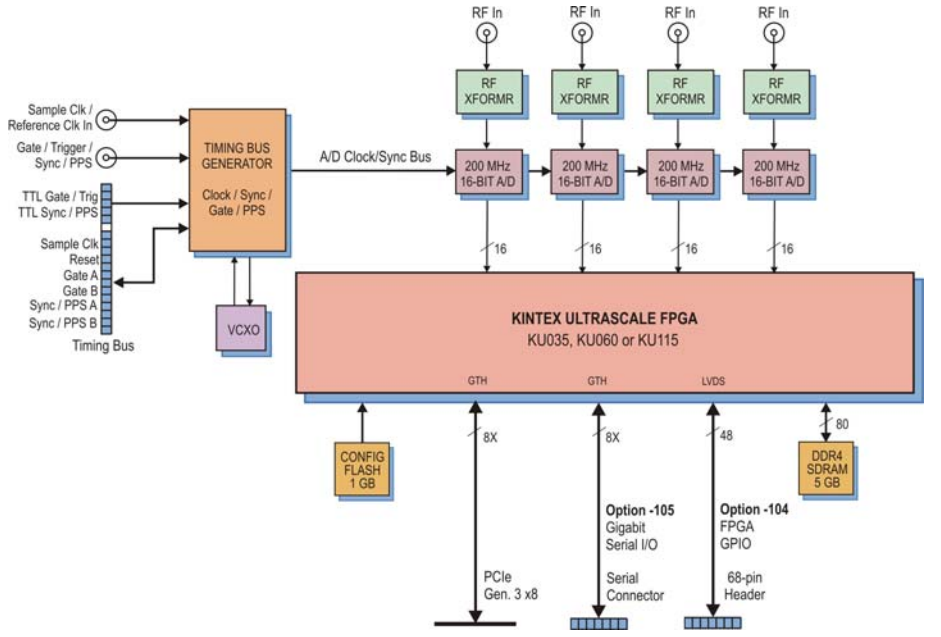
Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available



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Model 78861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe

A/D Acquisition IP Modules

The 78861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

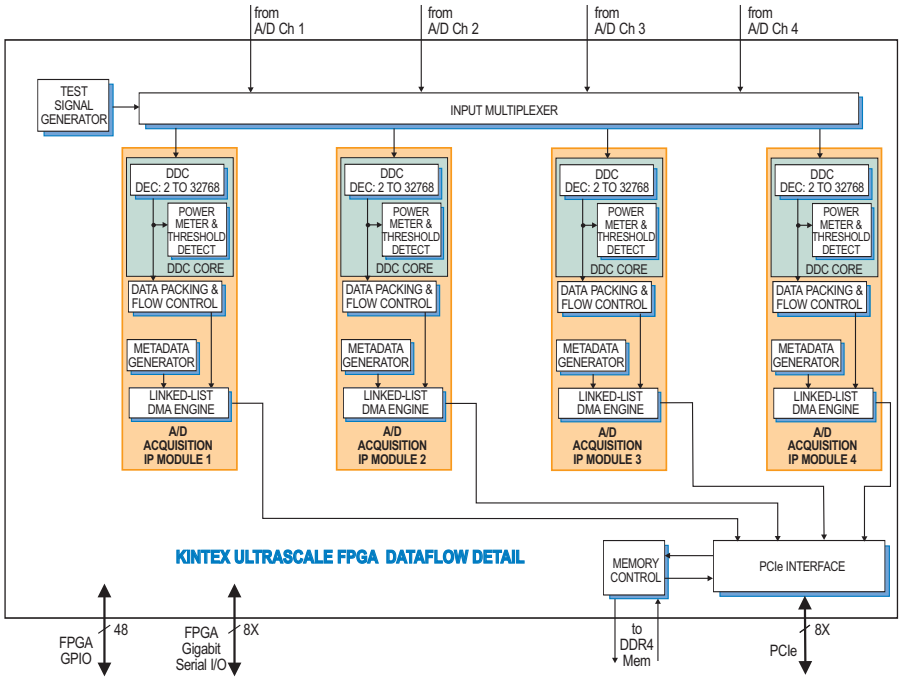
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Model 78861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
78861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through 68-pin ribbon cable connector
- 105	Gigabit serial FPGA I/O through serial connector
- 702	Air cooled, Level L2

➤ PCI Express Interface

The Model 78861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105:** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card, 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

➤

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New!

Model 78862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

JADE

NAVIGATOR Design Suite

General Information

Model 78862 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

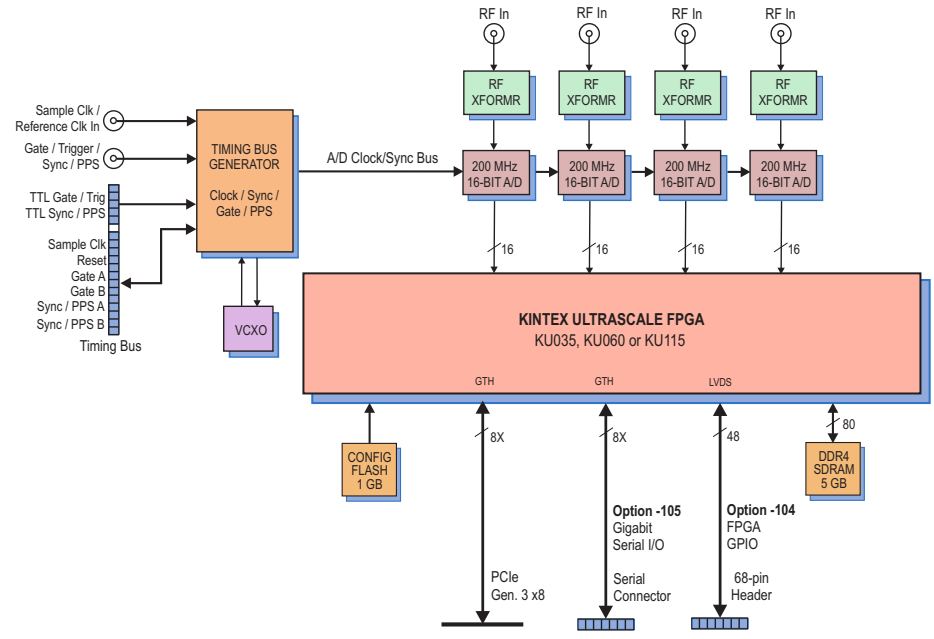
Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 78862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Modules

The 78862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

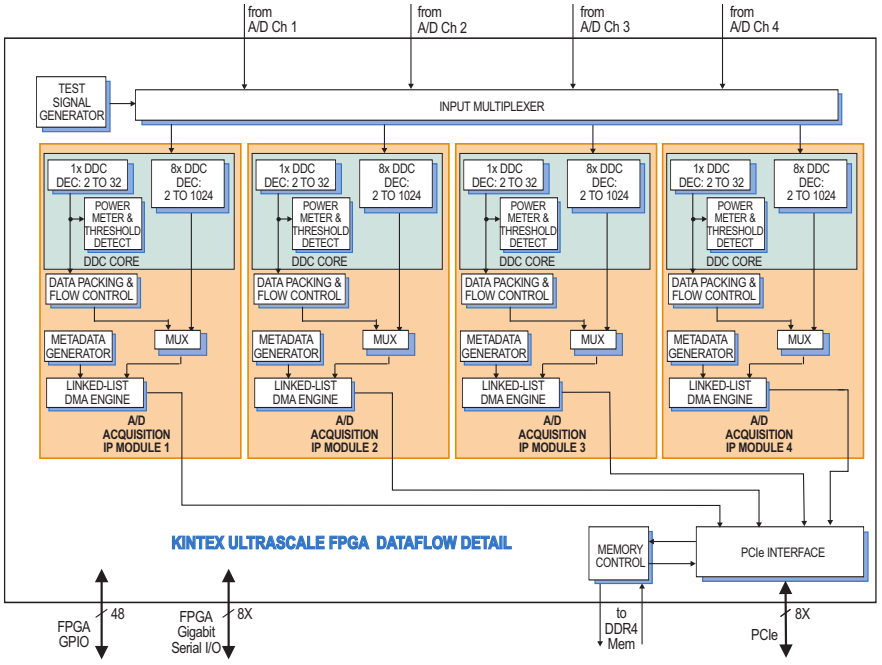
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 78862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
78862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - x8 PCIe
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through 68-pin ribbon cable connector
- 105	Gigabit serial FPGA I/O through serial connector
- 702	Air cooled, Level L2

➤ PCI Express Interface

The Model 78862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Four banks, 8 channels per bank
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105:** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card, 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 78800

Kintex UltraScale FPGA Coprocessor- x8 PCIe

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 78800 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 78800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

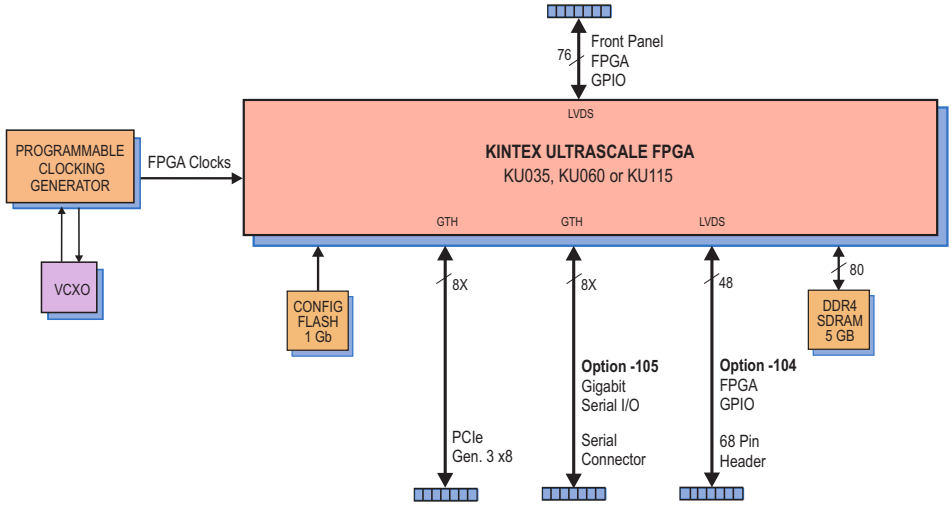
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides an 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Front Panel Digital I/O Interface

The 78800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 78800

Kintex UltraScale FPGA Coprocessor- x8 PCIe

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

➤ PCI Express Interface

The Model 78800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 78800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105** provides an 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

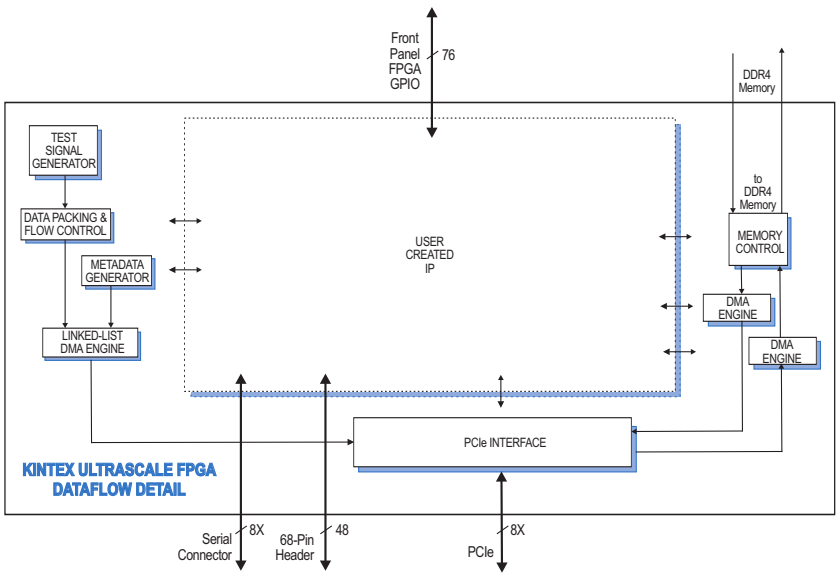
PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: PCIe card 4.375 in x 8.125 in (111.13 mm x 206.38 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



Ordering Information

Model	Description
78800	Kintex UltraScale FPGA Coprocessor - x8 PCIe
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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Model 7820

Bandit Two-Channel Analog RF Wideband Downconverter - PCIe

Bandit

ReadyFlow Board Support Package

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

General Information

The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

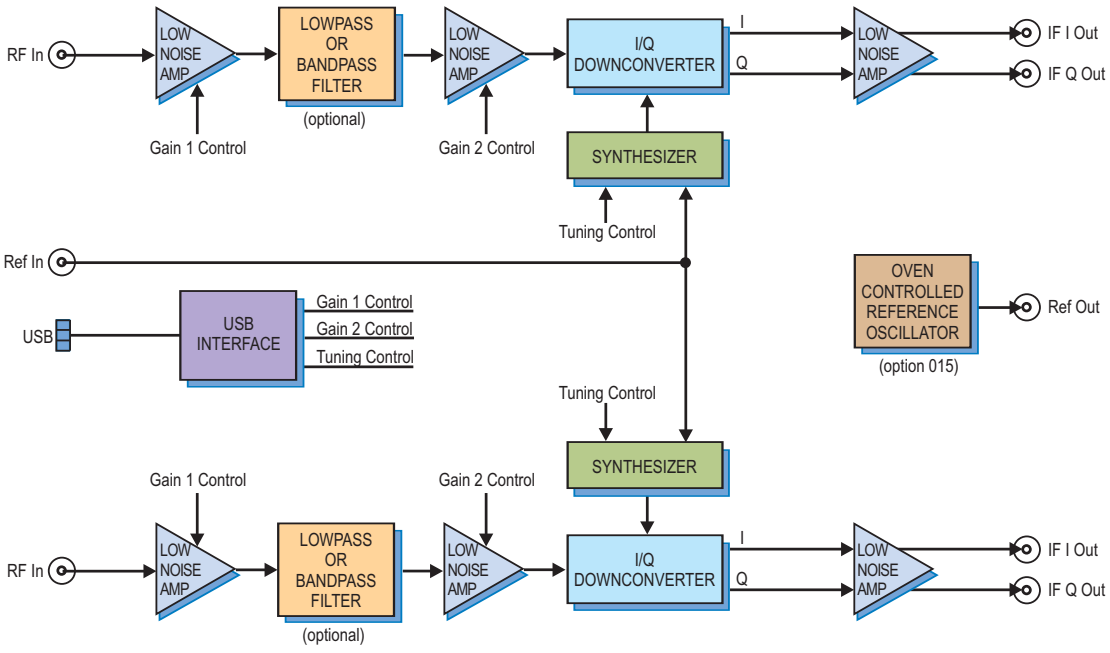
On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 7820 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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Model 7820

Bandit Two-Channel Analog RF Wideband Downconverter - PCIe

➤ Specifications

RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** –60 dBm to –20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

Phase Noise
- **1 kHz:** –90 dBc/Hz
- **100 kHz:** –110 dBc/Hz
- **1 MHz:** –130 dBc/Hz

Noise Figure (referred to input)
- **60 dB gain:** 2.6 dB

Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedence:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

Reference Output Signal
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm
- **Aging**
  - **Daily:** ±10 ppb/day
  - **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm
- **Phase Noise**
  - **1 Hz Offset:** –67 dBc/Hz
  - **10 Hz Offset:** –100 dBc/Hz
  - **100 Hz Offset:** –130 dBc/Hz
  - **1 KHz Offset:** –148 dBc/Hz
  - **10 KHz Offset:** –154 dBc/Hz
  - **100 KHz Offset:** –155 dBc/Hz

IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

PCI-Express Interface
- **PCI Express Bus:** x4 or x8, power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model	Description
7820	Bandit Two-Channel Analog RF Wideband Downconverter - PCIe

Option	Description
-015	Oven Controlled Reference Oscillator
-145	1.45 GHz lowpass input filter
-280	2.80 GHz lowpass input filter

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Model 8266

PC Development System for PCIe Cobalt, Onyx and Flexor Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 4U 19-inch rackmount PC server chassis, 21-inch deep
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box test examples

General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx® and Flexor™ PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

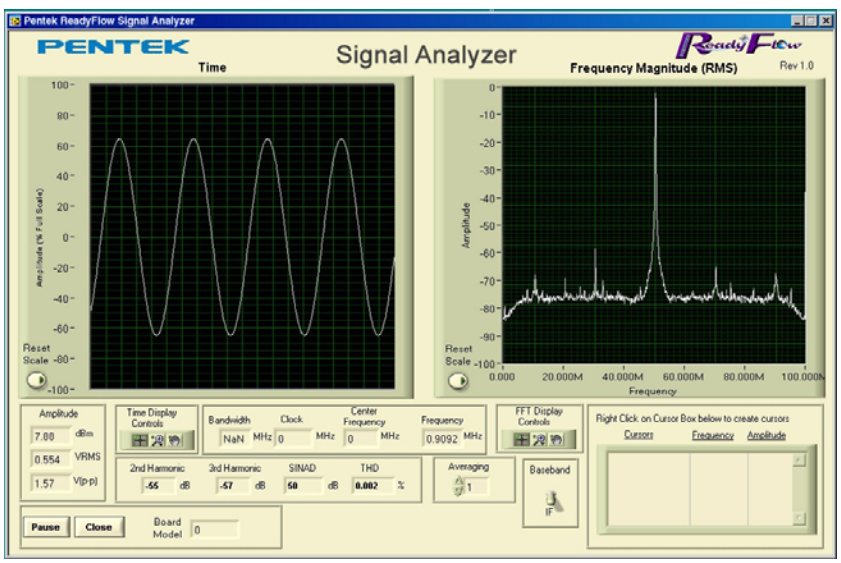
Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19" W x 21" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



Ordering Information

Model	Description
8266	PC Development System for PCIe Cobalt, Onyx and Flexor Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.

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RADAR & SDR I/O - 3U VPX - FORMAT 1

MODEL	DESCRIPTION
5308	Front Panel x8 PCI Express Adapter - 3U VPX
Cobalt 53620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX
Cobalt 53621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, 3U VPX
Cobalt 53624	Dual-Channel, 34-Signal Adaptive IF Relay - 3U VPX
Cobalt 53630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Cobalt 53640	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX
Cobalt 53641	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 3U VPX
Cobalt 53650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Cobalt 53651	2-Chan 500 MHz A/D with DDC, DUC with 2-Chan 800 MHz D/A, Virtex-6 FPGA - 3U VPX
Cobalt 53660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX
Cobalt 53661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
Cobalt 53662	4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - 3U VPX
Cobalt 53663	1100-Channel GSM Channelizer with Quad A/D - 3U VPX
Cobalt 53664	4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 3U VPX
Cobalt 53670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX
Cobalt 53671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX
Cobalt 53690	L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX
Onyx 53720	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 53721	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 53730	1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX
Onyx 53741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC,Virtex-7 FPGA - 3U VPX
Onyx 53751	2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 53760	4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 3U VPX
Onyx 53761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 3U VPX
Onyx 53791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 3U VPX
Jade 53131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Jade 53132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX
Jade 53141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - 3U VPX
Jade 53821	3-Channel 200 MHz A/D, DDC, DUC 2_Channel 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX
Jade 53841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - 3U VPX
Jade 53851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX
Jade 53861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - 3U VPX
Jade 53862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - 3U VPX
Jade 53800	Kintex UltraScale FPGA Coprocessor - 3U VPX Format 1
8267	3U VPX Development System for Cobalt, Onyx, Flexor, and Jade boards
	Customer Information

RADAR & SDR I/O - PMC/XMC

Click Here for the PRODUCT SELECTOR

RADAR & SDR I/O - CompactPCI

RADAR & SDR I/O - x8 PCI Express

RADAR & SDR I/O - AMC

RADAR & SDR I/O - 3U VPX - FORMAT 2

RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated March 2018

New!

Model 53800

Kintex UltraScale FPGA Coprocessor- 3U VPX

Model 5380 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex Ultra-Scale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 53800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 53800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

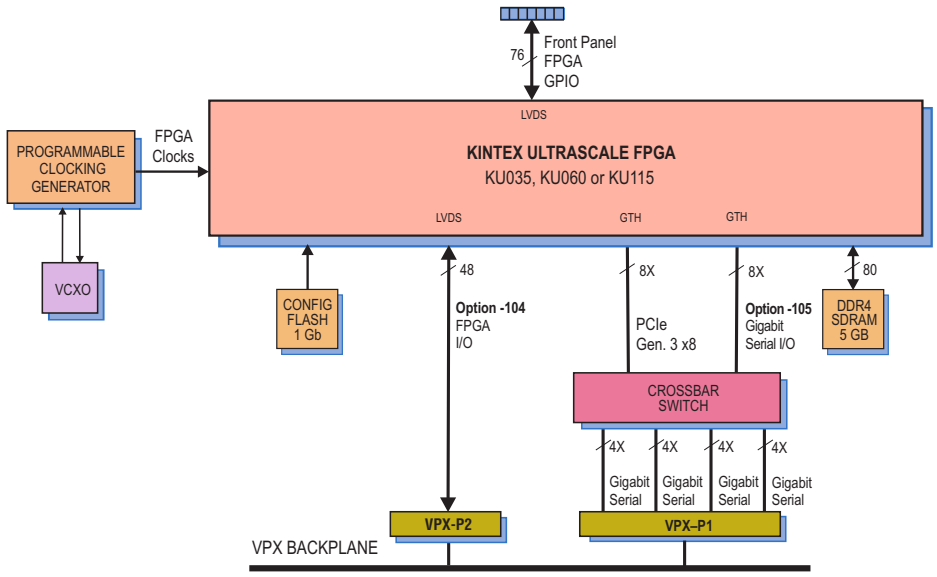
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Front Panel Digital I/O Interface

The 53800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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New!

Model 53800

Kintex UltraScale FPGA Coprocessor- 3U VPX

➤ Interfaces and Memory

The Model 53800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The 53800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Crossbar Switch

The 53800 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable input equalization and output pre-emphasis settings enable optimization.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

SPARK Development Systems

Ordering Information

Model	Description
53800	Kintex UltraScale FPGA Coprocessor - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity in all options:** 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

VPX Families

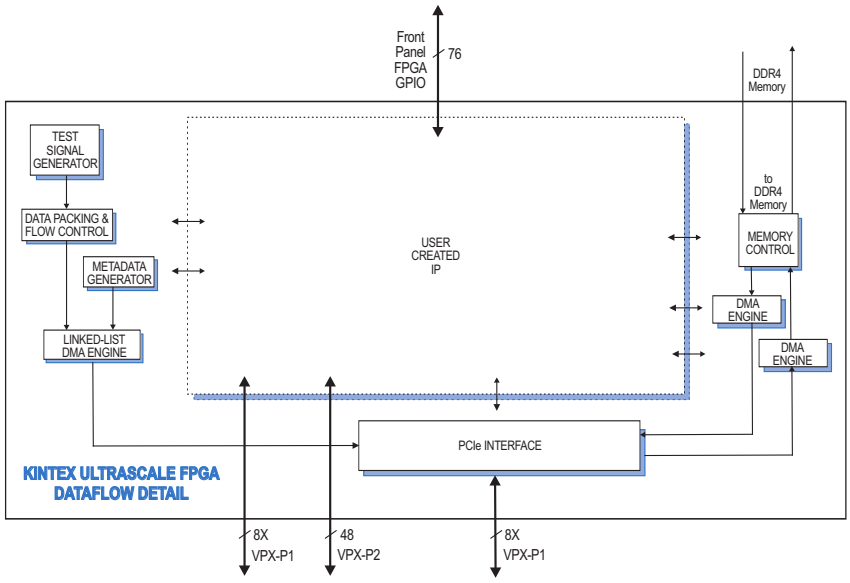
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 5308

Front Panel x8 PCI Express Adapter - 3U VPX

Features

- Front Panel x8 PCI Express connection to host PC
- 3U VPX form factor provides a compact, rugged platform
- Cascade mode provides connection to an addtional VPX system
- Compatible with several VITA standards including:
  VITA-46 (VPX Baseline Standard)
  VITA-48 (VPX REDI)
  VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Ordering Information

Model	Description
5308	Front Panel x8 PCI Express Adadpter - 3U VPX

Options:

-001	Host Adapter Mode (for connection to external host computer)
-002	Cascade Mode (for connection to additional VPX system)
-703	Level L3 Conduction-Cooled Version

Accessories:

Model	Description
4235	PCI Express x8 Host Card for PC
2180	PCI Express x8 Cable

General Information

Model 5308 is a front panel PCI Express adapter for 3U VPX systems. It provides a convenient interface from a 3U VPX system to an external host computer, to simplify development.

The 5308 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration allows selection of the desired VPX-P1 port.

Front Panel Connection

The 5308 provides a front panel interface to the 3U VPX system for connection to a host computer. It supports x4 or x8 PCIe protocol in compliance with PCI-SIG PCI Express® External Cabling 1.0 Specification. It can also be used to connect to an additional VPX system when ordered with Cascade Mode (option -002).

Model 5308 contains built-in PCI Express ReDriver™ circuitry. This circuitry provides signal conditioning that allows the user to correct for signal loss or data errors due to cable length.

PC Connection

The most common use for Model 5308 is for connection to an external host computer. In order to make this connection, the PC requires a PCIe host adapter which is also compliant to PCI-SIG PCI Express External Cabling 1.0 Specification. Adapters supporting either PCIe x8 Gen. 1 or Gen. 2 are available from Pentek under Model 4235.

Fabric-Transparent Crossbar Switch

Two ports from the front panel PCI Express connector are attached to a Fabric-Transparent Crossbar switch. This switch bridges numerous interfaces on the board using gigabit serial data paths with no latency. This allows the user to select the desired port on VPX-P1.

Data paths can be selected as single (x1) lanes, or groups of four lanes (x4). Programmable signal input equalization and output pre-emphasis settings enable optimization. A USB interface is provided for switch programming, and 4 MB onboard FLASH memory allows storage of up to 16 user configurations. Several useful configurations are pre-installed at the factory.

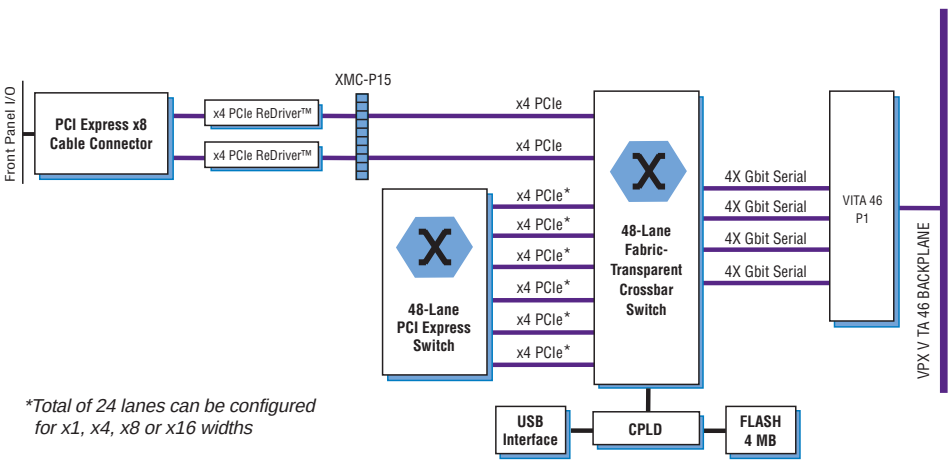
PCI Express Switch

The 5308 includes a multiport PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the fabric-transparent crossbar switch. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Data to or from the panel cable can be selected as x4 or x8 width. Both PCIe Gen. 1 and Gen. 2 are supported.

3U VPX Interface

The 5308 provides full-duplex links to the VPX P1 connector, each capable of peak rates up to 1 gigabyte per sec. Four sets of x4 links support PCI Express.



*Total of 24 lanes can be configured for x1, x4, x8 or x16 widths

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

Model 53620 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53620 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53620 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

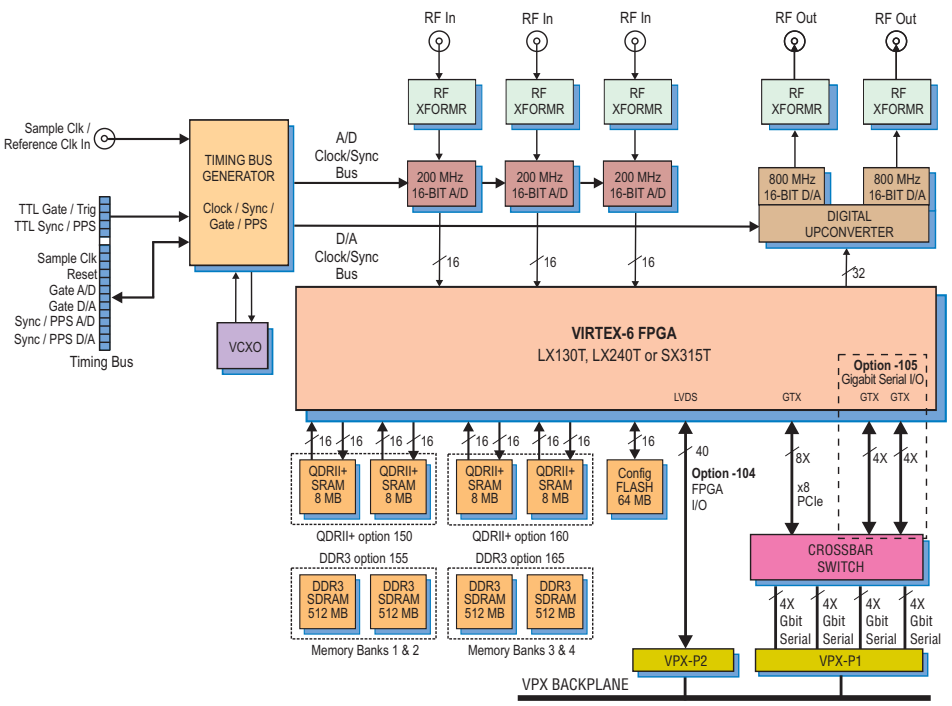
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

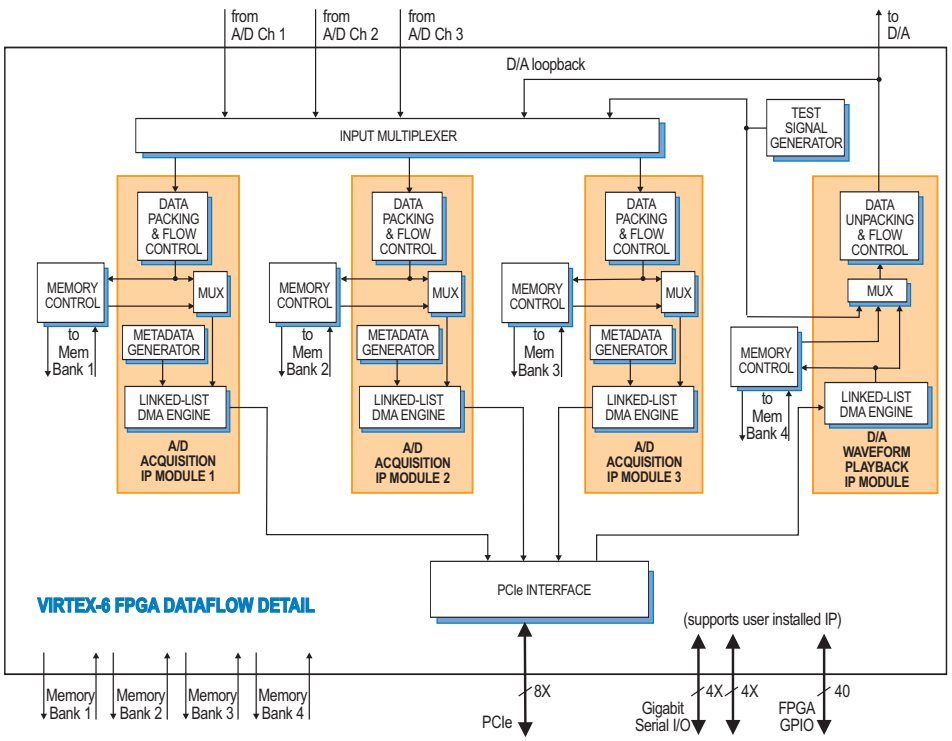
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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www.pentek.com

Model 53620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
53620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53620 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 53621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 53621 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Optional LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53621 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

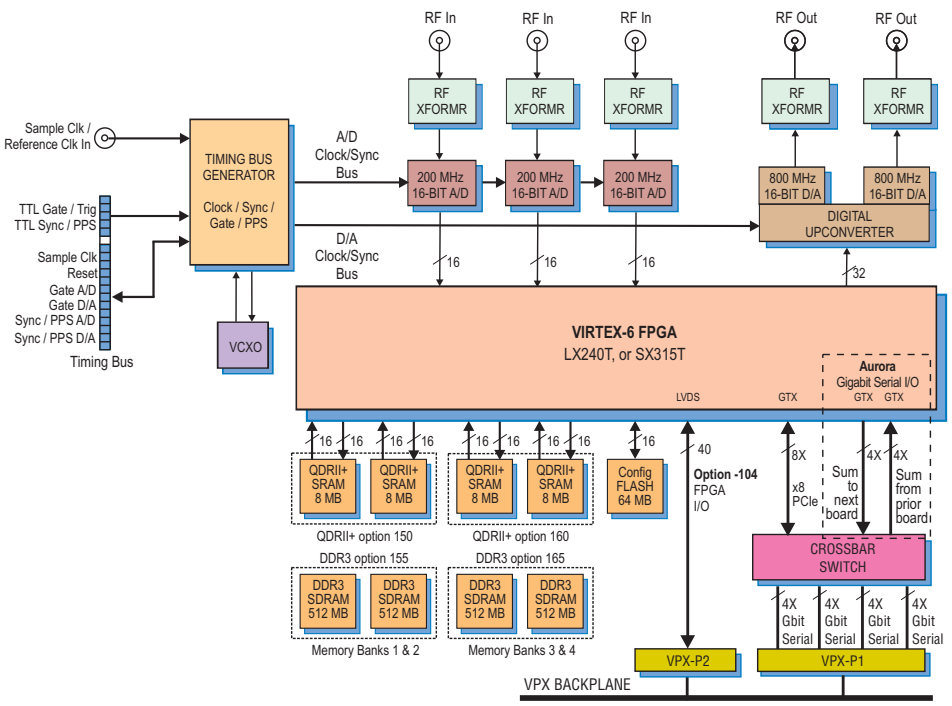
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

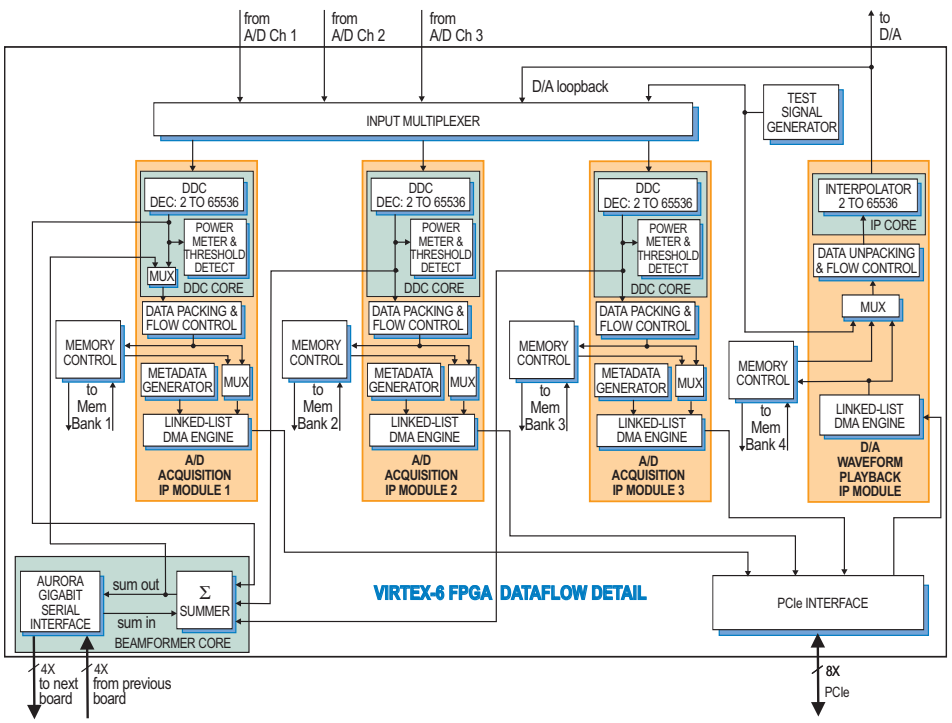
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to crate a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53621 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

Model 53621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Model 53624

Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

Model 53624 COTS (left) and rugged version

Features

- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/As
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

General Information

Model 53624 is a member of the Cobalt® family of high-performance 3U OpenVPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 53624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 53624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

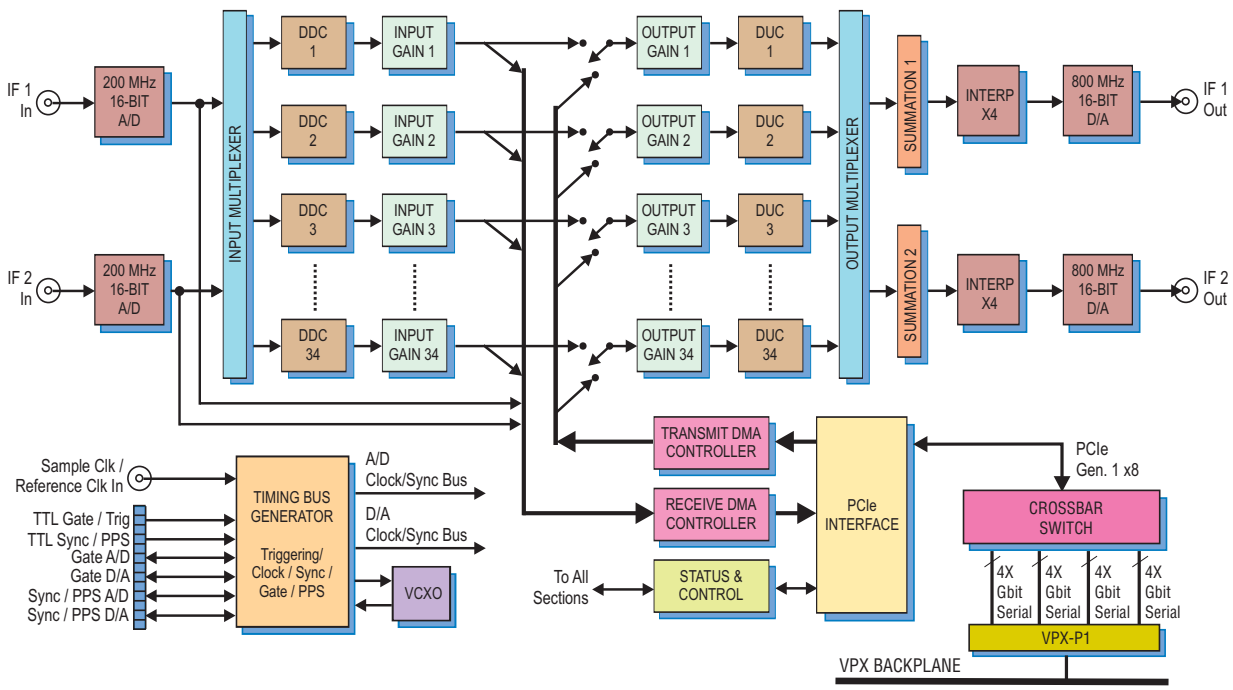
Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 53624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two summation blocks, ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ each associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 53624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 53624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 53624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz. ➤

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53624's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

The Model 53624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53624 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Quantity: Two
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

Model 53624 — Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53624	Dual-Channel 34-Signal Adaptive IF Relay - 3U OpenVPX

Options:

-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	Development System See 8267 Datasheet for Options

Digital Downconverters
Quantity: 34
Decimation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >100 dB
Phase Offset: 1 bit, 0 or 180 degrees
FIR Filter: 18-bit coefficients
Output: Complex, 16-bit I + 16-bit Q
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
Quantity: 34
Data: Complex, 16-bit I + 16-bit Q
Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
Quantity: 34
Data: Complex, 16-bit I + 16-bit Q
Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
Quantity: 34
Interpolation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
FIR Filter: 18-bit coefficients, 16-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Analog Output Channels: 2
Type: Texas Instruments DAC5688
Input Data Rate: 200 MHz max.
Output Signal: Real
Output Sampling Rate: 800 MHz max. with 4x interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Required: Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8;

Environmental
Standard:
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Option 702 L2 Extended Temp (air-cooled):
Operating Temp: -20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-cond.
Option 712 L2 Extended Temp (conduction-cooled):
Operating Temp: -20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U VPX board, 100 x 160 mm (3.937 x 6.299 in.)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

Model 53630 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53630 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

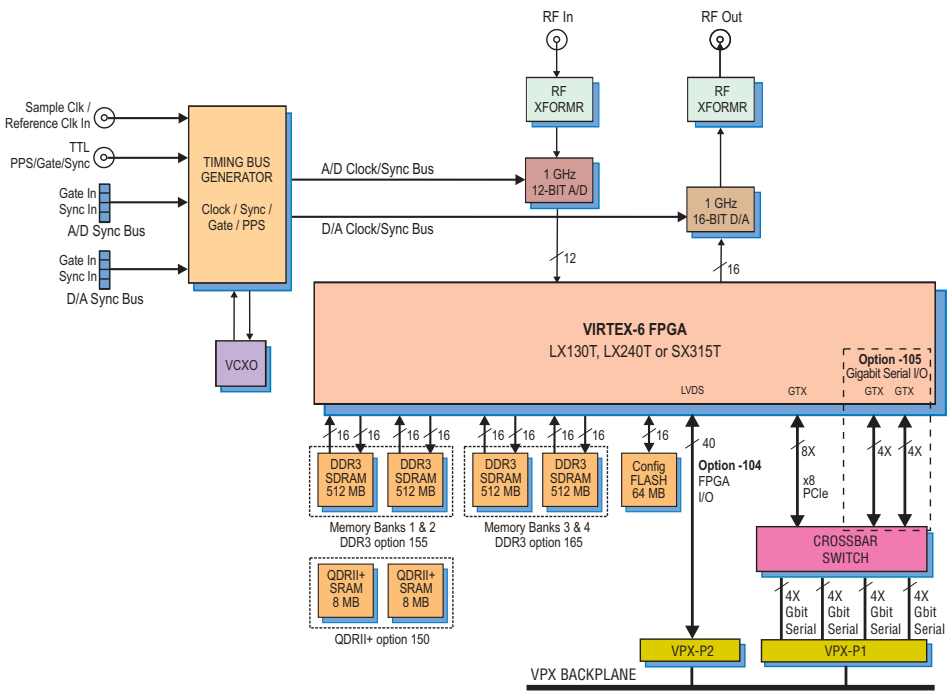
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Module

The 53630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

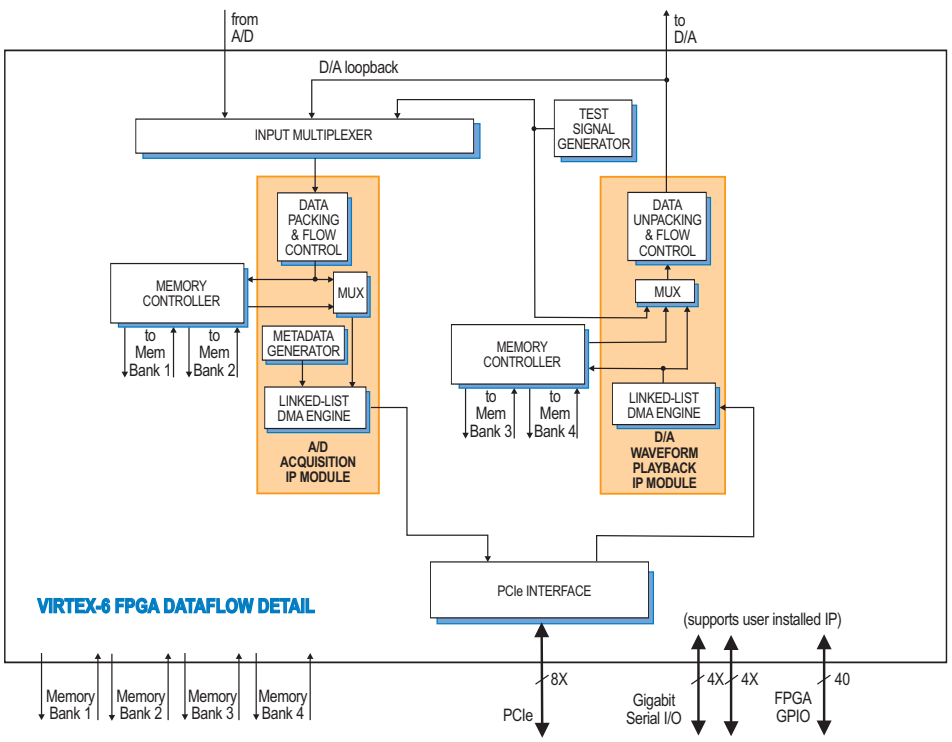
A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 5392 and Model 9192 Cobalt Synchronizers can drive multiple 53630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 53630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

PCI Express Interface

The Model 53630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53630 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen.1: x4 or x8; Gen 2: x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

Model 53640 COTS (left) and rugged version

General Information

Model 53640 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

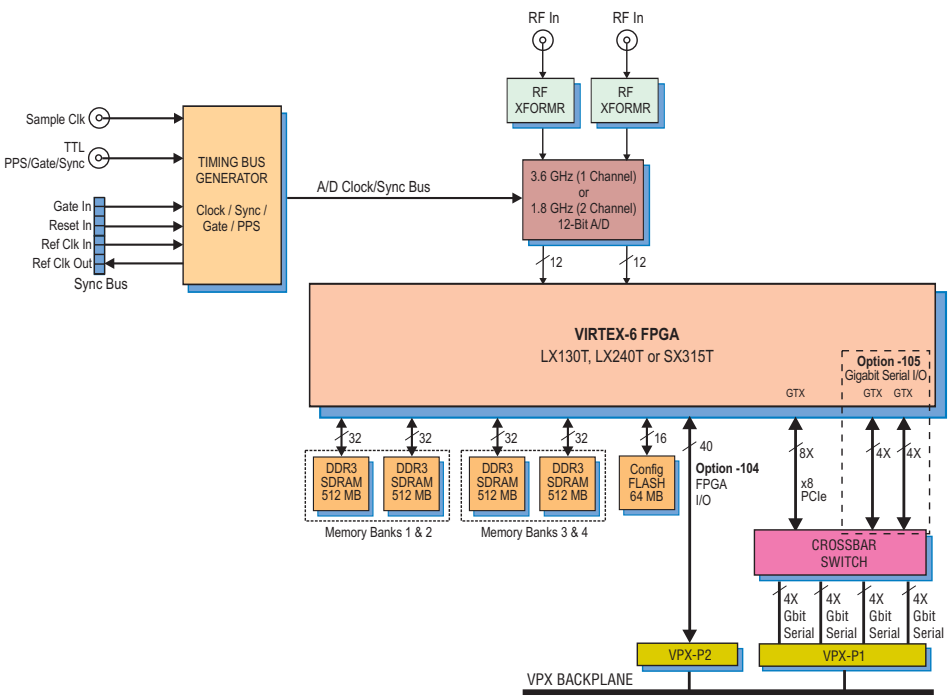
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 53640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 53640's can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 53640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

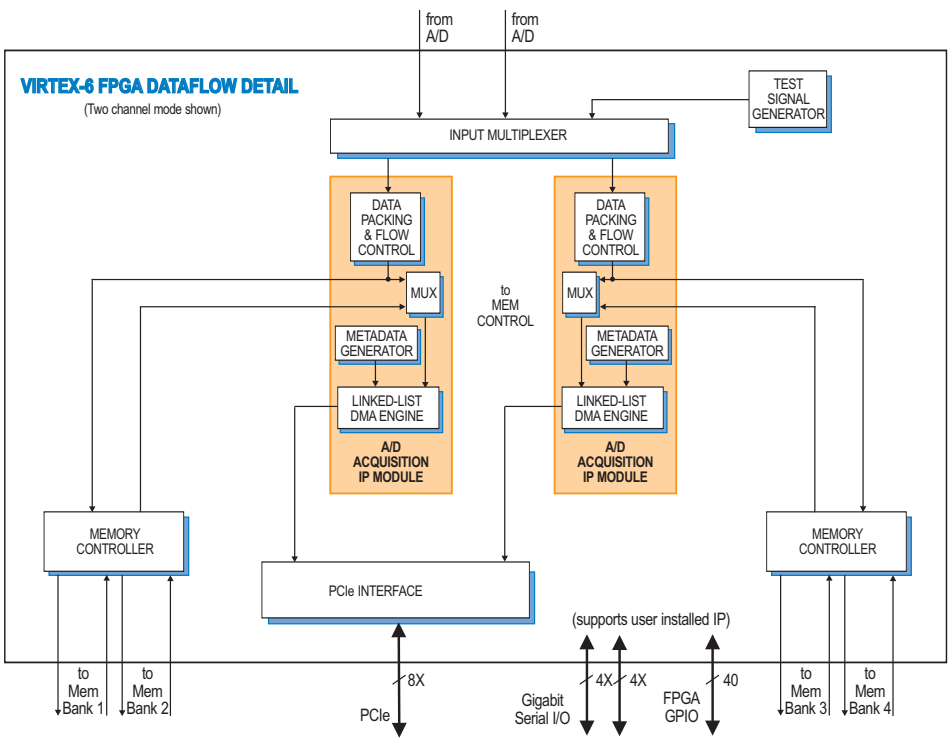
The Model 53640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Module

The 53640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Fabric-Transparent Crossbar Switch

The 53640 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1or Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Model 53641 COTS (left) and rugged version

General Information

Model 53641 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53641 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

A/D Converter Stage

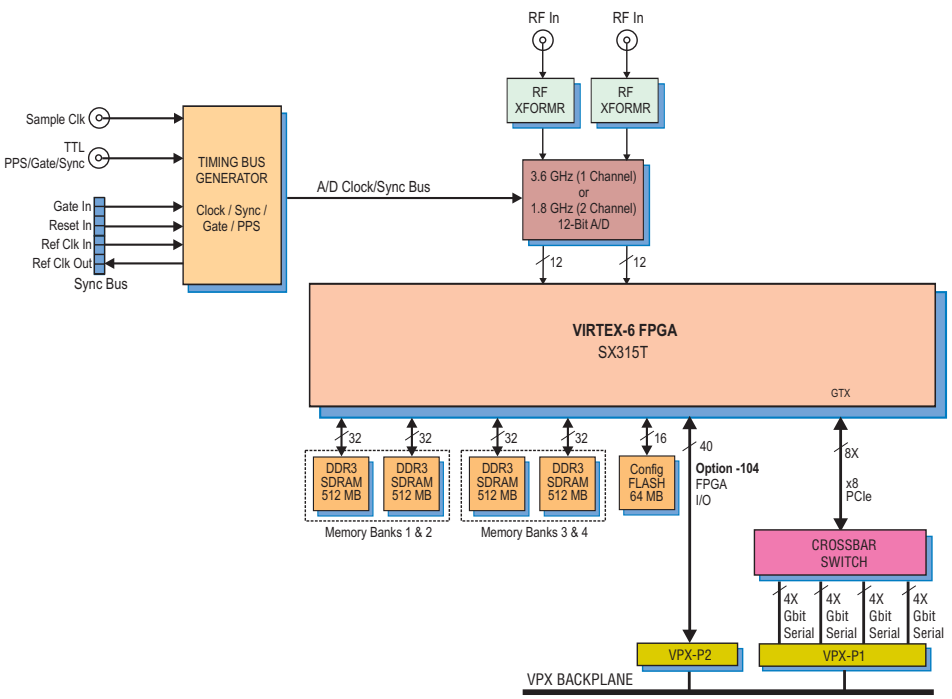
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programmable one- or two-channel DDC (Digital Downconverter)
- PCI Express (Gen. 1 & 2) interface, up to x8
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Module

The 53641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

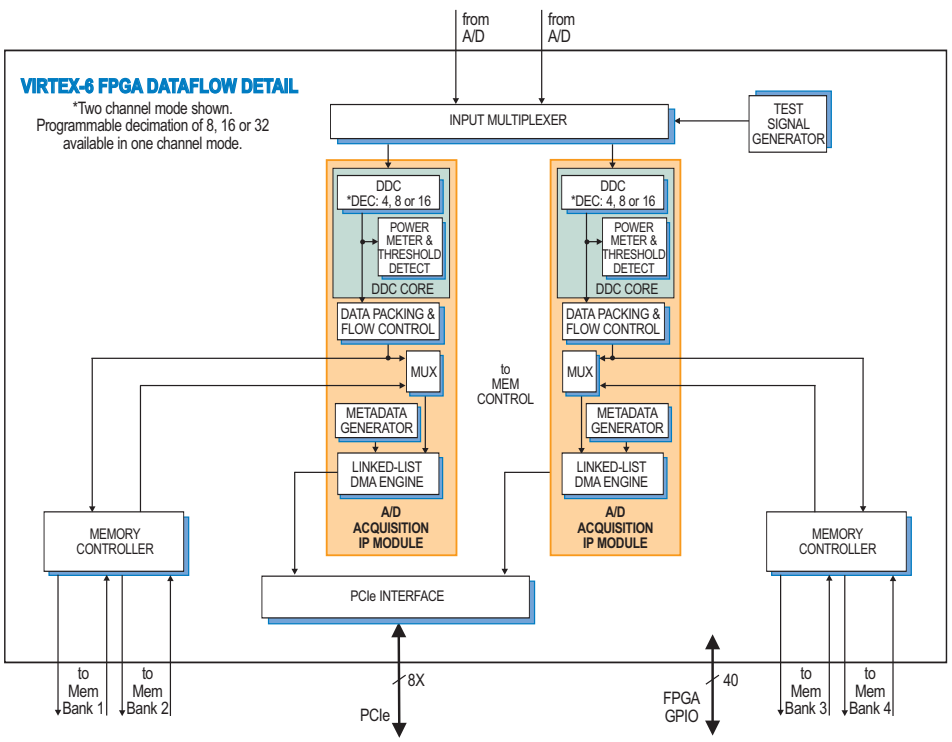
Clocking and Synchronization

The 53641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 53641's can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 53641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ PCI Express Interface

The Model 53641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53641 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1or Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

Model 53650 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53650 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53650 includes two A/Ds, one DUC (digital upconverter), two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

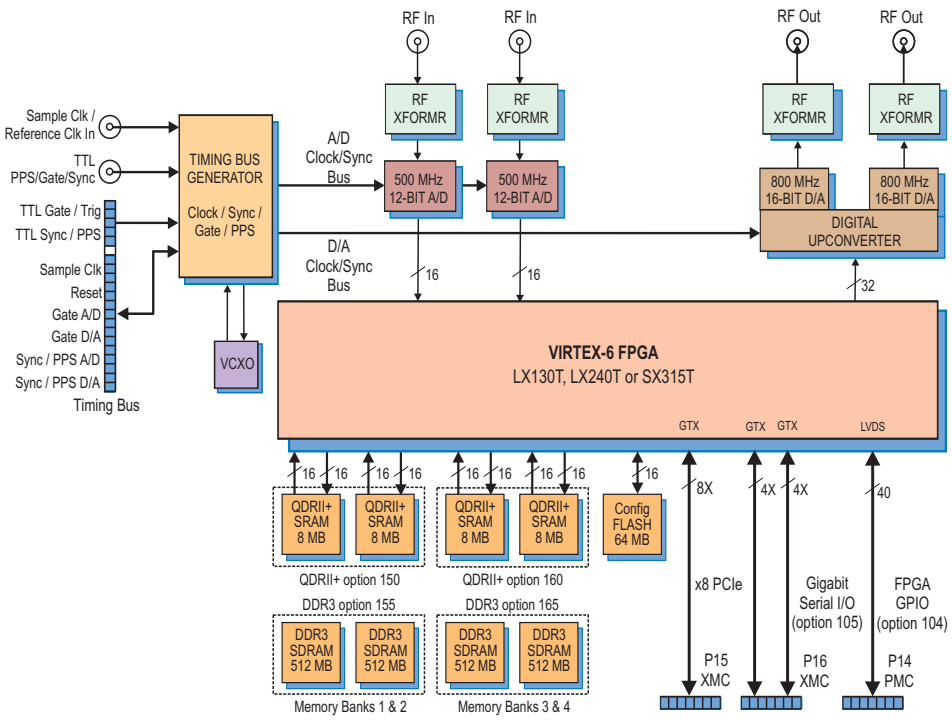
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

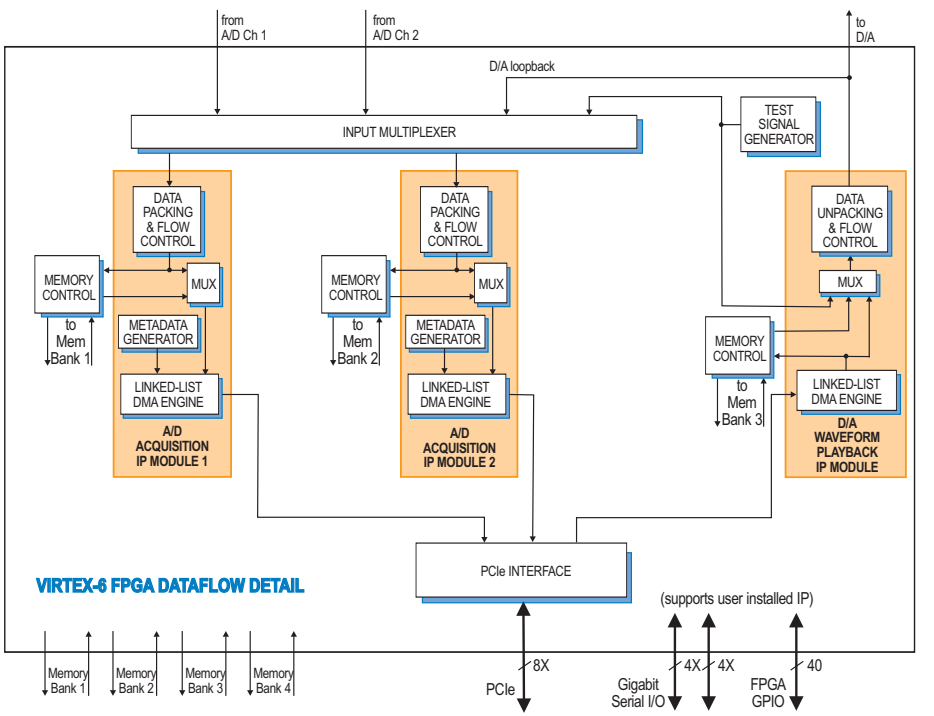
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. ➤



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Model 53650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53650	Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep.

Fabric-Transparent Crossbar Switch

The 53650 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector for serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen.1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 53651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 53651 COTS (left) and rugged version

Cobalt GateFlow ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53651 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53651 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

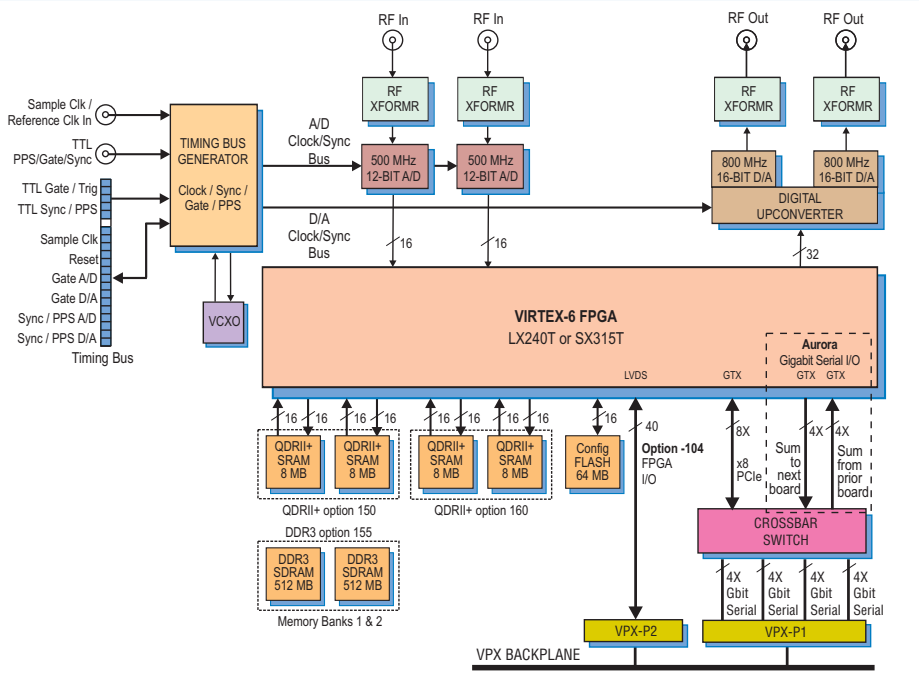
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Model 53651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

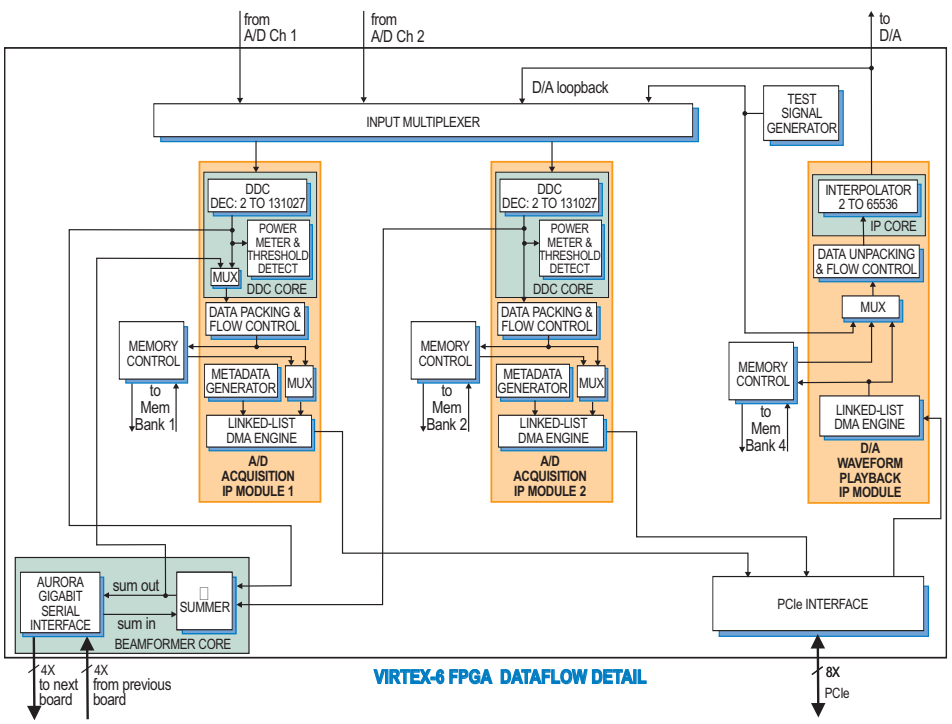
A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53651's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



VIRTEX-6 FPGA DATAFLOW DETAIL

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53651 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits ➤

Model 53651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240 FPGA
-064	XC6VSX315 FPGA
-104	LVDS FPGA I/O through the VPX P2 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

A/D Converters (option -014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link over the VPX P1connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-T2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Model 53660 COTS (left) and rugged version

General Information

Model 53660 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

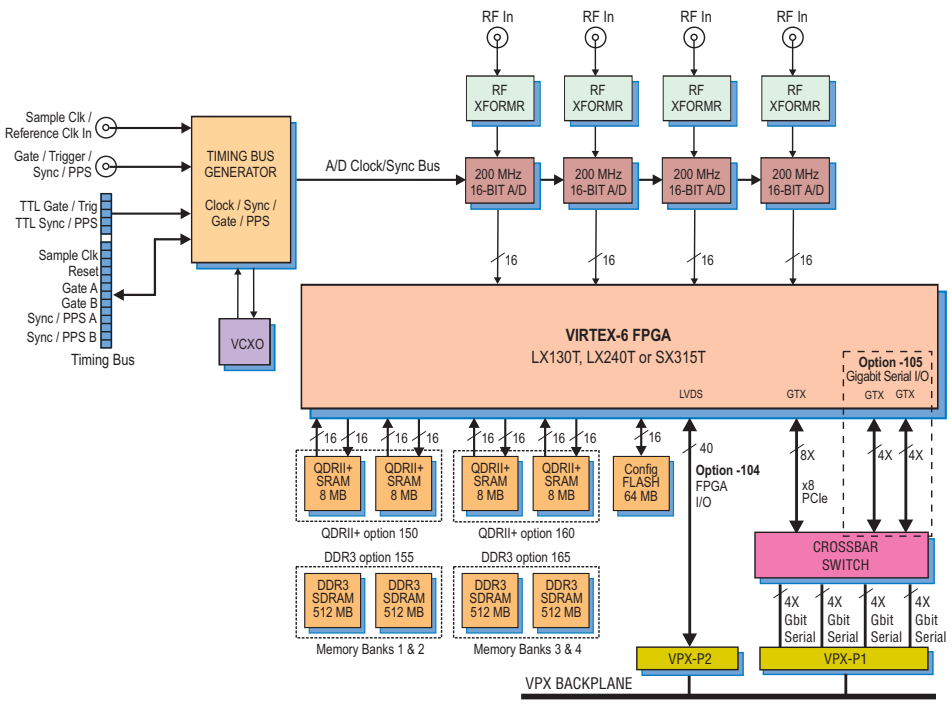
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

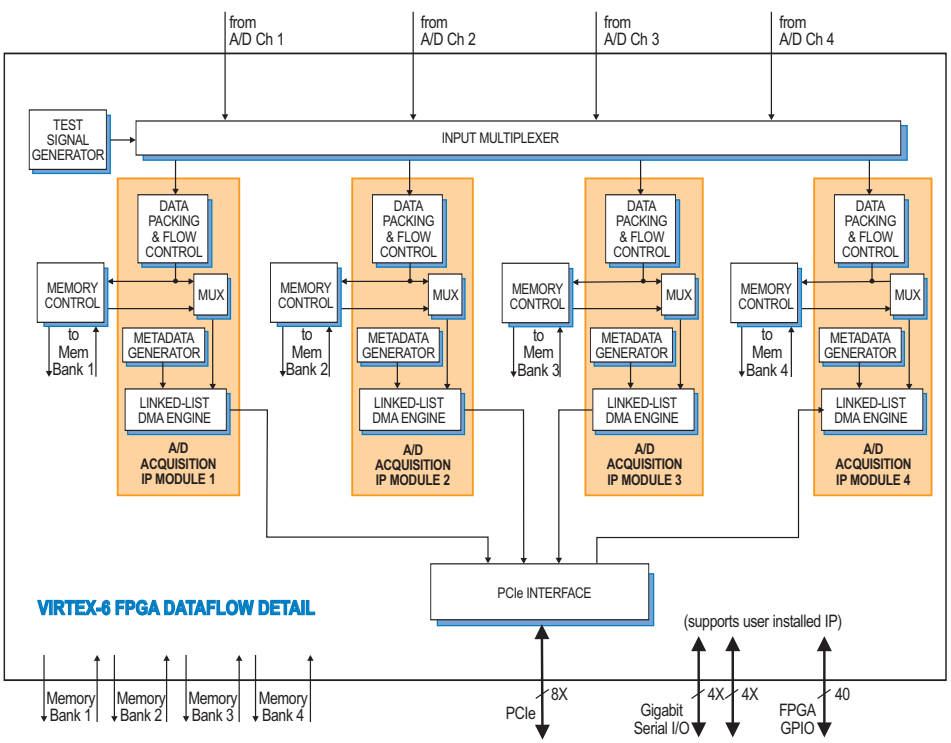
The Model 53660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Modules

The 53660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53660	4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Fabric-Transparent Crossbar Switch

The 53660 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

Model 53661 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53661 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53661 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

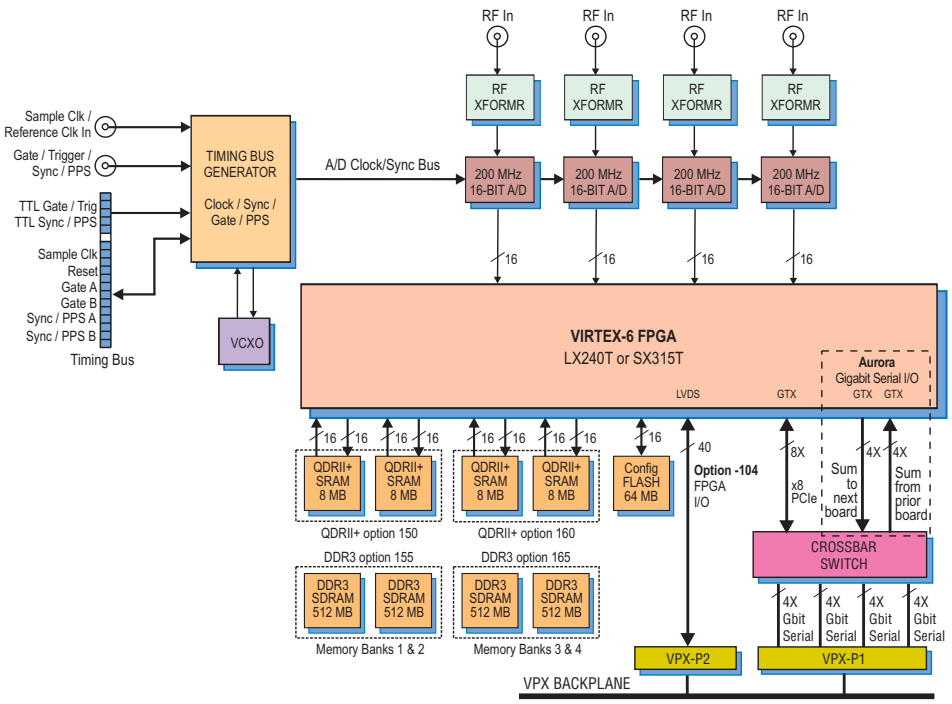
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

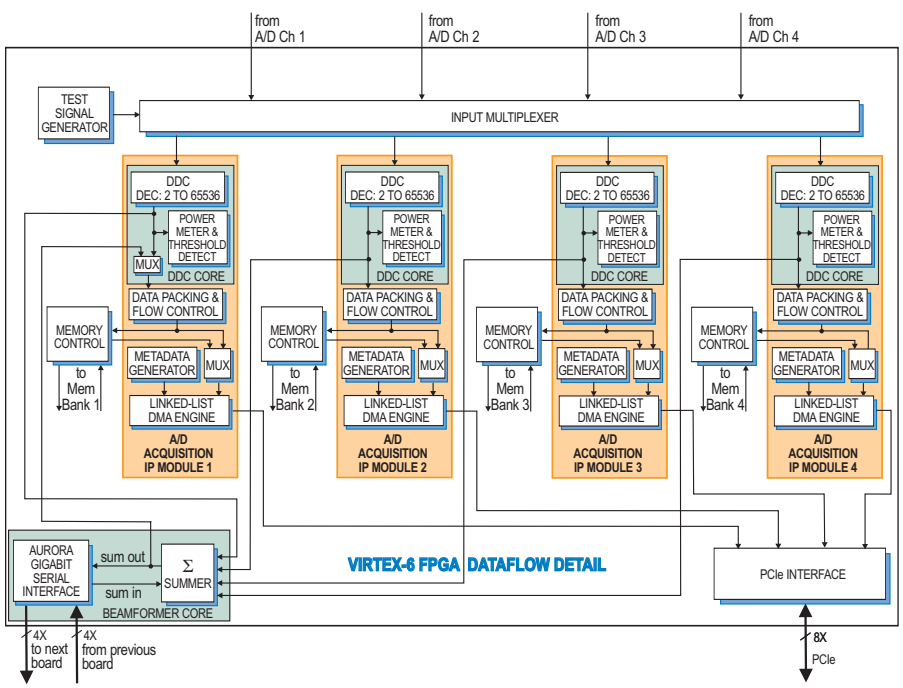
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.



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Model 53661 — 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Memory Resources

The 53661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. DDR3 SDRAM banks can each be up to 512 MB deep.

Fabric-Transparent Crossbar Switch

The 53661 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector,
- **Functions:** trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCIe Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

Model 53662 COTS (left) and rugged version

General Information

Model 53662 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

The 53662 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 53662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

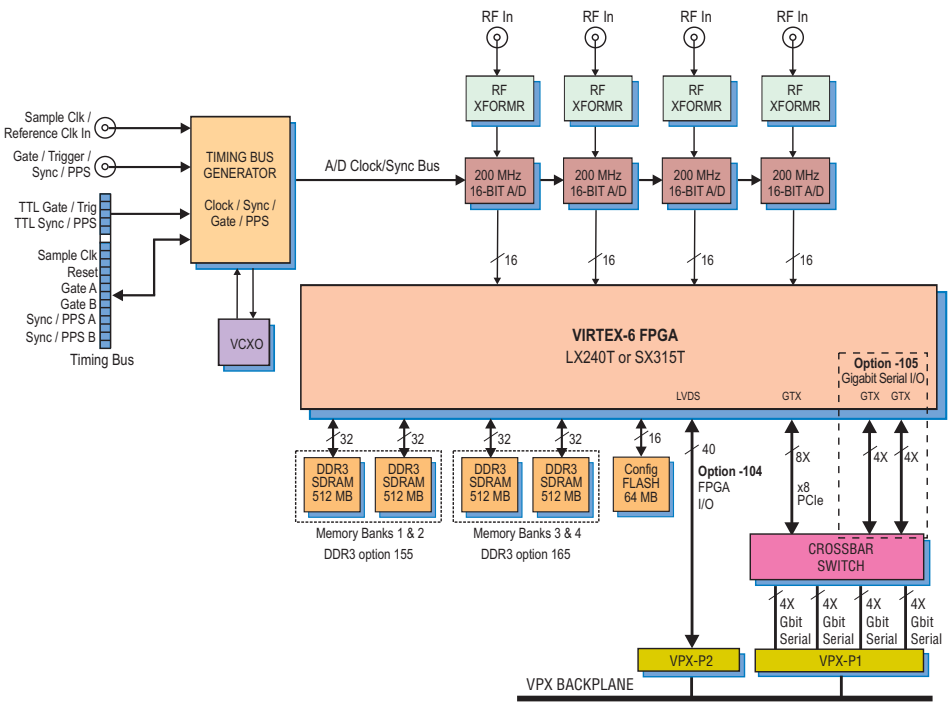
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

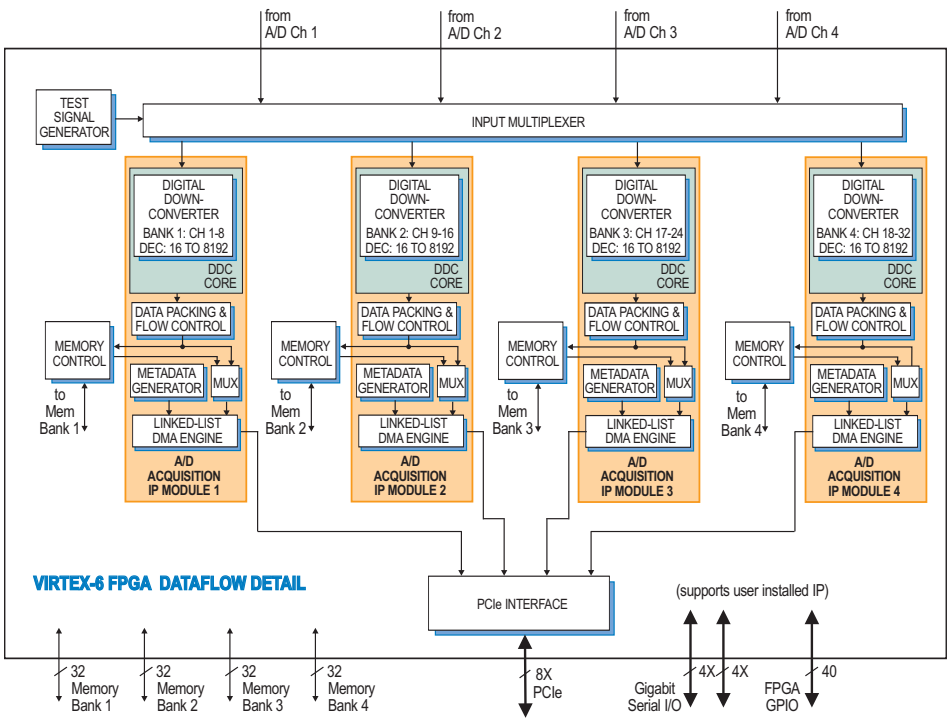
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.



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Model 53662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53662 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
53662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53662 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53663

1100-Channel GSM Channelizer with Quad A/D - VPX

Model 53663 Commercial (left) and rugged version

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8
- 3U VPX form factor provides a compact, rugged platform

General Information

Model 53663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 53663 is a complete, full-featured subsystem, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

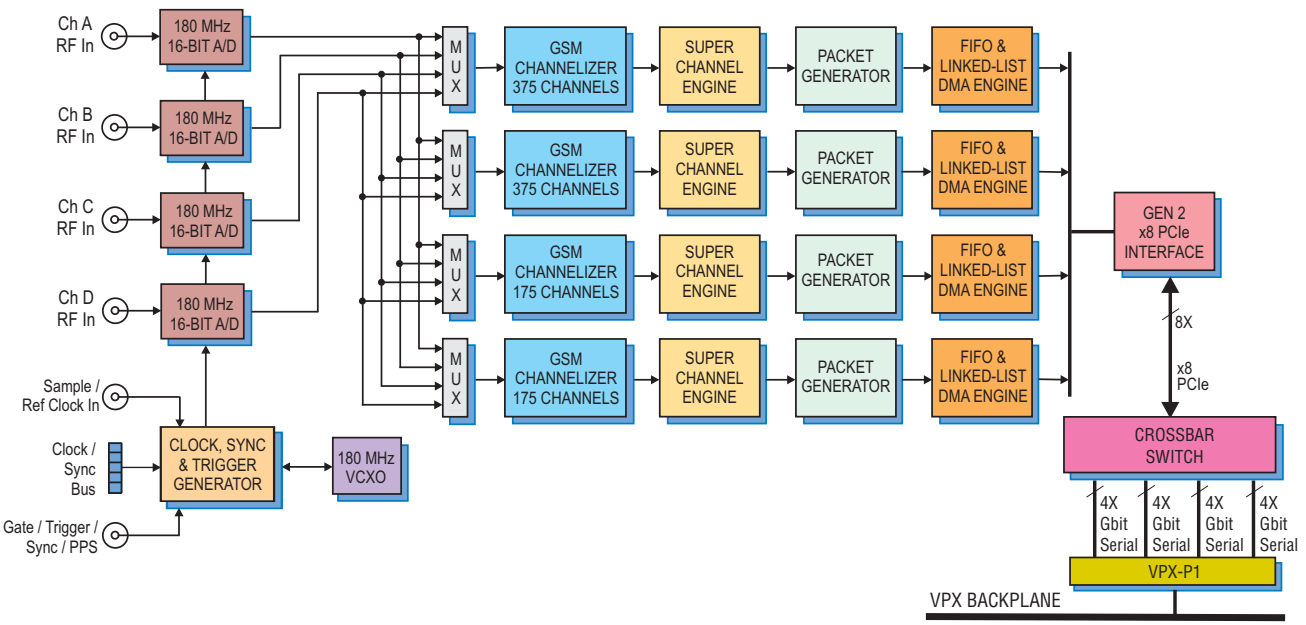
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 53663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤



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➤ The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 53663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 53663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI Express Interface

The Model 53663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 53663 and host.

Fabric-Transparent Crossbar Switch

The 53663 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X). ➤

Model 53663 — 1100-Channel GSM Channelizer with Quad A/D - VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53663	1100-Channel GSM Channelizer with Quad A/D - VPX

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics:**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  First: $-f_s/4$ (-270.8333 kHz)
  Second: 0 Hz
  Third: $+f_s/4$ (+270.8333 kHz)
  Fourth: $+f_s/2$ (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

Model 53664 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA-49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53664 is a member of the Cobalt® family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 53664 PCIe output supports fully the VITA-49.0 Radio Transport (VRT) Standard.

The 53664 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

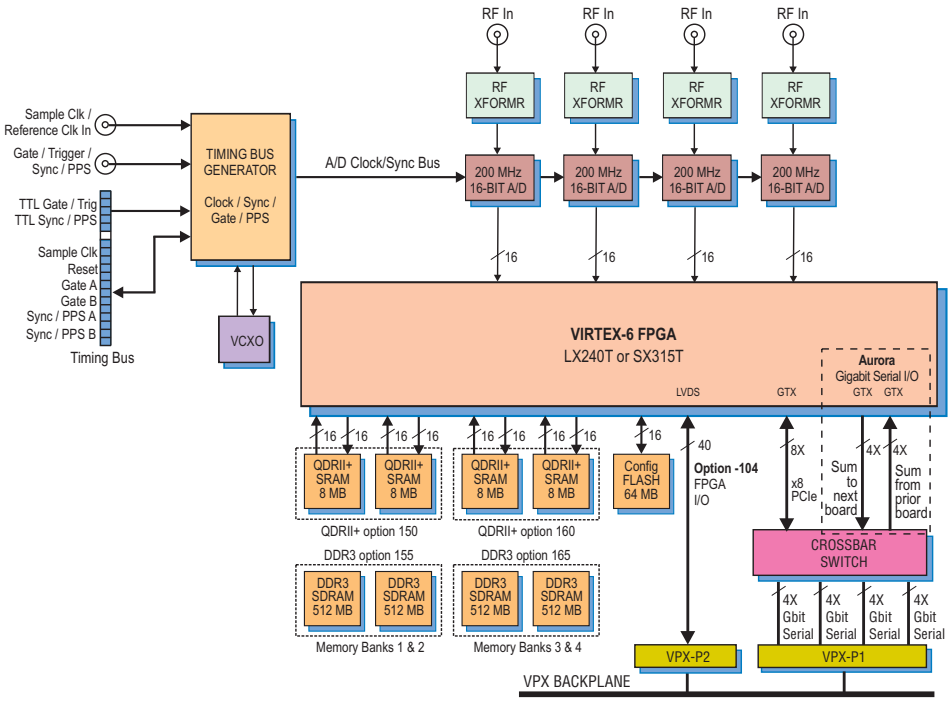
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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A/D Acquisition IP Modules

The 53664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53664 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

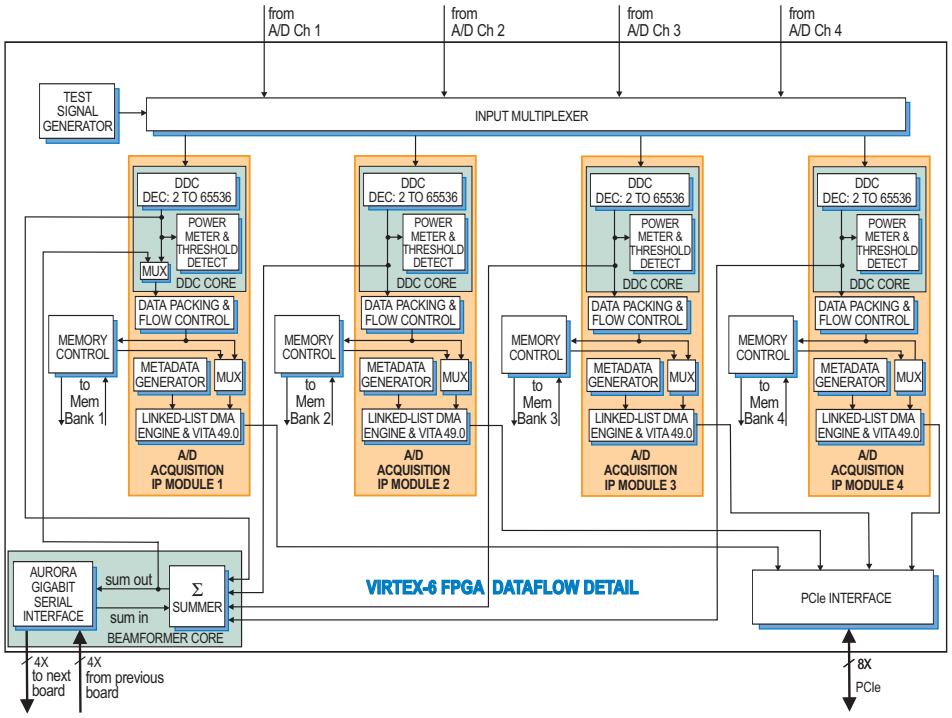
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53663's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA-49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 53664 supports fully the VITA 49.0 specification. ➤



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➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53664's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53664 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X). ➤

Model 53664 — 4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector,
- **Functions:** trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCIe Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

➤

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Model 53670 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- User-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53670 includes general purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

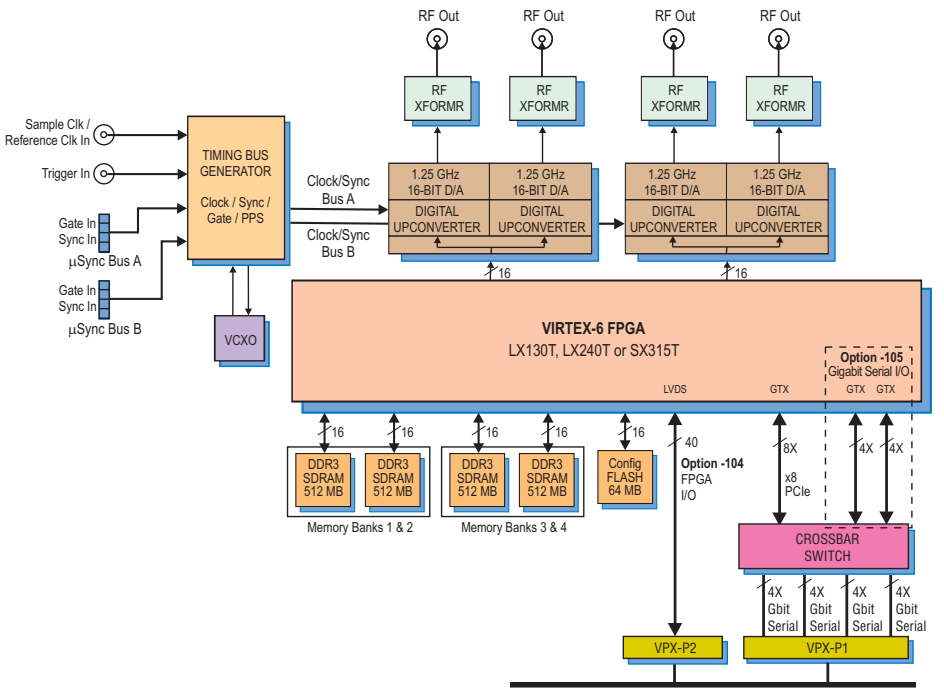
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5392 or 9192 Cobalt Synchronizers can drive multiple 53670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 53670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

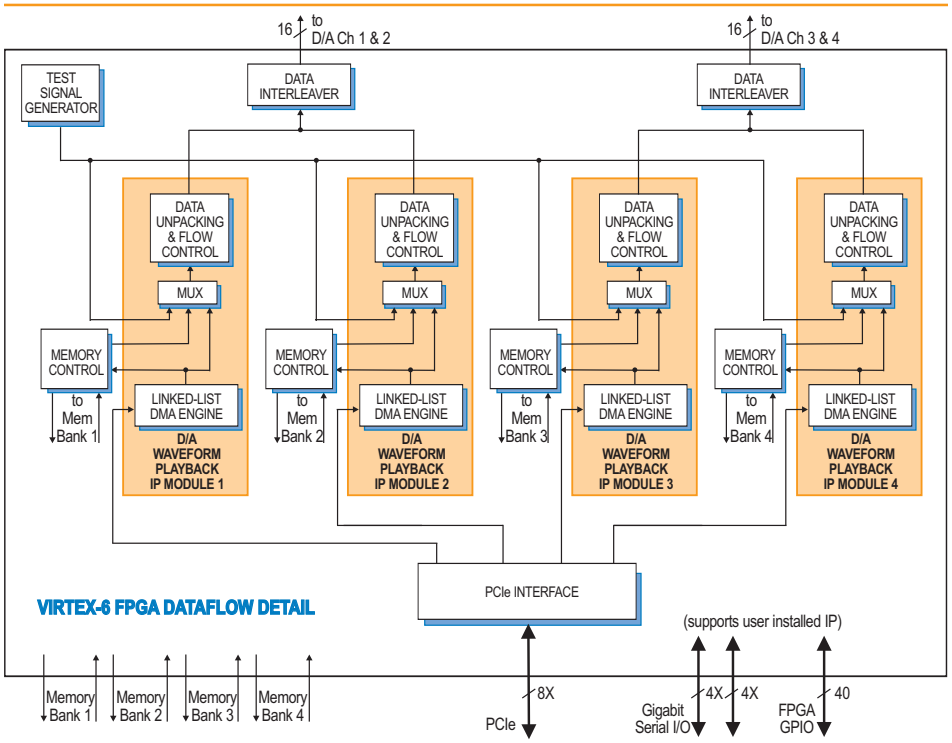
The Model 53670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

D/A Waveform Playback IP Module

The Model 53670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
53670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Fabric-Transparent Crossbar Switch

The 53670 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Model 53671 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- Extended interpolation range from 2x to 1,048,576x
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53671 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

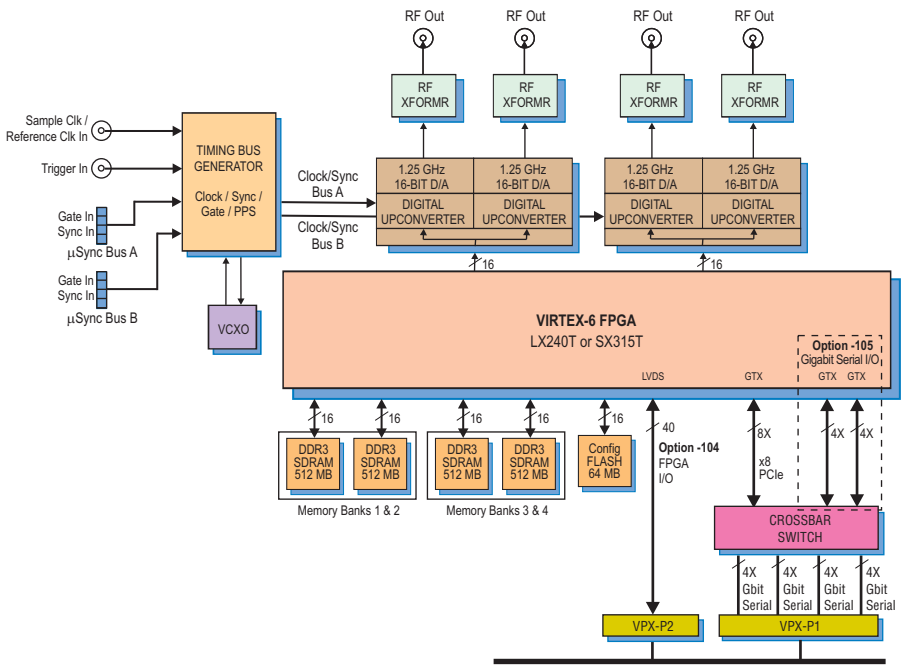
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 53671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5392 or 9192 Cobalt Synchronizers can drive multiple 53671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 53671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

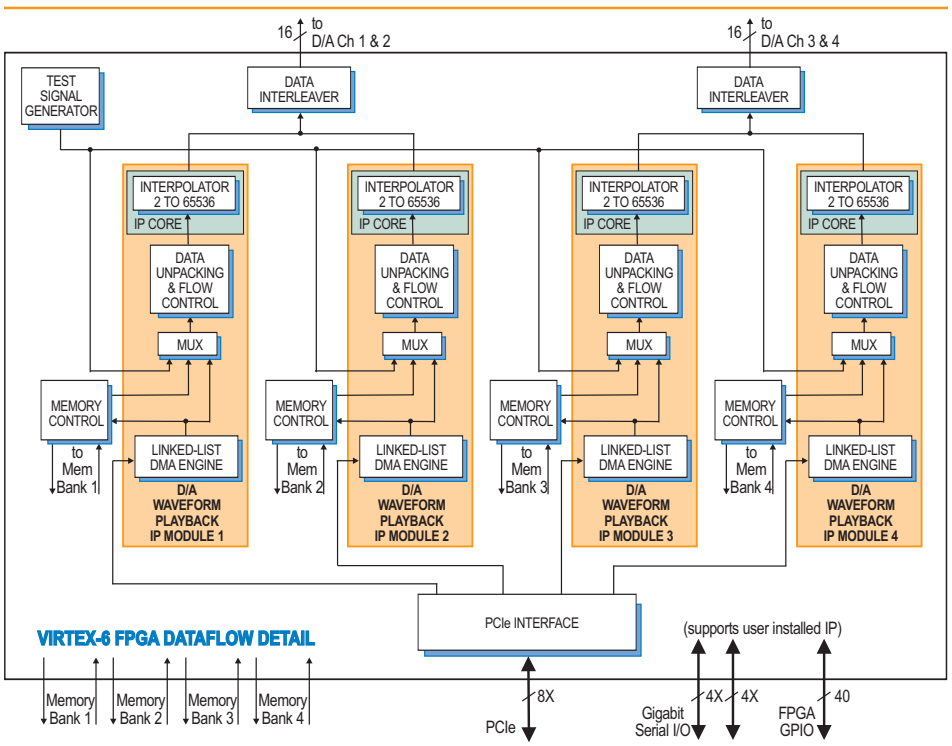
D/A Waveform Playback IP Module

The Model 53671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Options:

-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ PCI Express Interface

The Model 53671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53671 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array:
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 53690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

Model 53690 COTS (left) and rugged version

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 53690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

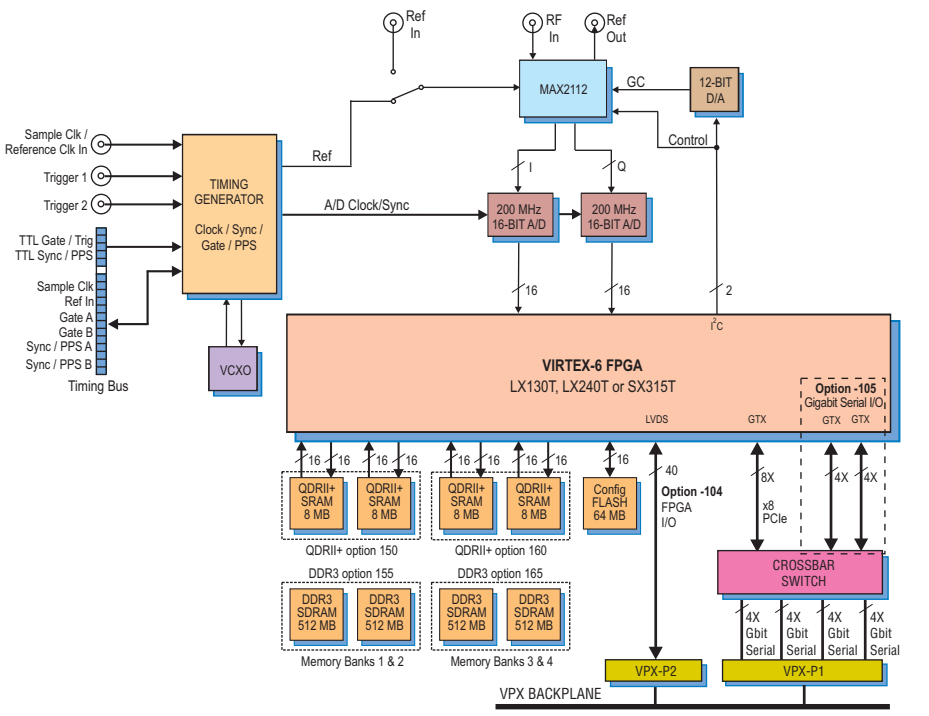
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

➤ RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

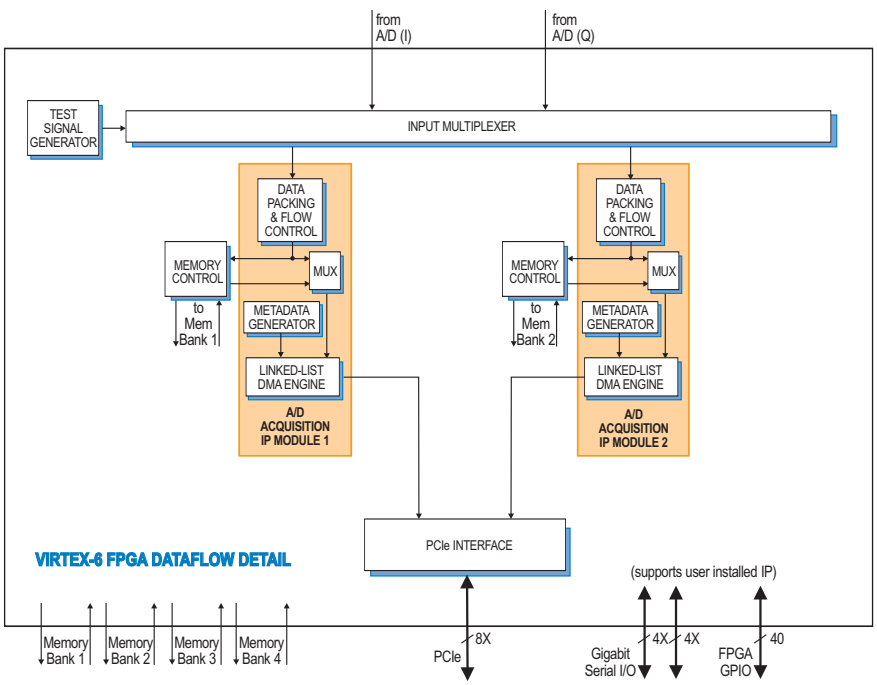
The 53690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. ➤

A/D Acquisition IP Modules

The 53690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 53690 — L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Built-in memory functions include multichannel A/D data capture, tagging and streaming. The factory-installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user IP within the FPGA.

Fabric-Transparent Crossbar Switch

The 53690 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference ($freq_{REF}$):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- ***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector for serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2 x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

Model 53720 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53720 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53720 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

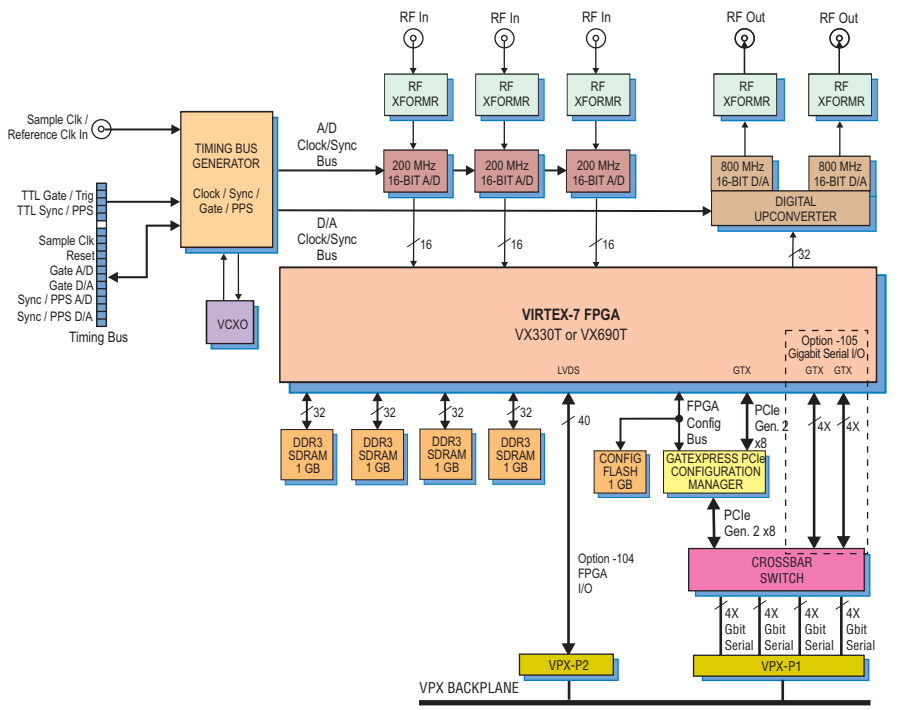
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

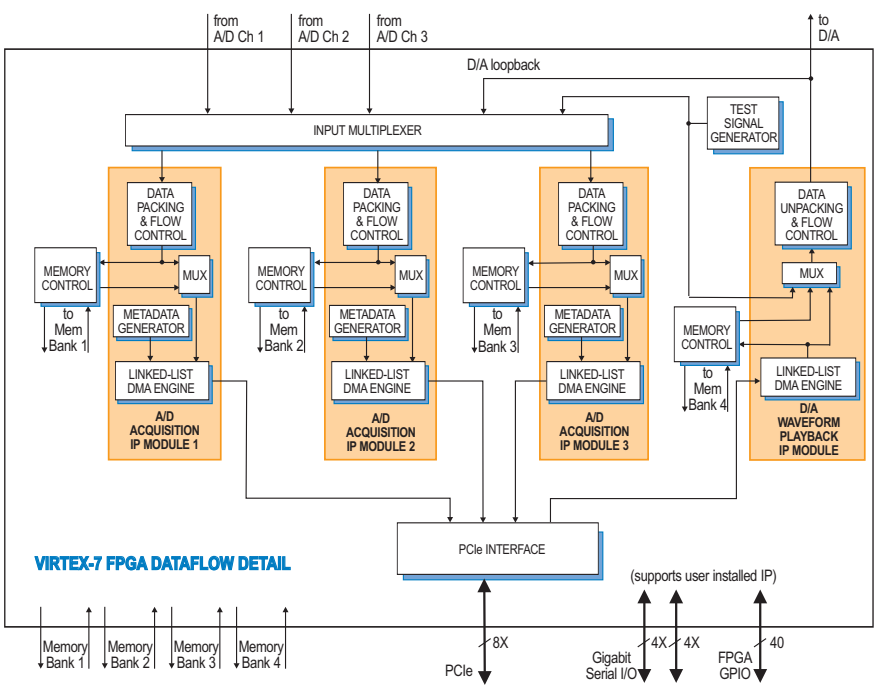
A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of SSMC connectors. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

Memory Resources

The 53720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 53720 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator).

Crossbar Switch

The 53720 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Model 53721 COTS (left) and rugged version

General Information

Model 53721 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

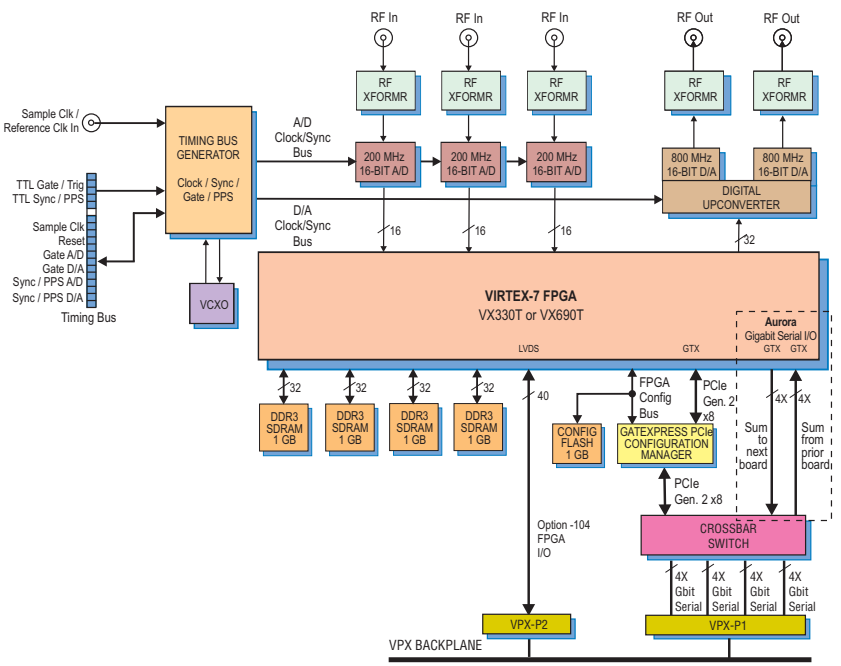
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Model 53721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

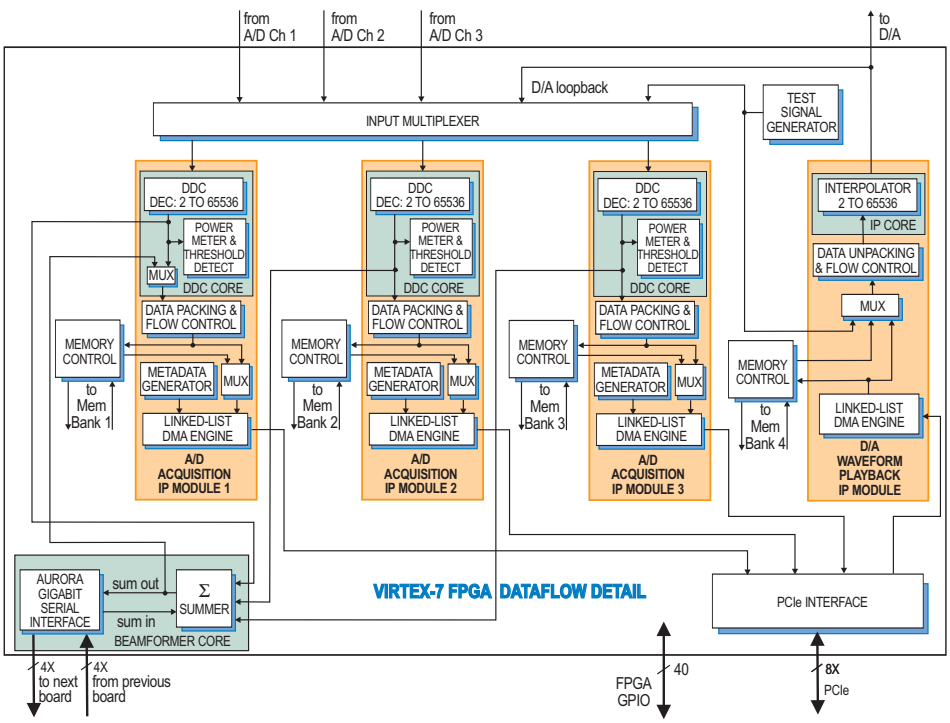
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53721's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Model 53721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Memory Resources

The 53721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53721 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53721's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

Model 53721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Model 53730 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53730 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

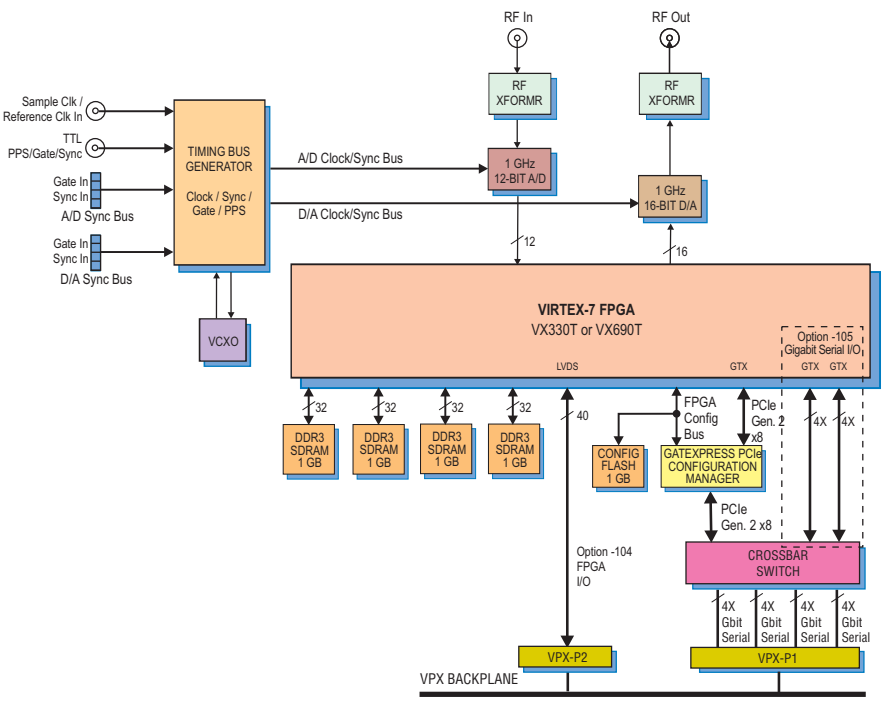
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Module

The 53730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

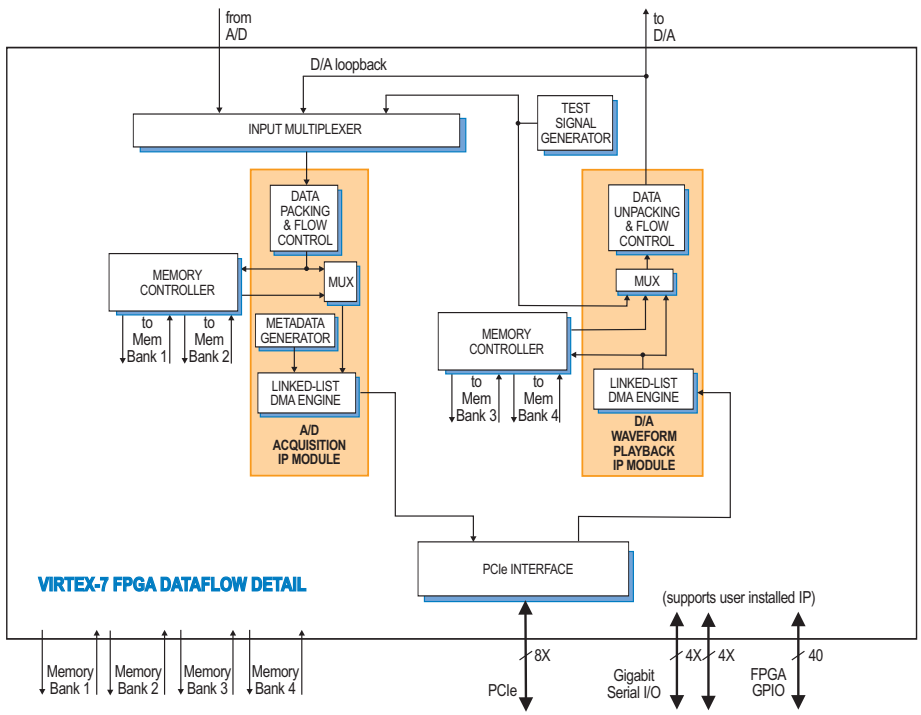
A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Memory Resources

The 53730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 53730 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53730	1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

Crossbar Switch

The 53730 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 53741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Model 53741 COTS (left) and rugged version

Onyx

GateXpress

ReadyFlow Board Support Package

GateFlow

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*

General Information

Model 53741 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

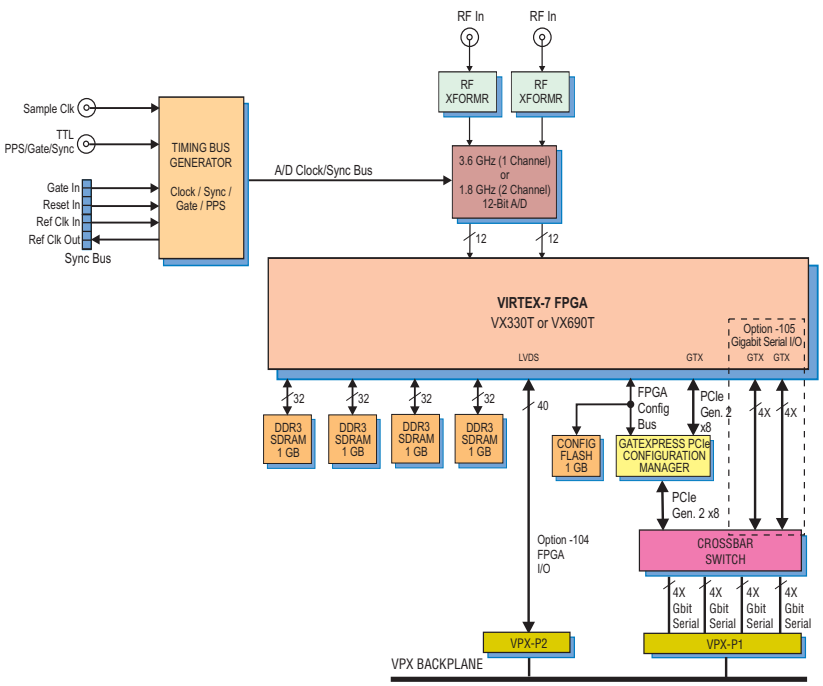
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Module

The 53741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

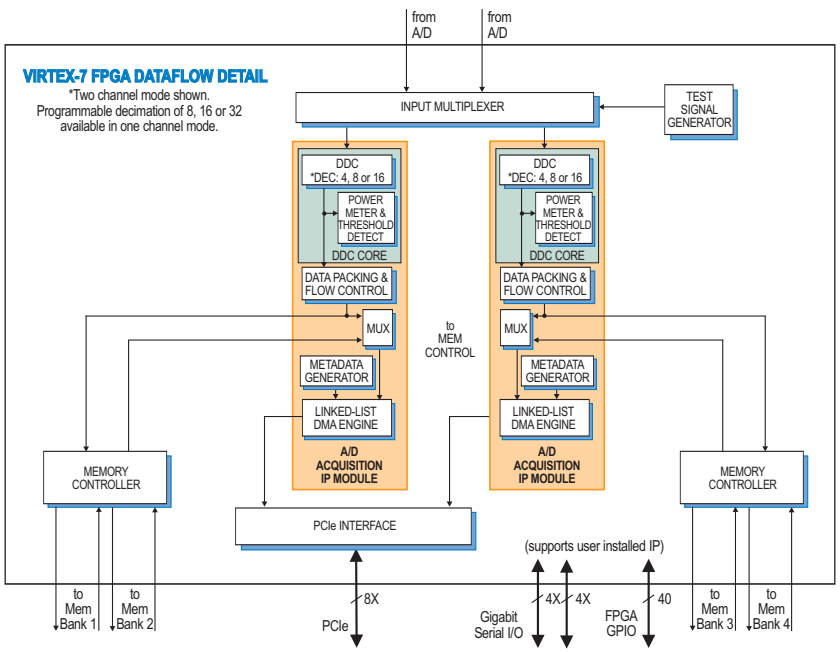
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Memory Resources

The 53741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Crossbar Switch

The 53741 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

Clocking and Synchronization

The 53741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 53741's can be synchronized with a simple cable. For larger systems, multiple 53741's can be synchronized using the Model 5392 high-speed sync board to drive the sync bus.

PCI Express Interface

The Model 53741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel : 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Model 53751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

Model 53751 commercial (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*

General Information

Model 53751 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53751 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53751 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

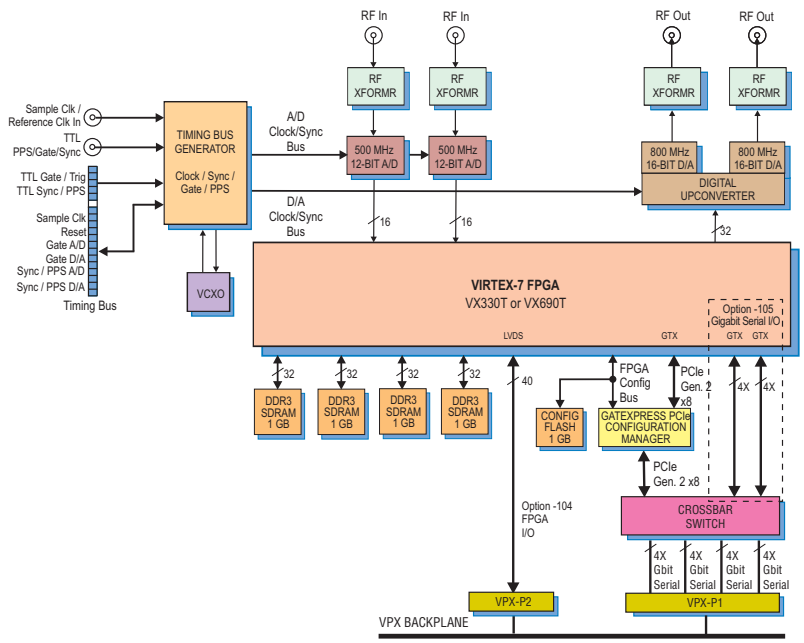
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 53751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

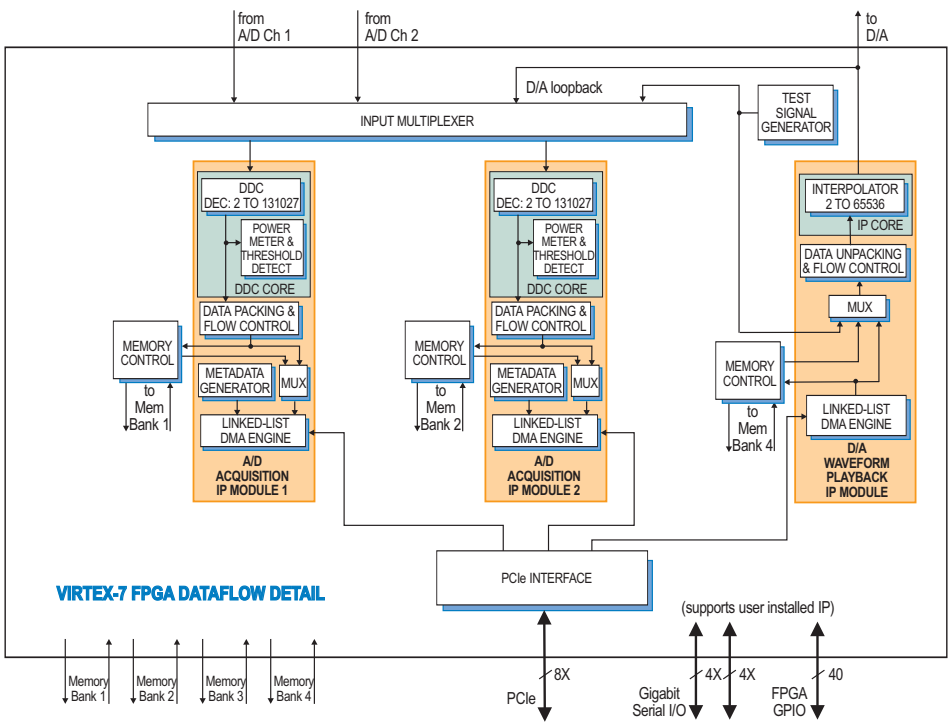
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458

Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53751's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53751 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

PCI Express Interface

The Model 53751 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 53751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 53760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

Model 53760 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Advanced reconfigurability features
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53760 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

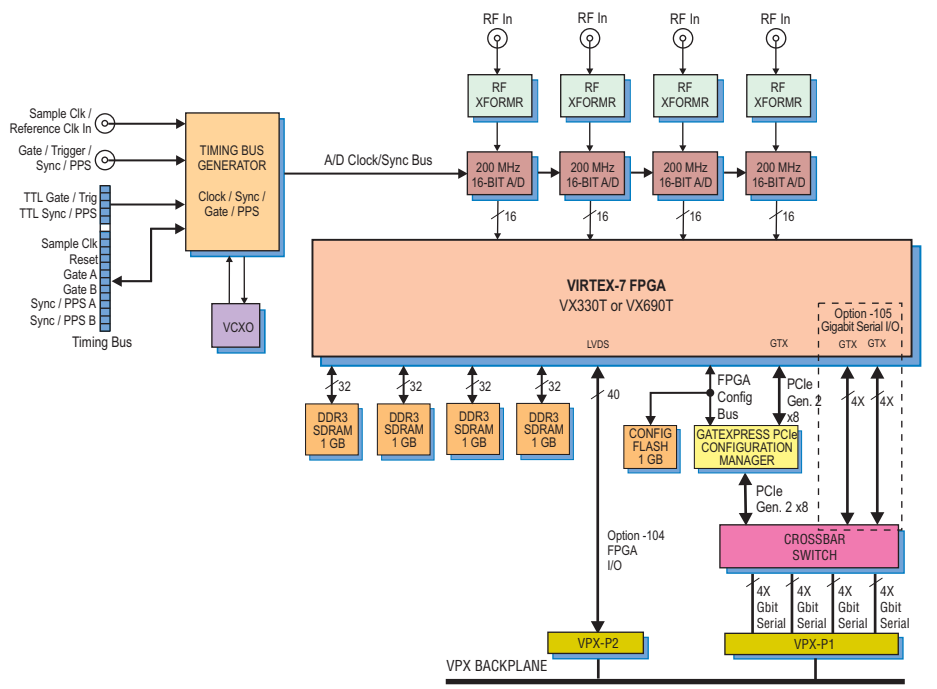
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

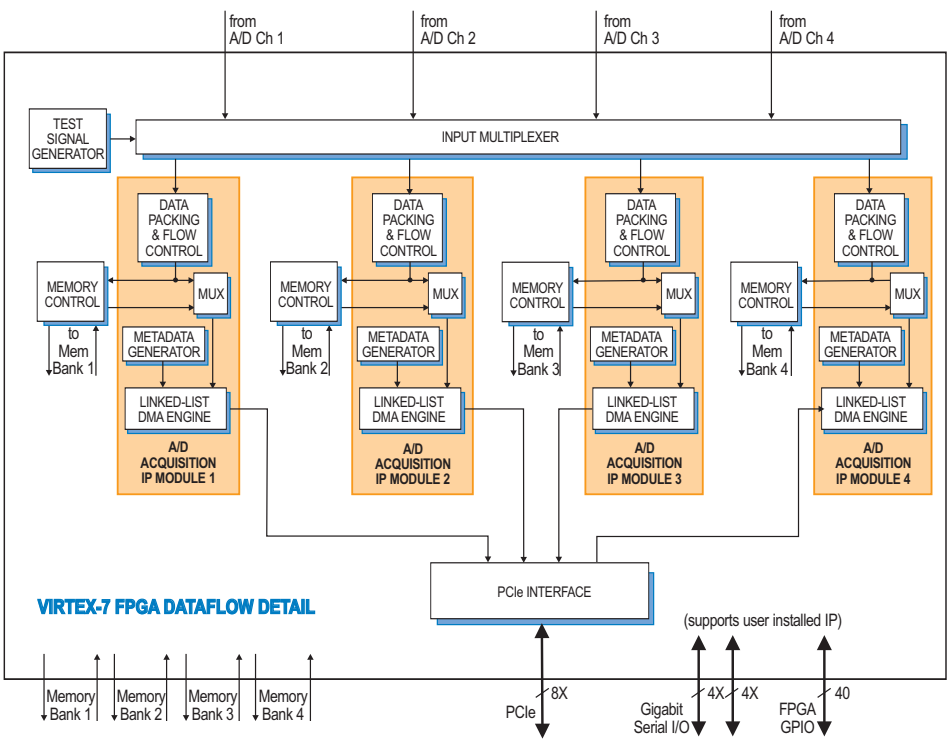
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel ➤

A/D Acquisition IP Modules

The 53760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Model 53760 — 4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

PCI Express Interface

The Model 53760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53760 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53760	4-Channel 200 MHz A/D with Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53760's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8;

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Model 53761 COTS (left) and rugged version

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53761 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53761 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

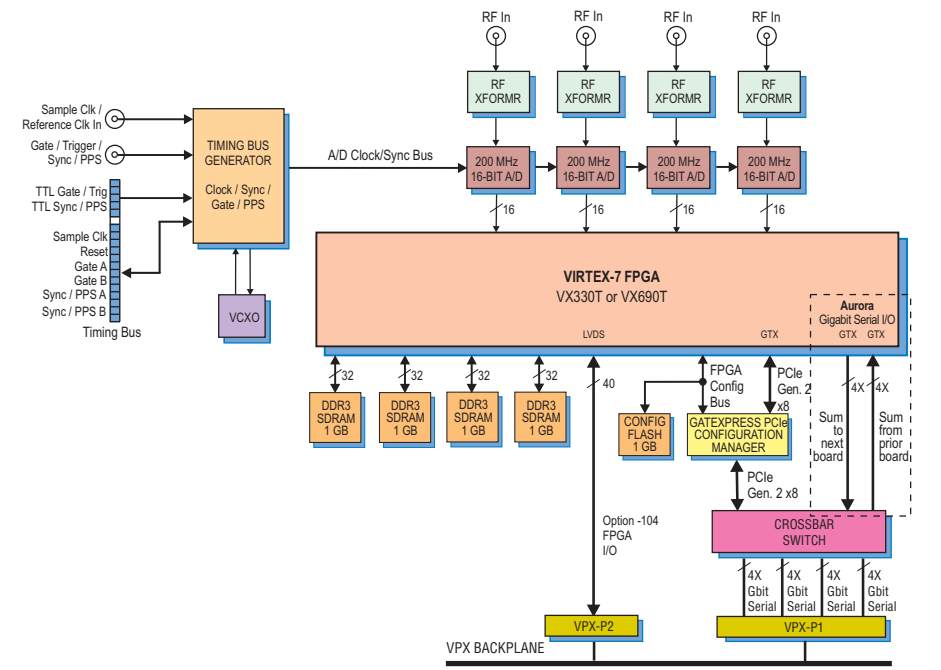
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 53761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

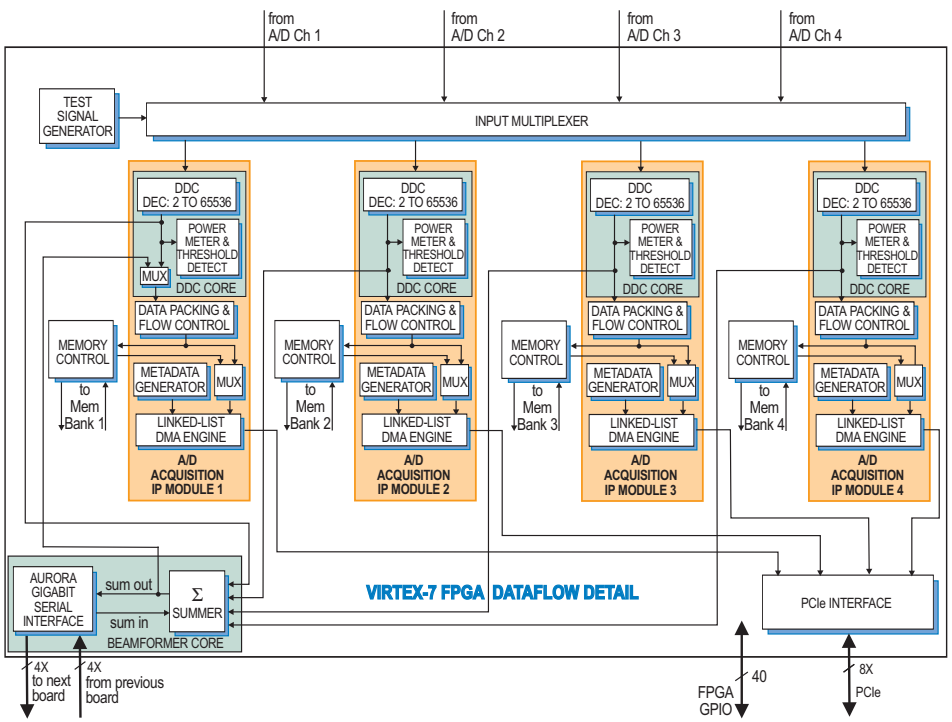
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53761's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53761 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53761 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. ➤

Model 53761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Model 53791 COTS (left) and rugged version

General Information

Model 53791 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 53791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 53791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 2 PCIe interface.

Thus, the 53791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

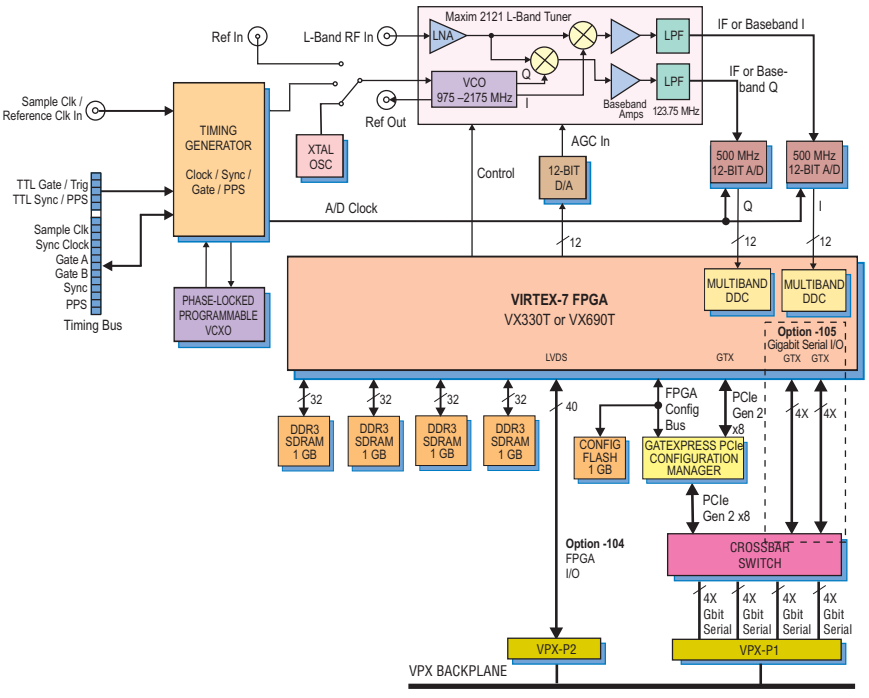
For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 53791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

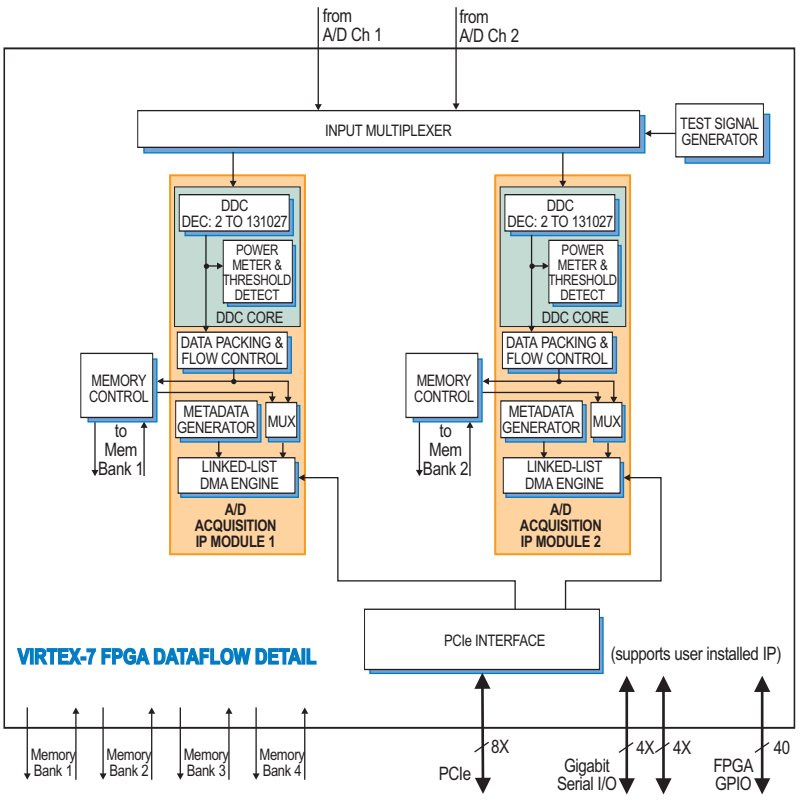
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

Fabric-Transparent Crossbar Switch

The 53791 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X). ➤

Model 53791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
53791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:

-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ PCI Express Interface

The Model 53791 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** –97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** 3 dB cutoff frequency: 123.75 MHz

A/D Converters
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Model 53131 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53131 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

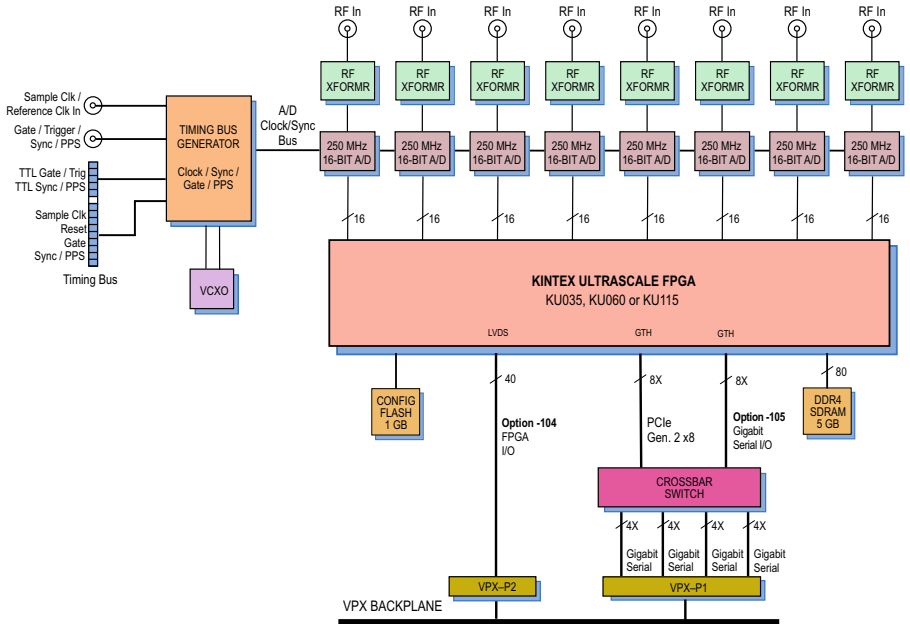
Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 53131 features eightA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

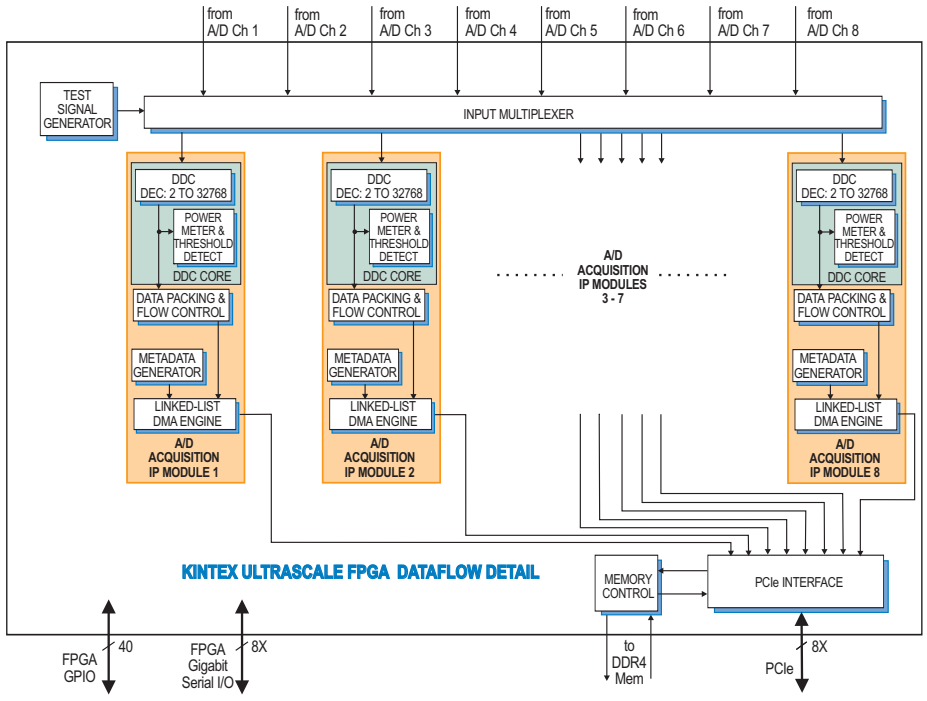
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 53131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Crossbar Switch

The 53131 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Ordering Information

Model	Description
52131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 53131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Connects 20 LVDS pairs between the FPGA and VPX P2
- **Option -105:** Connects eight gigabit serial lanes between the FPGA and VPX P1

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100.00 mm x 170.60 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

Model 53132 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 53132 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

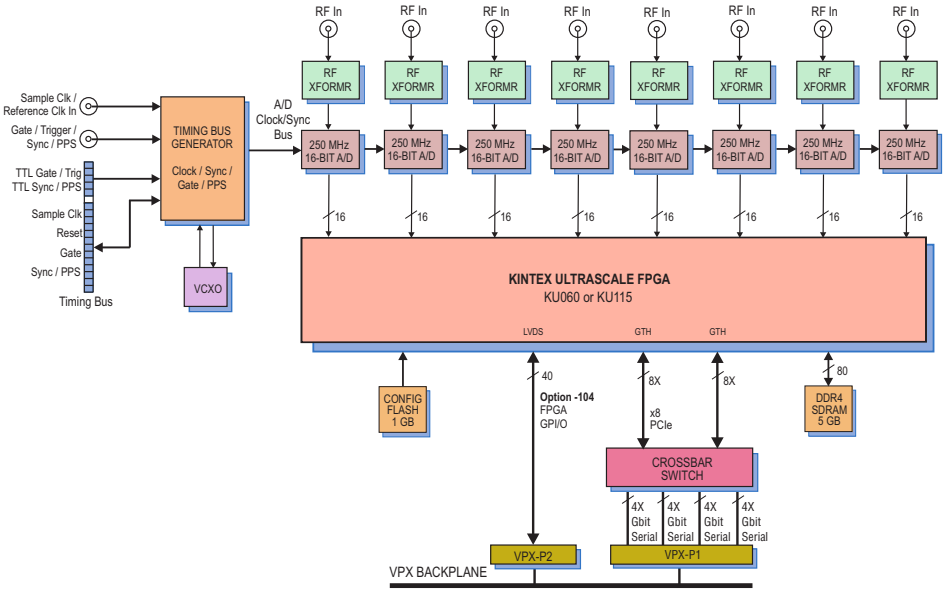
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52862 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downonversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

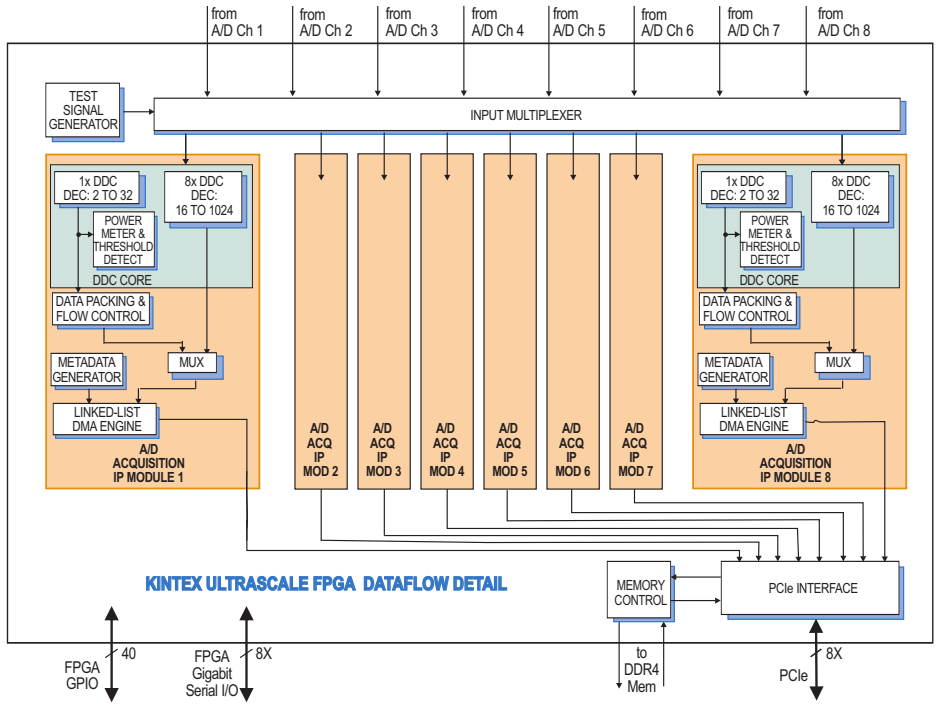
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected b oards. For larger systems, the Model 5293 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

➤ PCI Express Interface

The Model 53132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53132 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
53132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Eight banks, 8 channels per bank
Decimation Range: 16x to 1024x in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female MMCX connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity in all cases: 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New

Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Model 53141CORS (left) and Rygged versions

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53141 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

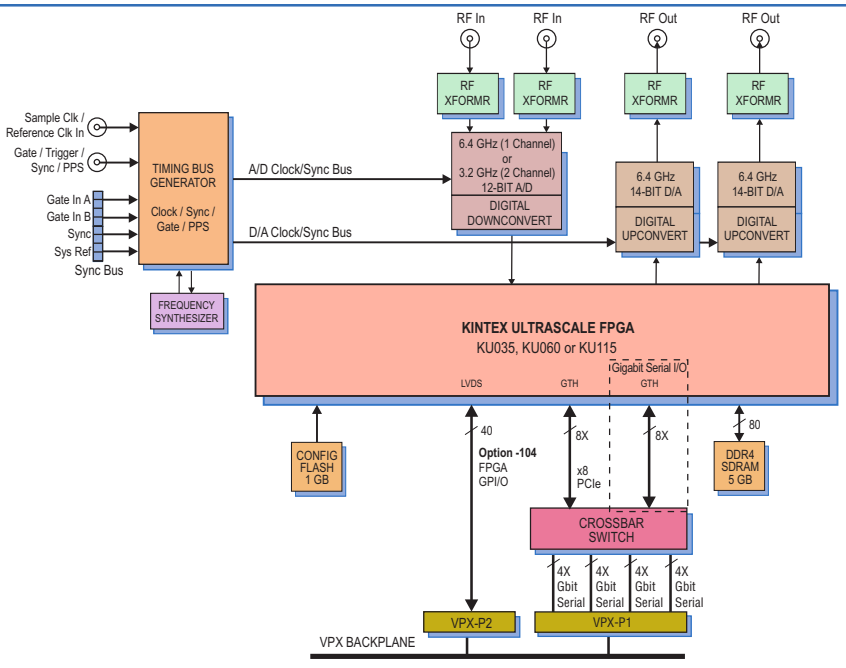
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Module

The 53141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 53141 factory installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections between the FPGA and the VPX P2 connector the for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 53141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

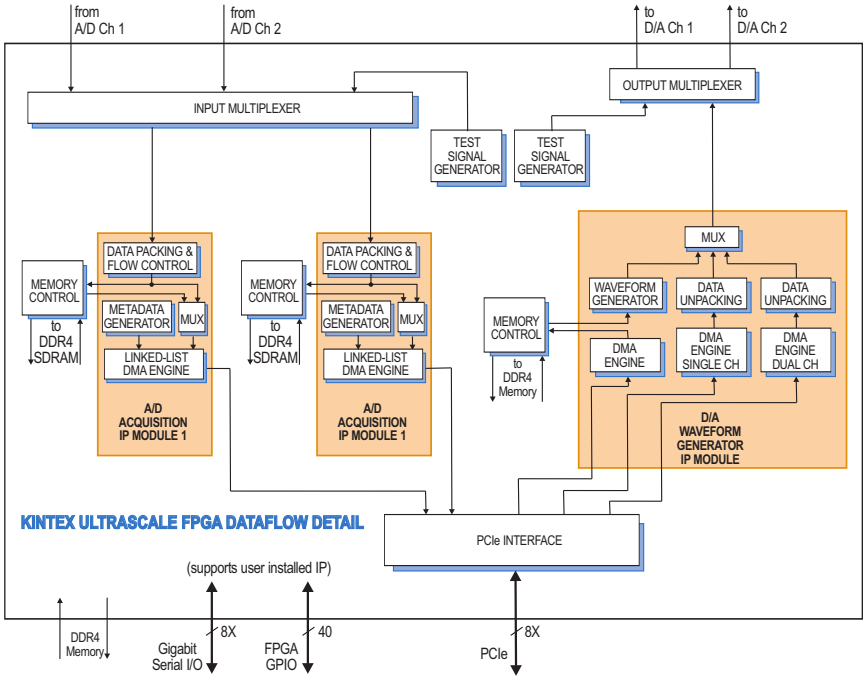
PCI Express Interface

The Model 53141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 53141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems. ➤



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Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
53141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Convection cooled, Level L3

➤ Fabric-Transparent Crossbar Switch

The 53161 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 4X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 53821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Model 53821 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53821 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 53821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

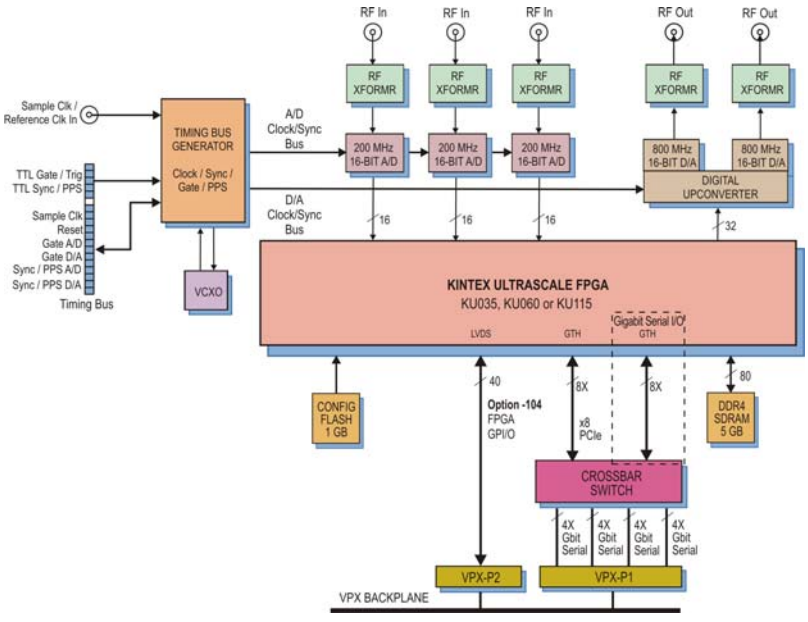
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 53821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 53821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

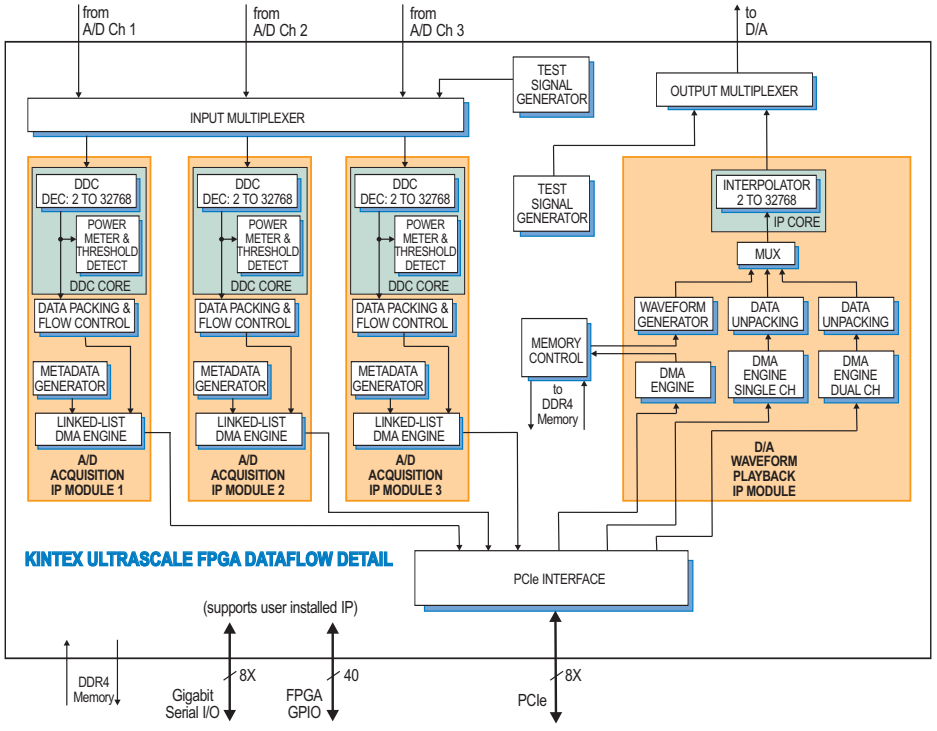
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 53821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

➤ Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

Model 53821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
53821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core
Interpolation Range: 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3U VPX board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

New!

Model 53841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Model 53841 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Down-converter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53841 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53841 is a high-speed data converter with programmable DDCs (digital down-converters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

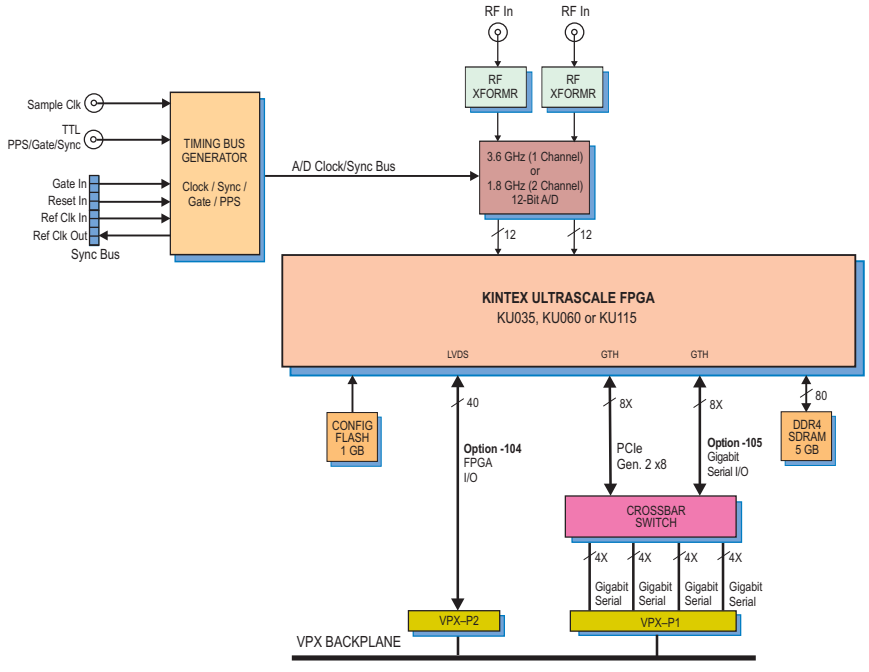
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Module

The 53841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has an associated 5 GB memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

A/D Converter Stage

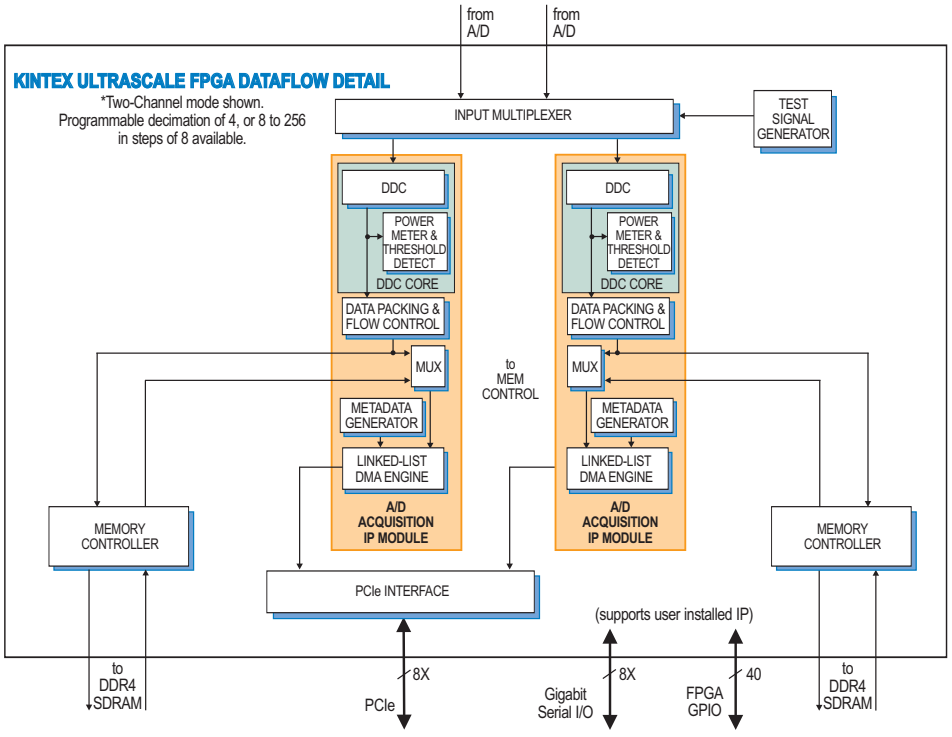
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

PCI Express Interface

The Model 53841 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board ➤



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Model 53841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Memory Resources

The 53841 architecture supports an optional 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Crossbar Switch

The 53841 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Ordering Information

Model	Description
53841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Clocking and Synchronization

The 53841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 53841's can be synchronized with a simple cable. For larger systems, multiple 53841's can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input Level:** may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Single-channel mode:** decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** the DDC can be bypassed completely
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Connects 20 LVDS pairs between the FPGA and VPX P2
- **Option -105:** Connects 8X gigabit serial links between the FPGA and VPX P1 or P2

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 53851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Model 53851 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Model 53851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

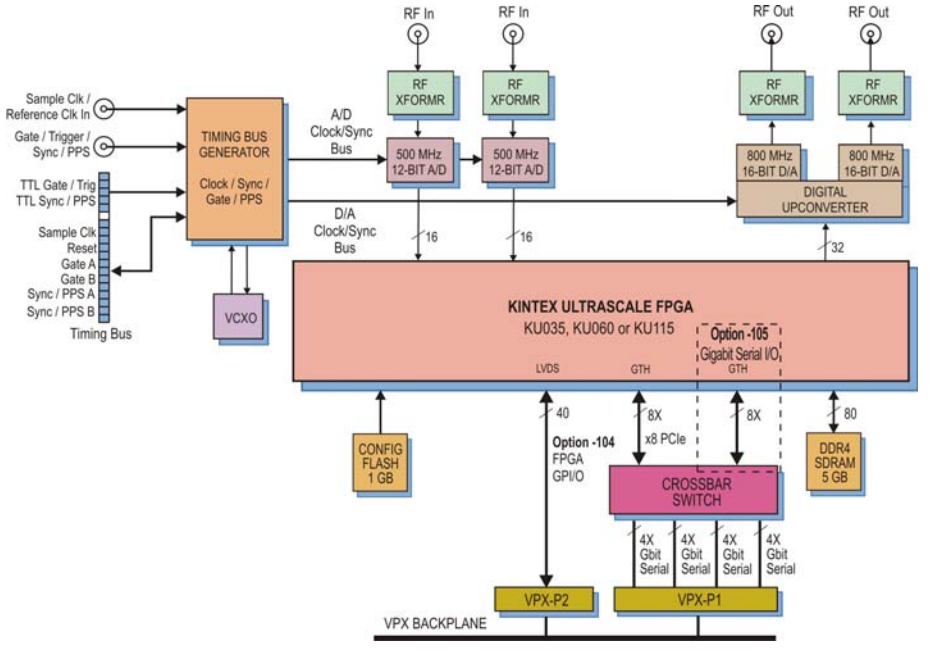
The 53851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 53851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 53851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

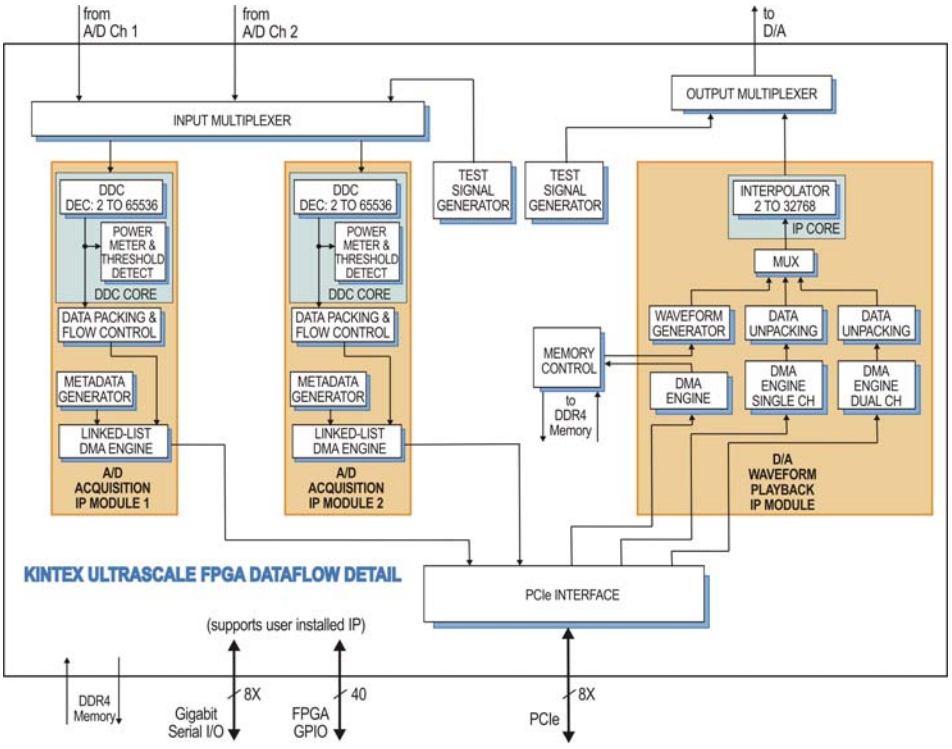
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 53851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53851 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014)

Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Model 53851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
53851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2 connector
-105	Gigabit serial FPGA I/O through VPX P1 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ **Digital Downconverters**
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3U VPX board 3.937 in x 6.717 in (100.00 mm x 170.61 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Model 53861 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53861 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

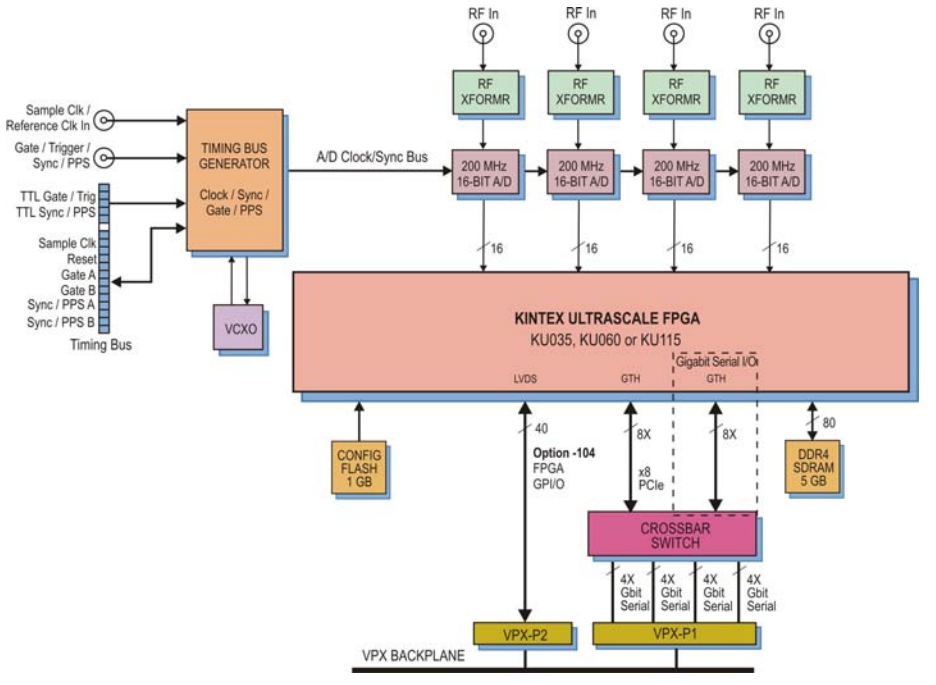
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 53861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 53861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

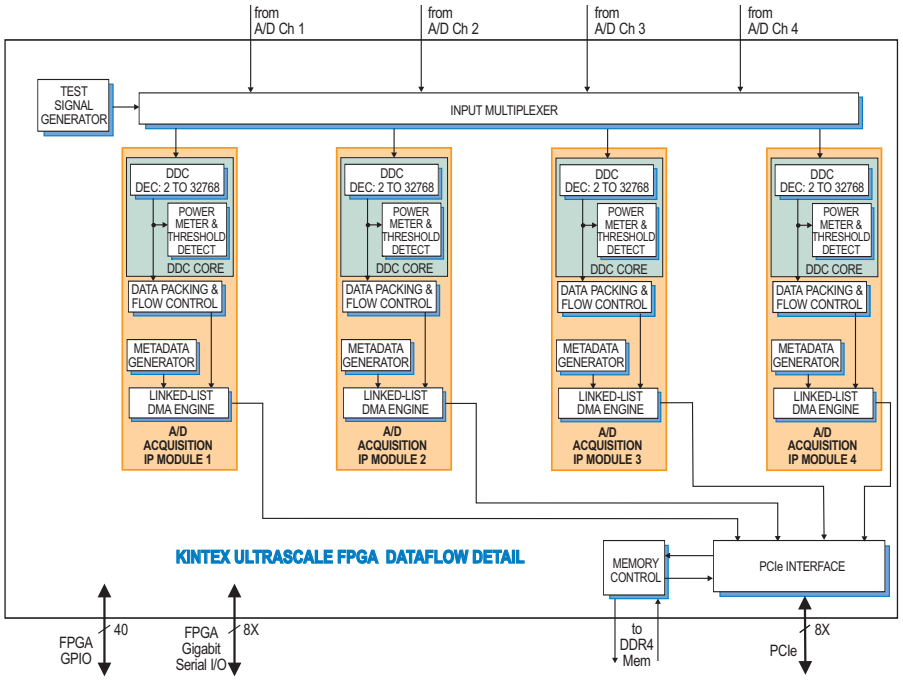
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 53861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

➤ Fabric-Transparent Crossbar Switch

The 53861 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
53861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

PCI Express Interface

The Model 53861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

Model 53862 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53862 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

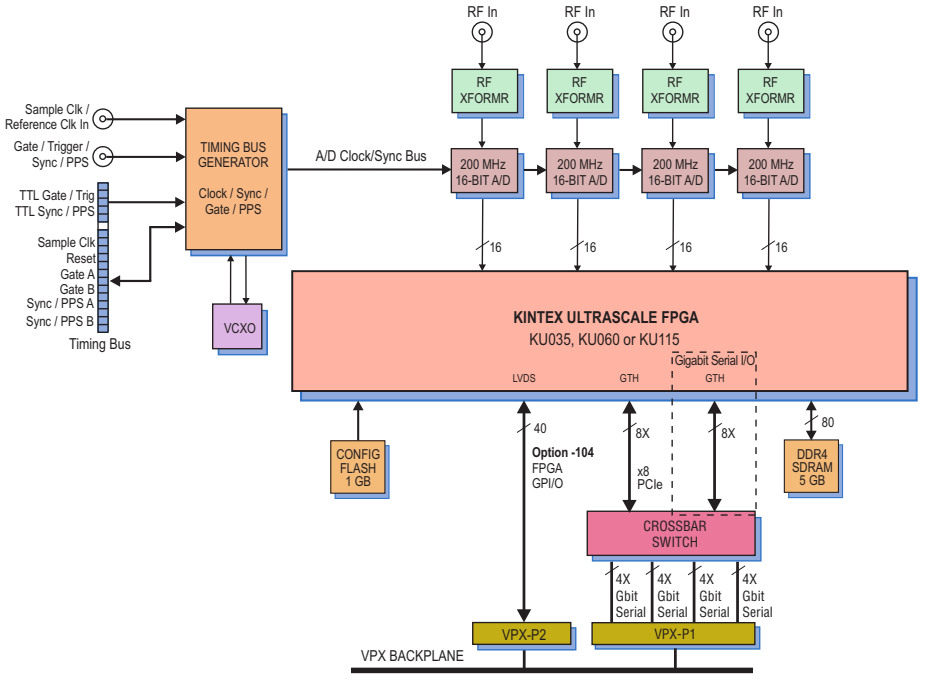
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included.) Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Model 53862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 53862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

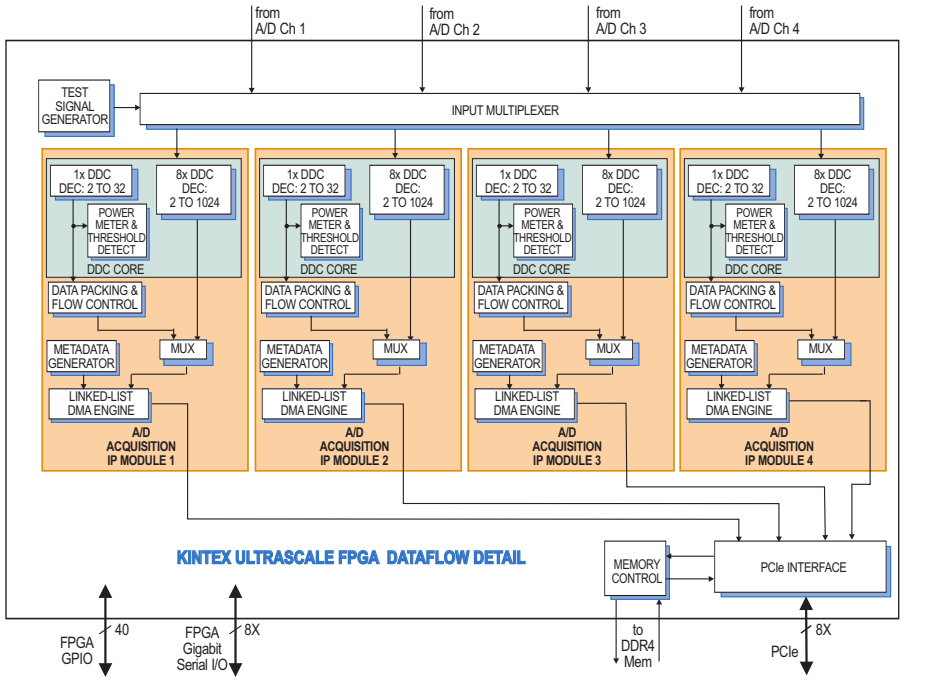
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Model 53862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

➤ Fabric-Transparent Crossbar Switch

The 53862 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

PCI Express Interface

The Model 53862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

SPARK Development Systems

Ordering Information

Model	Description
53862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Four banks, 8 channels per bank
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
- **In all Cases Relative Humidity:** 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 53800

Kintex UltraScale FPGA Coprocessor- 3U VPX

Model 5380 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex Ultra-Scale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 53800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 53800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

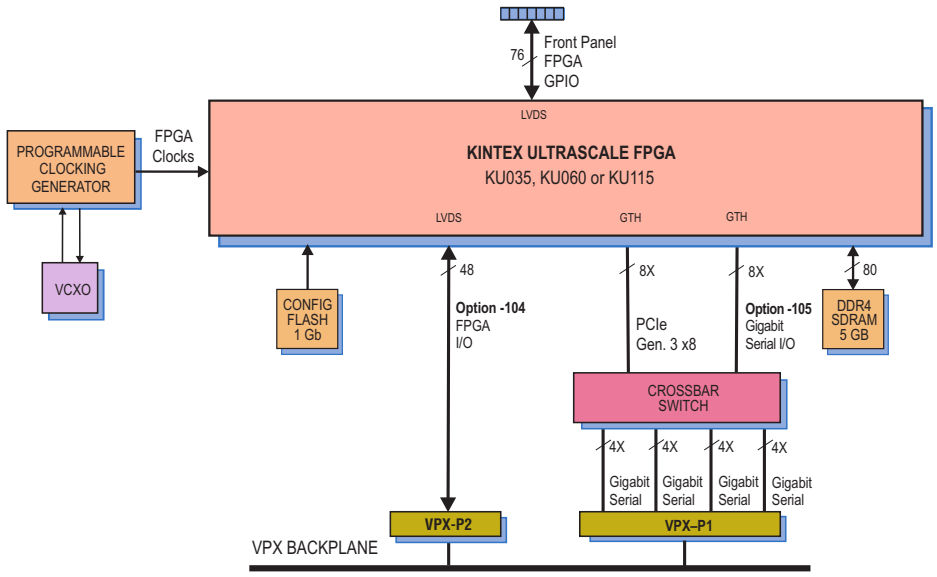
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Front Panel Digital I/O Interface

The 53800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 53800

Kintex UltraScale FPGA Coprocessor- 3U VPX

➤ Interfaces and Memory

The Model 53800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The 53800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Crossbar Switch

The 53800 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable input equalization and output pre-emphasis settings enable optimization.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

SPARK Development Systems

Ordering Information

Model	Description
53800	Kintex UltraScale FPGA Coprocessor - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity in all options:** 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

VPX Families

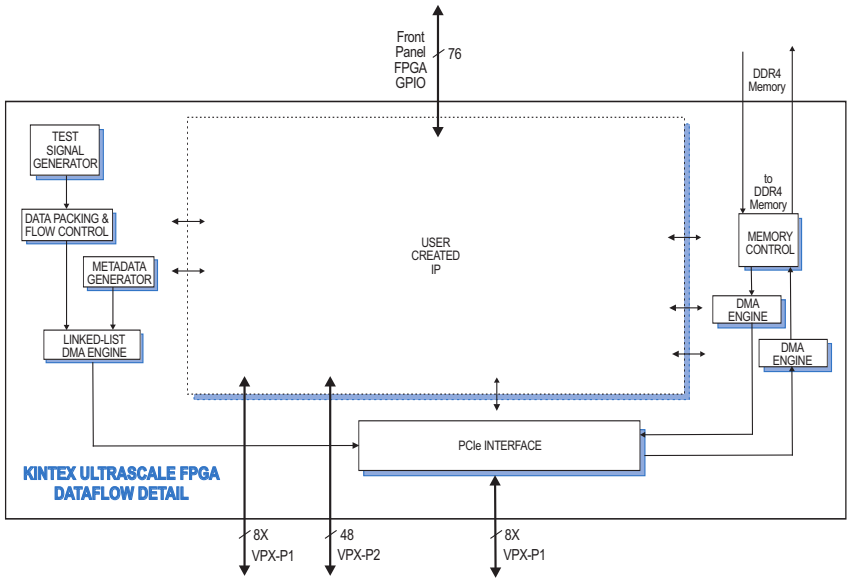
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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New!

Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 9-slot, 4U 19-inch rackmount, 12-inch deep chassis which houses 3U VPX boards
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box ready-to-run examples

Ordering Information

Model	Description
8267	3U VPX Development System for Cobalt, Onyx and Flexor Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS
-101	Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

General Information

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies gurantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

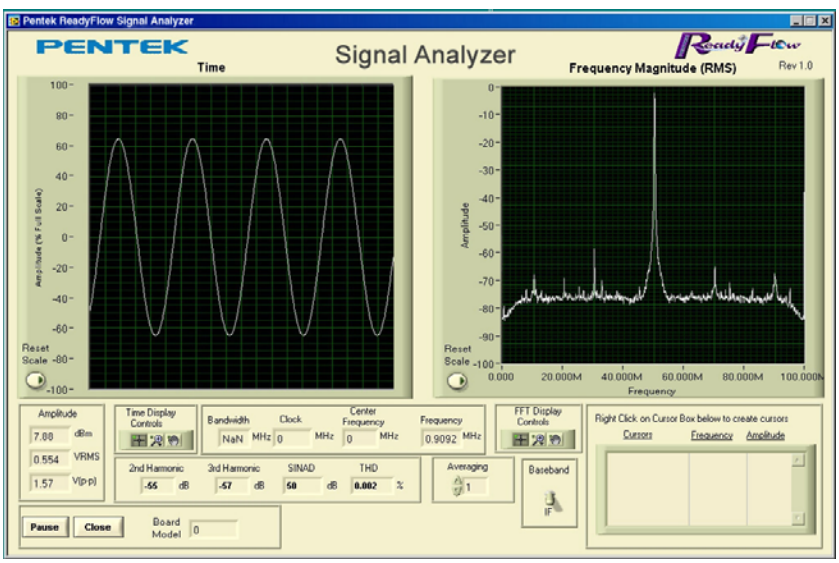
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and extended memory support.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19" W x 12" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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RADAR & SDR I/O - AMC

MODEL	DESCRIPTION
Cobalt 56620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC
Cobalt 56621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC
Cobalt 56624	Dual-Channel, 34-Signal Adaptive IF Relay - AMC
Cobalt 56630	1 GHz A/D and D/A, Virtex-6 FPGA - AMC
Cobalt 56640	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - AMC
Cobalt 56641	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Wideband DDC, Virtex-6 FPGA - AMC
Cobalt 56650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - AMC
Cobalt 56651	2-Chan 500 MHz A/D with DDC, DUC with 2-Chan 800 MHz D/A, Virtex-6 FPGA - AMC
Cobalt 56660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - AMC
Cobalt 56661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC
Cobalt 56662	4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - AMC
Cobalt 56663	1100-Channel GSM Channelizer with Quad A/D - AMC
Cobalt 56664	4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - AMC
Cobalt 56670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC
Cobalt 56671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC
Cobalt 56690	L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC
Onyx 56720	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC
Onyx 56721	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC
Onyx 56730	1 GHz A/D and D/A, Virtex-7 FPGA - AMC
Onyx 56741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC,Virtex-7 FPGA - AMC
Onyx 56751	2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC
Onyx 56760	4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - AMC
Onyx 56761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - AMC
Onyx 56791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC
Jade 51131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA -AMC
Jade 51132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA -AMC
Jade 51141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - AMC
Jade 51821	3-Channel 200 MHz A/D, DDC, DUC 2_Channel 800 MHz D/A, Kintex UltraScale FPGA - AMC
Jade 51841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - AMC
Jade 51851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - AMC
Jade 51861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA -AMC
Jade 51862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - AMC
Jade 56800	Kintex UltraScale FPGA Coprocessor - AMC
Bandit 5620	Two-Channel Analog RF Wideband Downconverter - AMC
	Customer Information

RADAR & SDR I/O - PMC/XMC

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RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated: March 2018

Model 56132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56132 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Eight banks, 8 channels per bank
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front- panel connector for custom I/O

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

Ordering Information

Model	Description
56132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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➤ module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56620 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

General Information

Model 56621 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56621 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

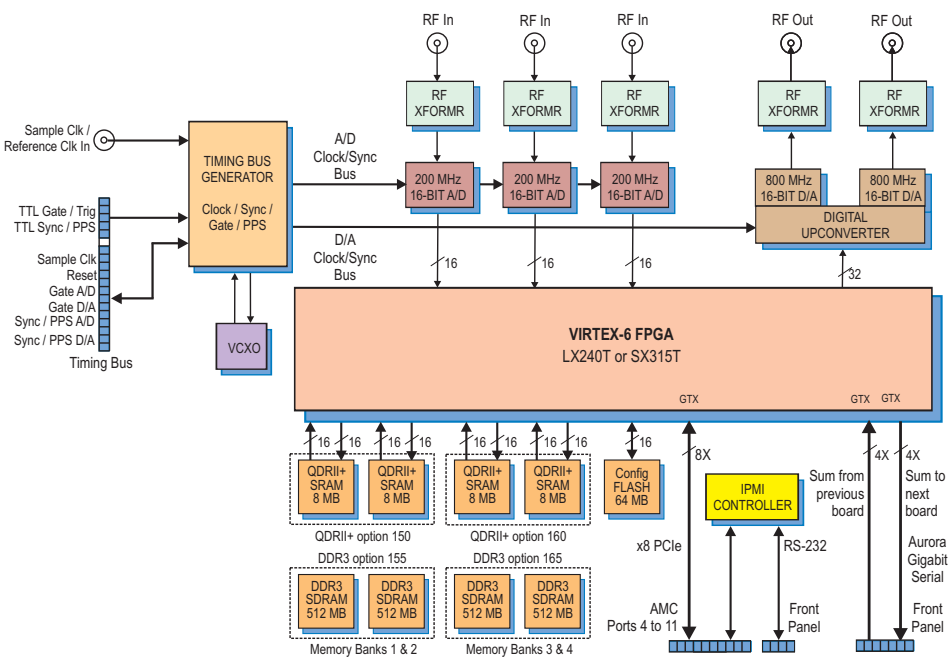
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 56621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

A/D Acquisition IP Modules

The 56621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

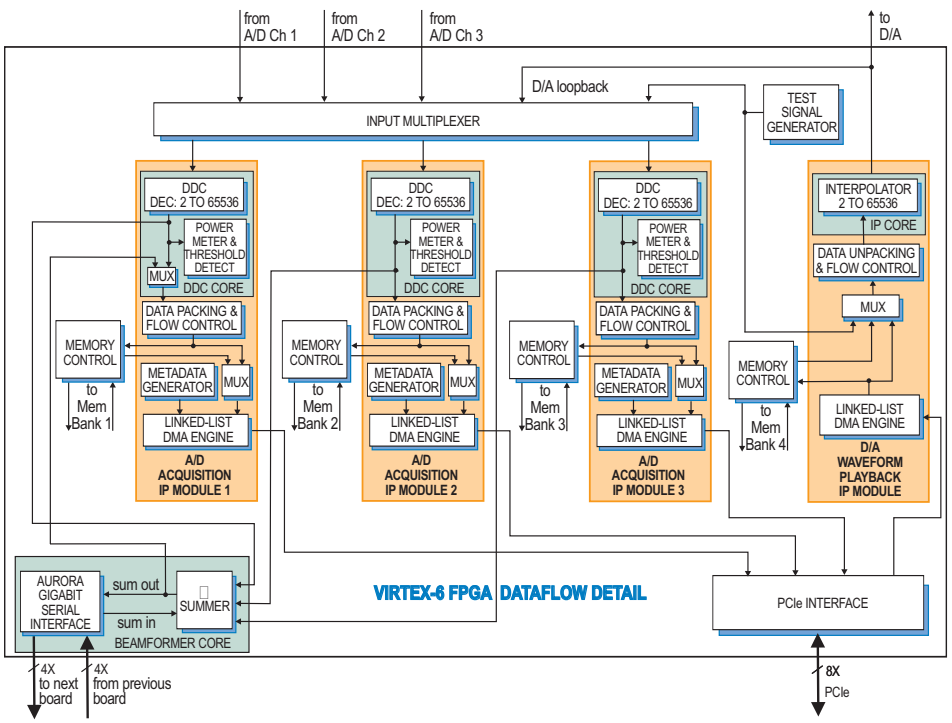
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56621's can be chained together via a built-in Xilinx Aurora gigabit serial interface which allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 56621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56621 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 56621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

Options:

-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 56624

Dual-Channel, 34-Signal Adaptive IF Relay - AMC

Features

- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/As
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

General Information

Model 56624 is a member of the Cobalt® family of high-performance AMC boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 56624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 56624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

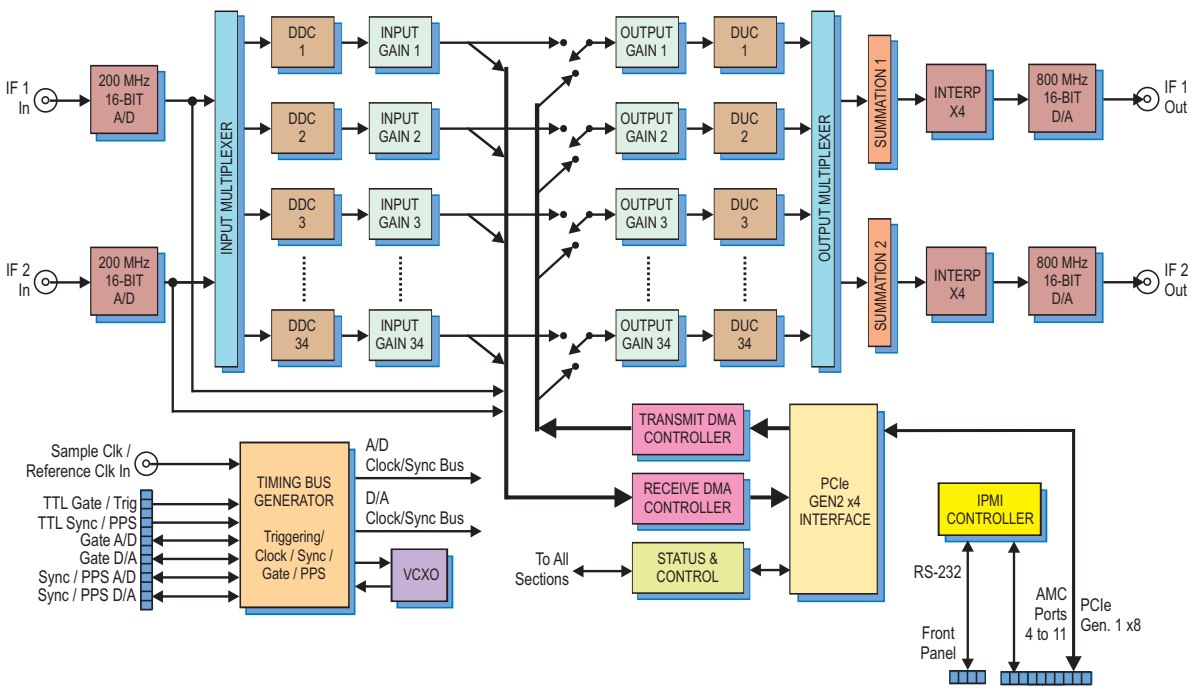
Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 56624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two summation blocks, each ➤



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➤ associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 56624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 56624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 56624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz. ➤

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56624's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

AMC Interface

The Model 56624 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

Model 56624 — Dual-Channel, 34-Signal Adaptive IF Relay - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- **Quantity:** 34
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
- **Quantity:** 34
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Required:** Xilinx Virtex-6 XC6VSX315T

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8

Environmental
- **Standard:**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 702 L2 Extended Temp (air-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 712 L2 Extended Temp (conduction-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56624	Dual-Channel 34-Signal Adaptive IF Relay - AMC

Options:

-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

General Information

Model 56630 is a member of the Cobalt® family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56630 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

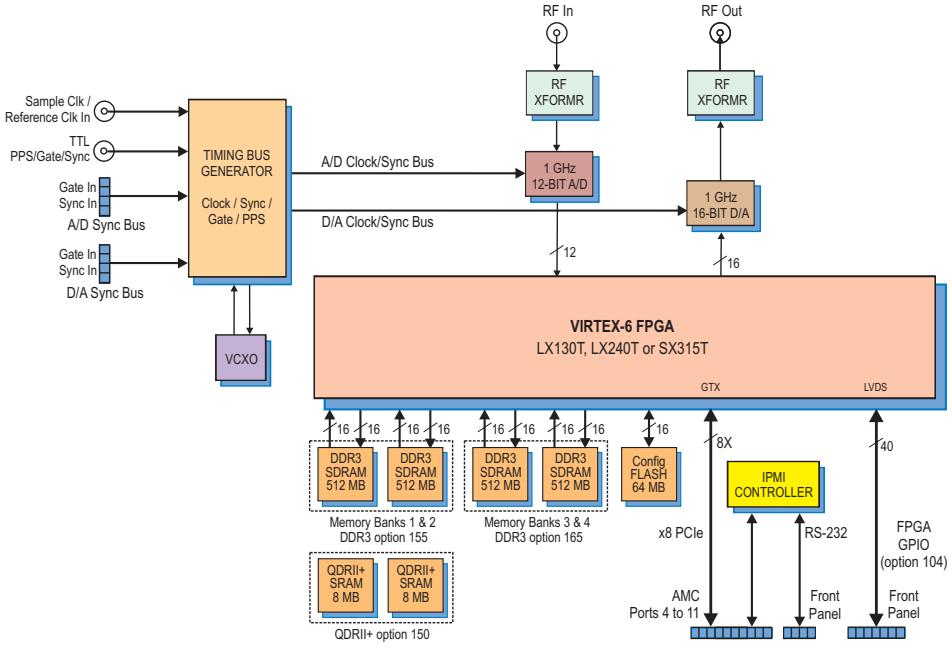
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 56630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

A/D Acquisition IP Module

The 56630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 56630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

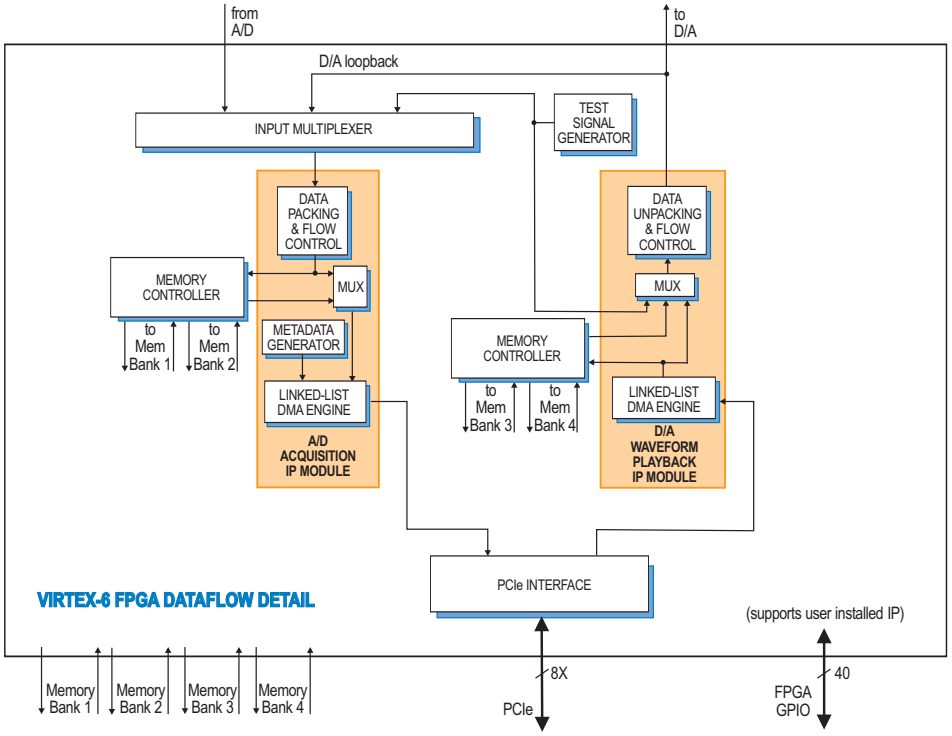
A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 5692 and Model 9192 Cobalt Synchronizers can drive multiple 53730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 56630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Model 56630 — 1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

➤ AMC Interface

The Model 56630 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen.1: x4 or x8; Gen 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56630	1 GHz A/D and D/A, Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

General Information

Model 56640 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56640 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

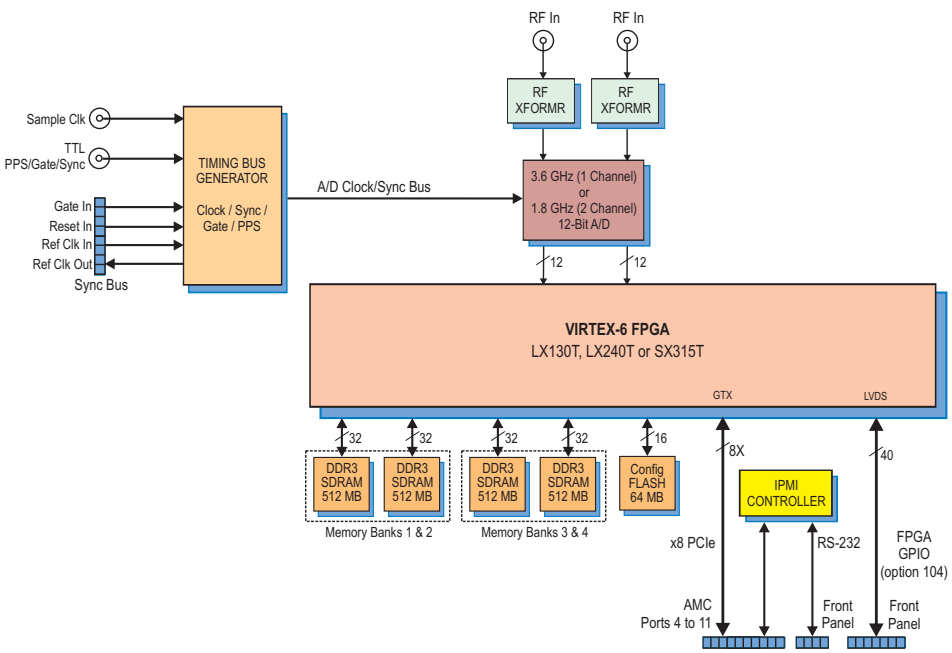
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 56640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 56640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 56640's can be synchronized using the Cobalt high speed sync module to drive the sync bus.

Memory Resources

The 56640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

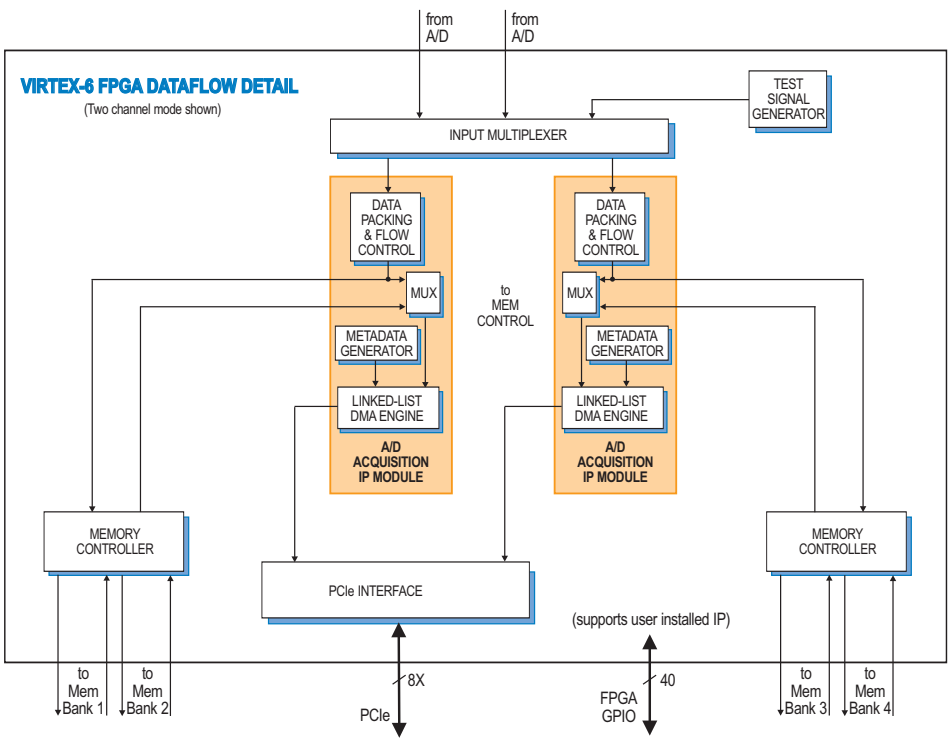
The Model 56640 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ➤

A/D Acquisition IP Module

The 56640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 56640 — 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

➤ PCI Express Interface

The Model 56640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

General Information

Model 56641 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56641 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

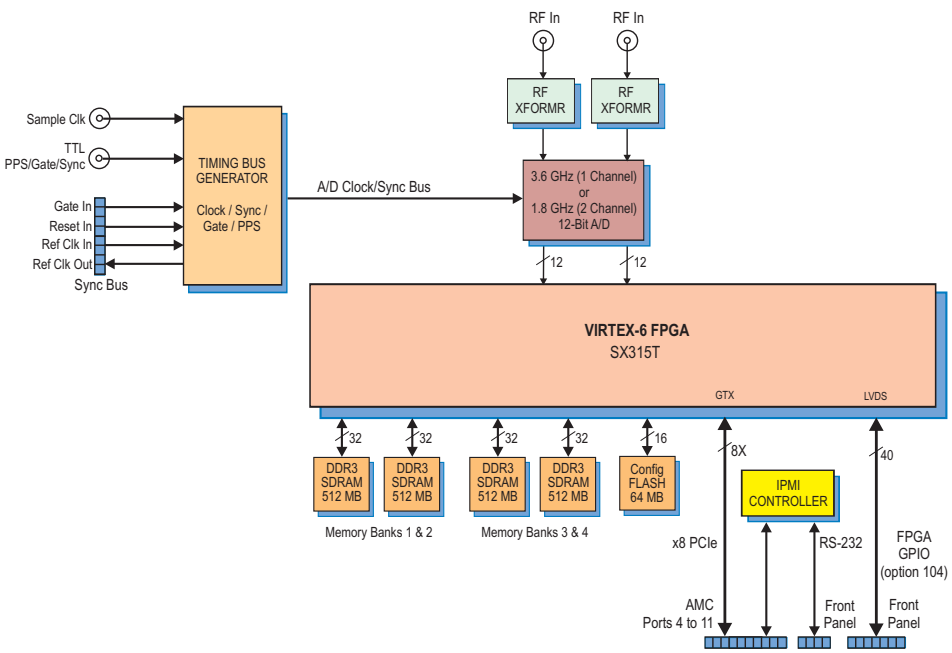
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 56641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

A/D Acquisition IP Module

The 56641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

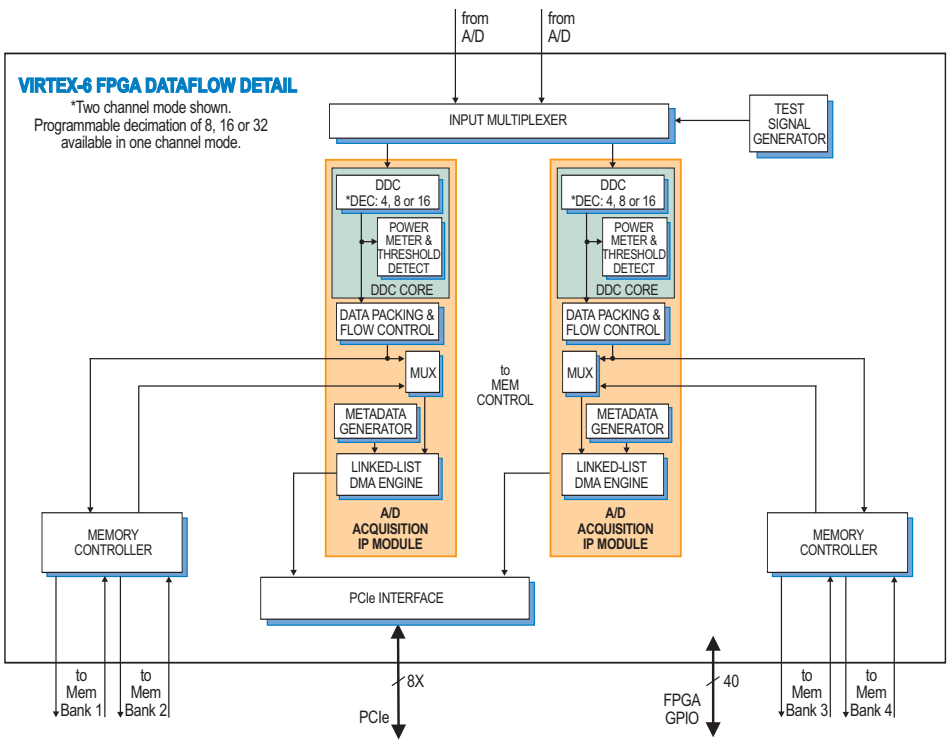
➤ Clocking and Synchronization

The 56641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 56641's can be synchronized with a simple cable. For larger systems, multiple 56641's can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

Memory Resources

The 56641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Model 56641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

➤ AMC Interface

The Model 56641 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin front panel connector, includes gate, reset, and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include trigger and gate

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - AMC

General Information

Model 56650 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56650 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

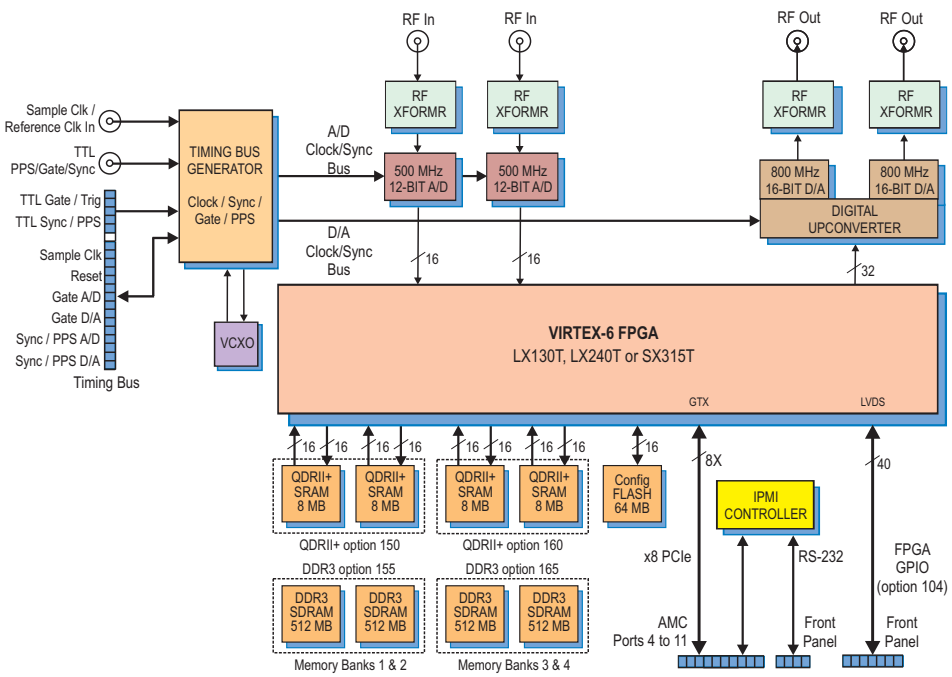
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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A/D Acquisition IP Modules

The 56650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

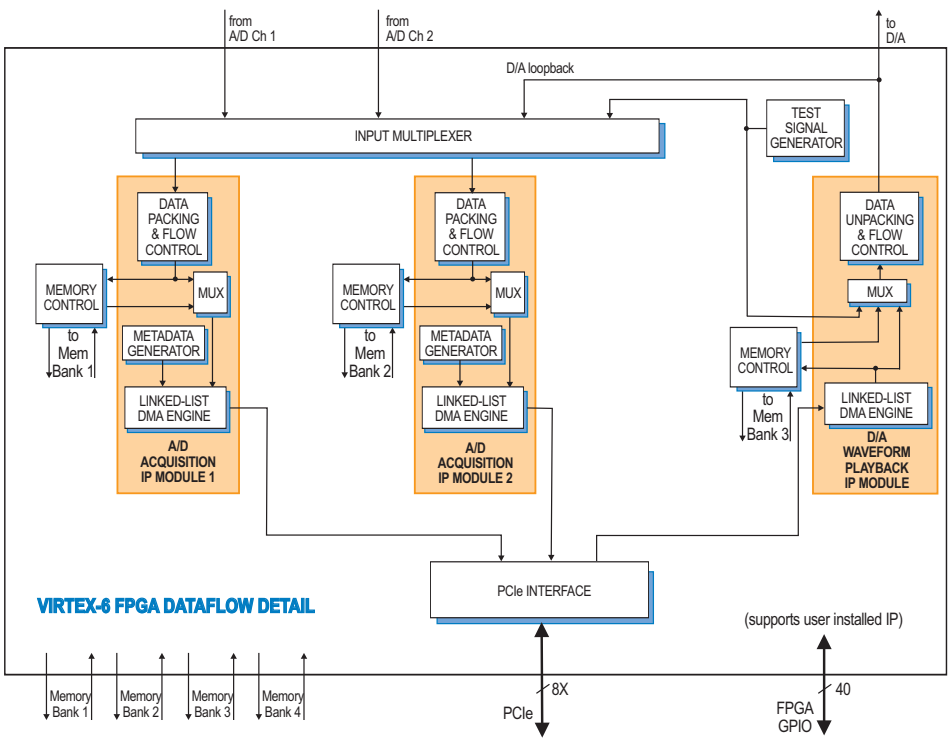
A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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➤ module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56650 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option 014)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen.1 or Gen.2, x4 or x8

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56650	Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240 FPGA
-064	XC6VSX315 FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

General Information

Model 56651 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56651 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56651 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

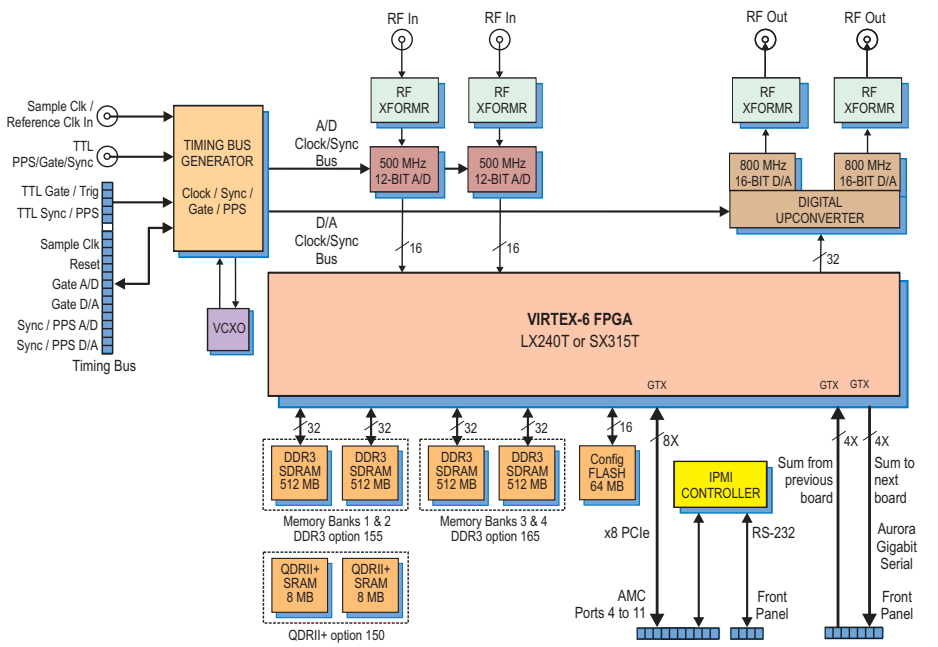
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

A/D Acquisition IP Modules

The 56651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

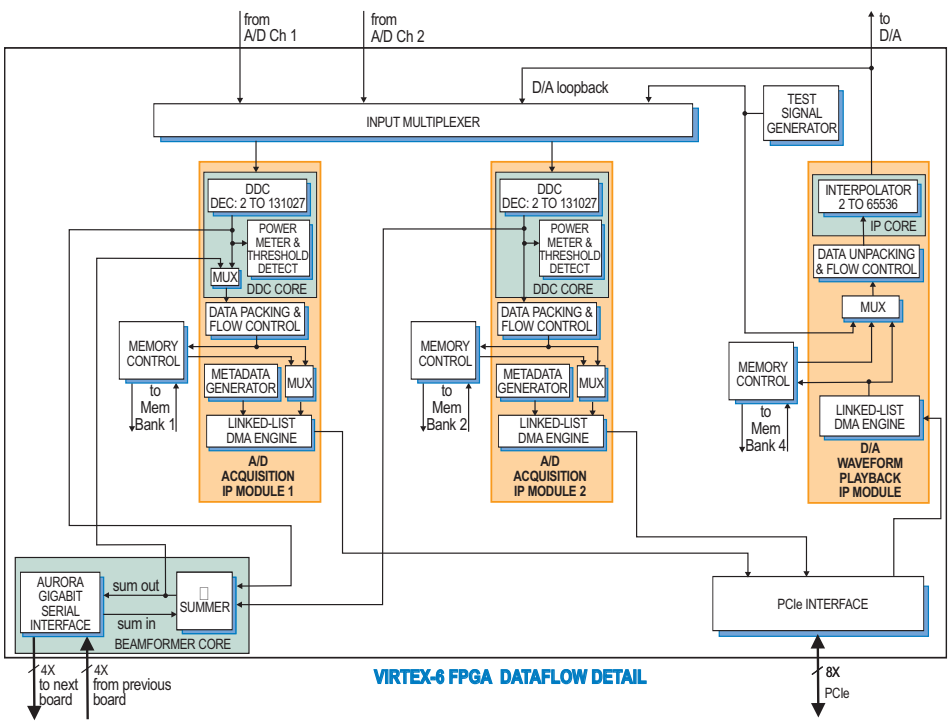
A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56651's can be chained together via a built-in Xilinx Aurora gigabit serial interface to allow summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 56651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

➤ A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56651 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56651 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 56651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option -150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option -155 or -165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 2: x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

General Information

Model 56660 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56660 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

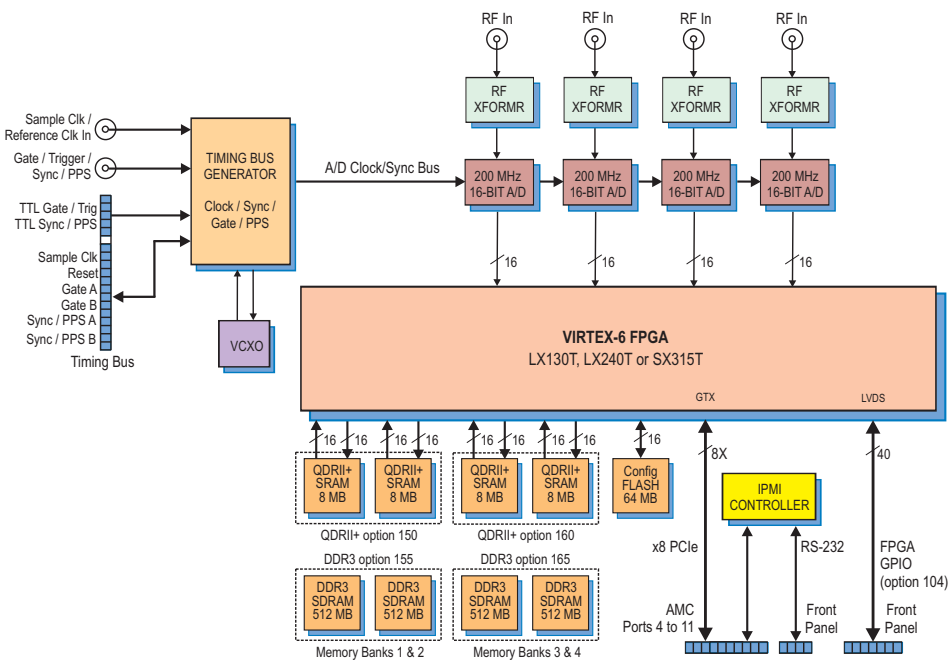
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

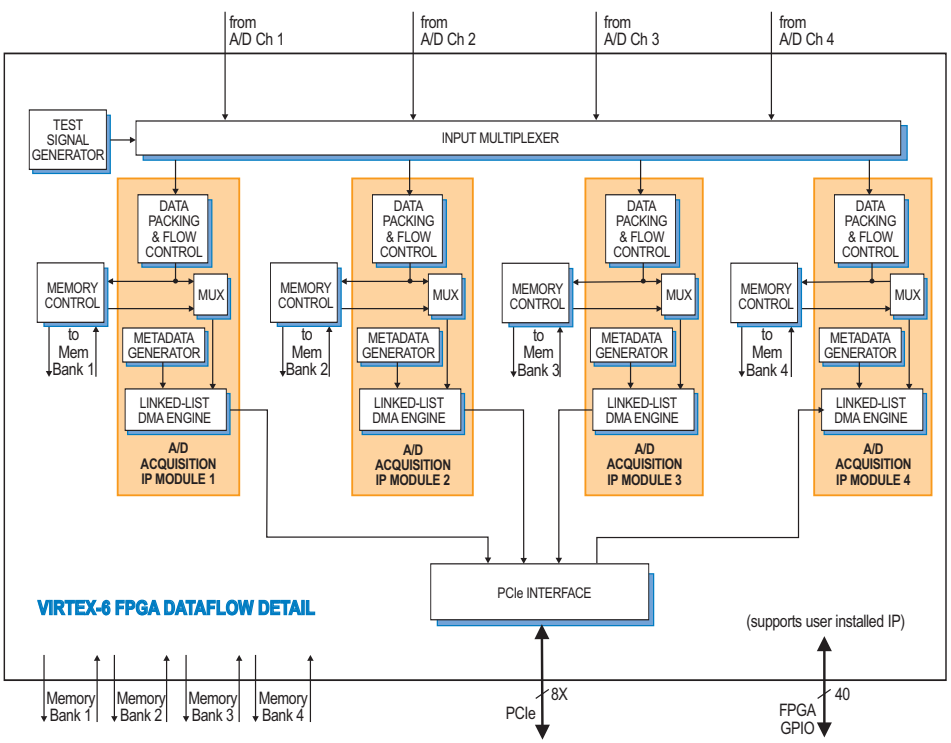
The Model 56660 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ➤

A/D Acquisition IP Modules

The 56660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 56660 — 4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

➤ PCI Express Interface

The Model 56660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56660	4-Channel 200 MHz A/D with Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC

General Information

Model 56661 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56661 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

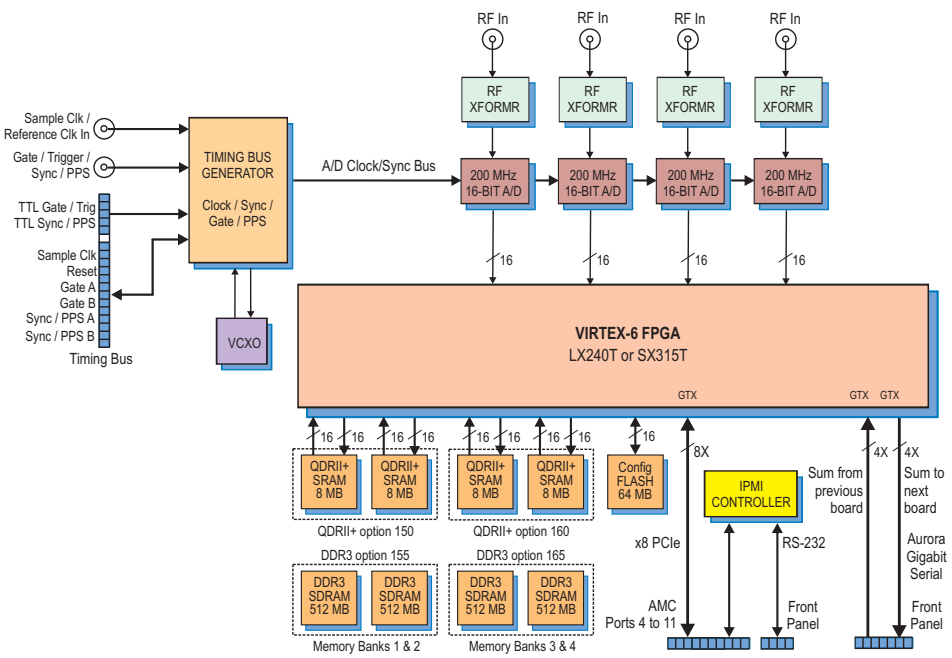
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC

A/D Acquisition IP Modules

The 56661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

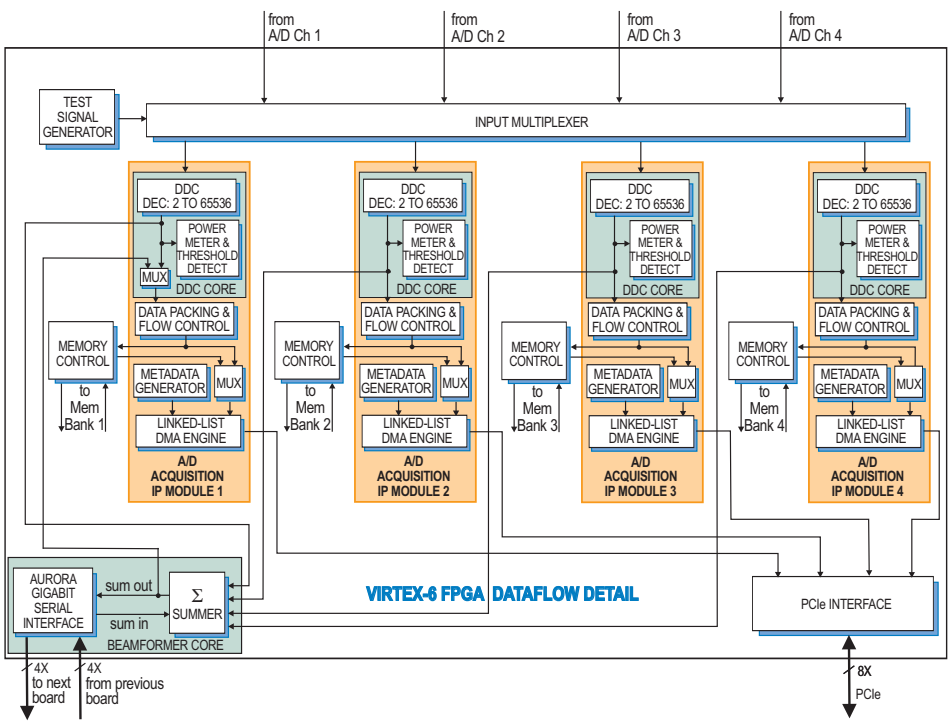
➤ A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56661 — 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC

AMC Interface

The Model 56661 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

Model	Description
56661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

➤ mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56661's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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Model 56662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 56662 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56662 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 56662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

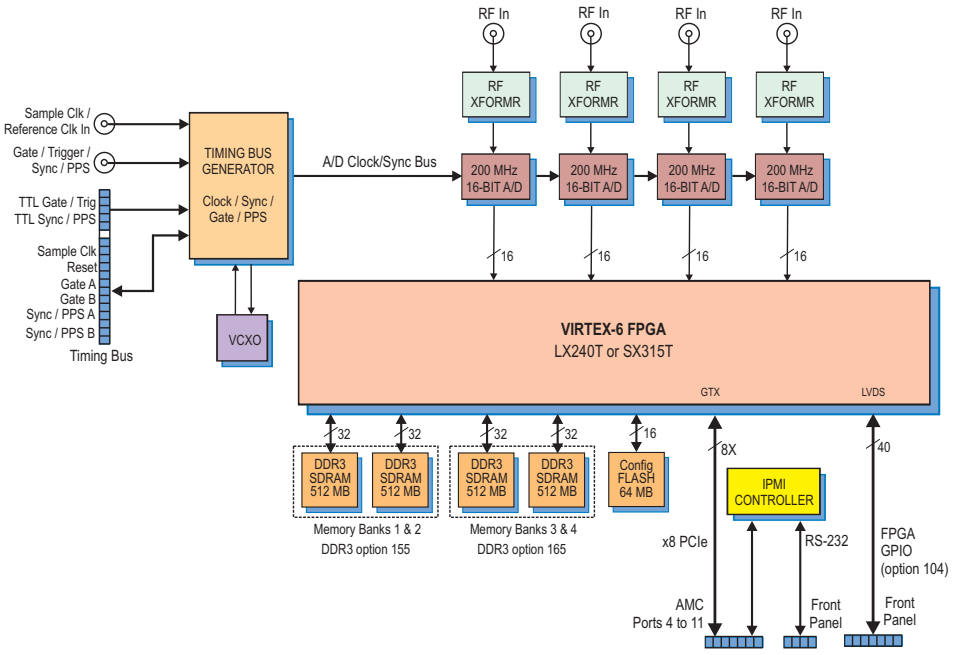
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



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Model 56662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC

A/D Acquisition IP Modules

The 56662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

➤ A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

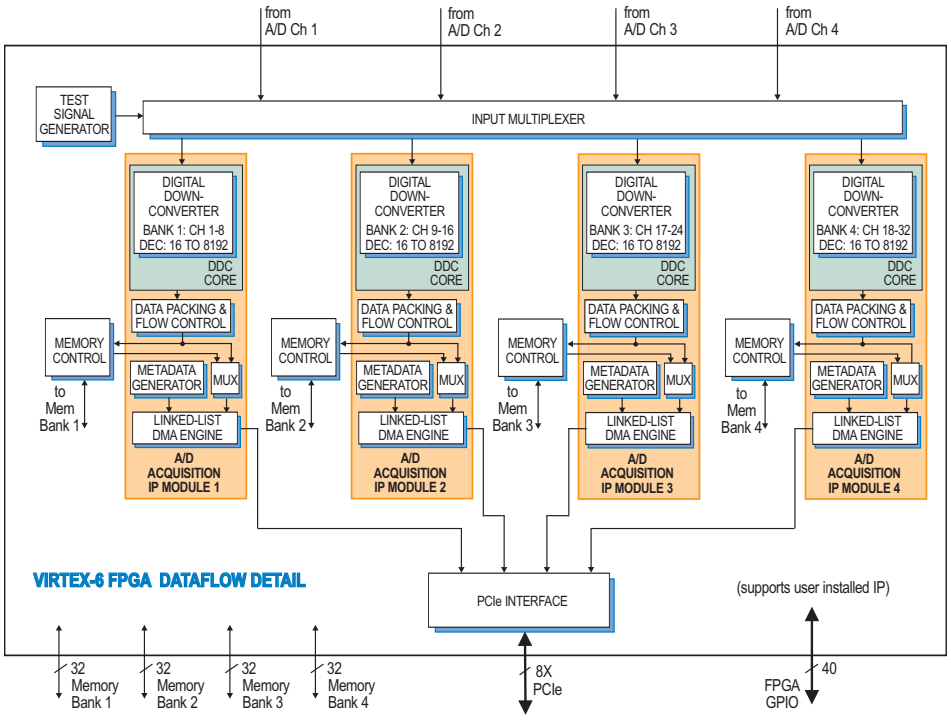
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM. ➤



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Model 56662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56662 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of ruged and conduction-cooled versions

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Model 56663

1100-Channel GSM Channelizer with Quad A/D - AMC

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express Gen. 2 x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)

General Information

Model 56663 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 56663 is a complete, full-featured subsystem, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

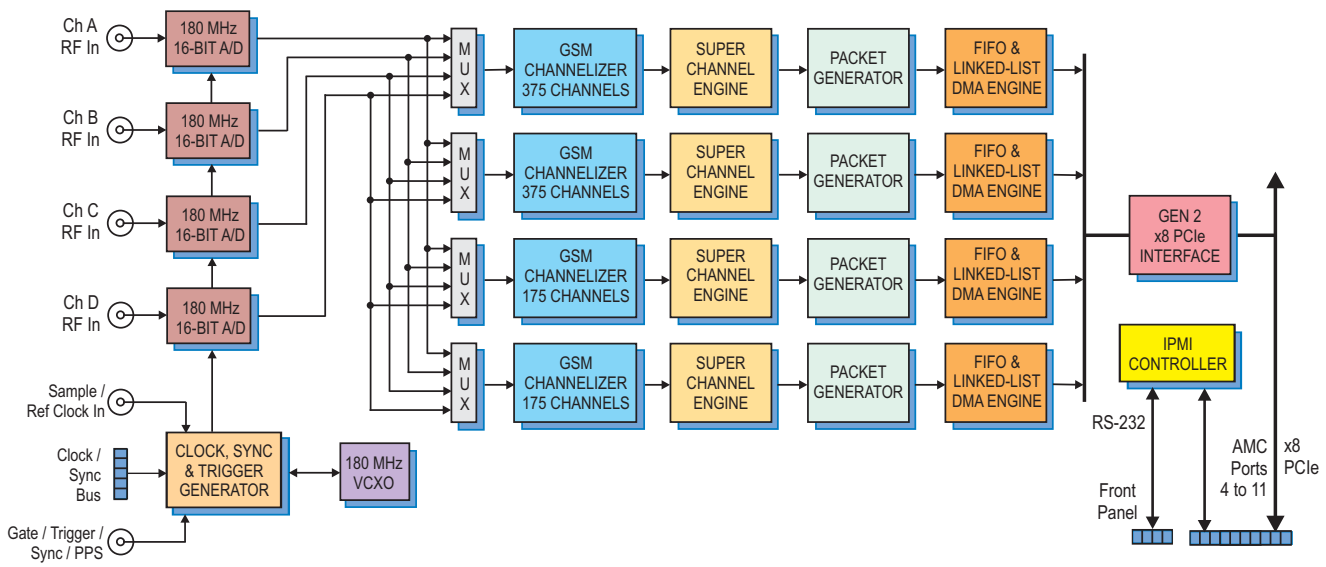
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

GSM Channelizer Cores

The 56663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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➤ The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 56663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 56663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI Express Interface

The Model 56663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 56663 and host.

AMC Interface

The Model 56663 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ➤

Model 56663 — 1100-Channel GSM Channelizer with Quad A/D - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: $-f_s/4$ (-270.8333 kHz)
  - Second: 0 Hz
  - Third: $+f_s/4$ (+270.8333 kHz)
  - Fourth: $+f_s/2$ (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56663	1100-Channel GSM Channelizer with Quad A/D - AMC

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - AMC

General Information

Model 56664 is a member of the Cobalt family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 56664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56664 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

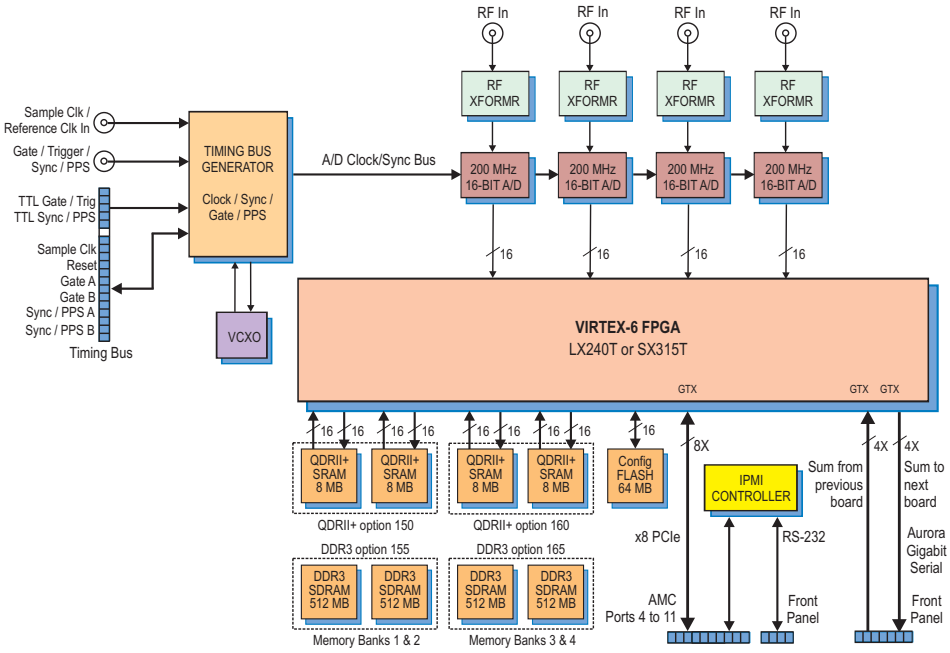
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 56664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - AMC

A/D Acquisition IP Modules

The 56664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56664 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

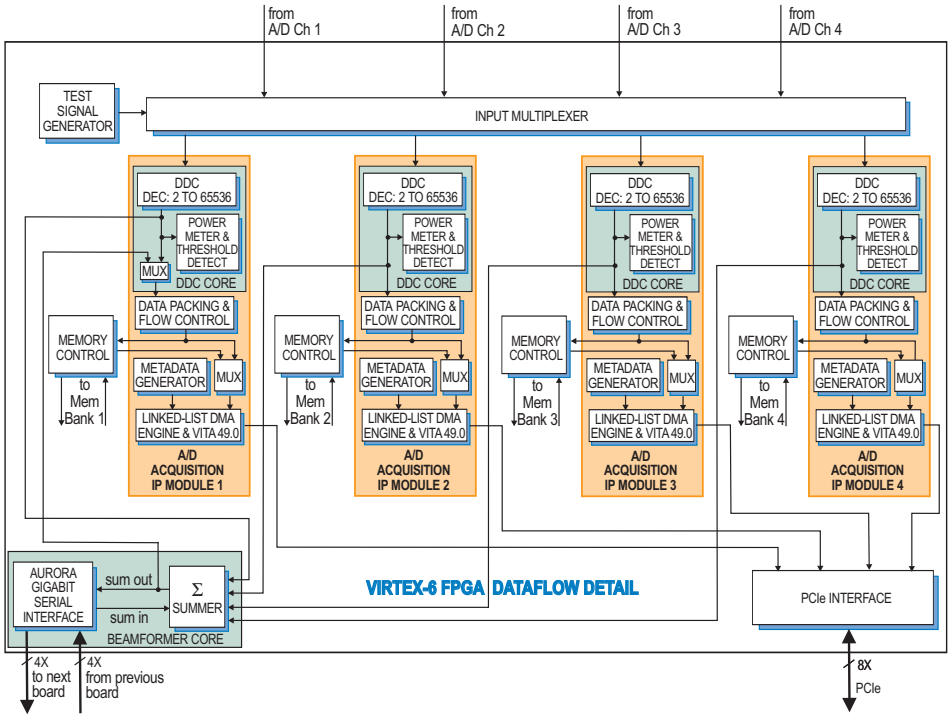
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56664's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 56664 supports fully the VITA 49.0 specification. ➤



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➤ A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56664's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56664 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

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Model 56664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in. ➤

Ordering Information

Model	Description
56664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 56670 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

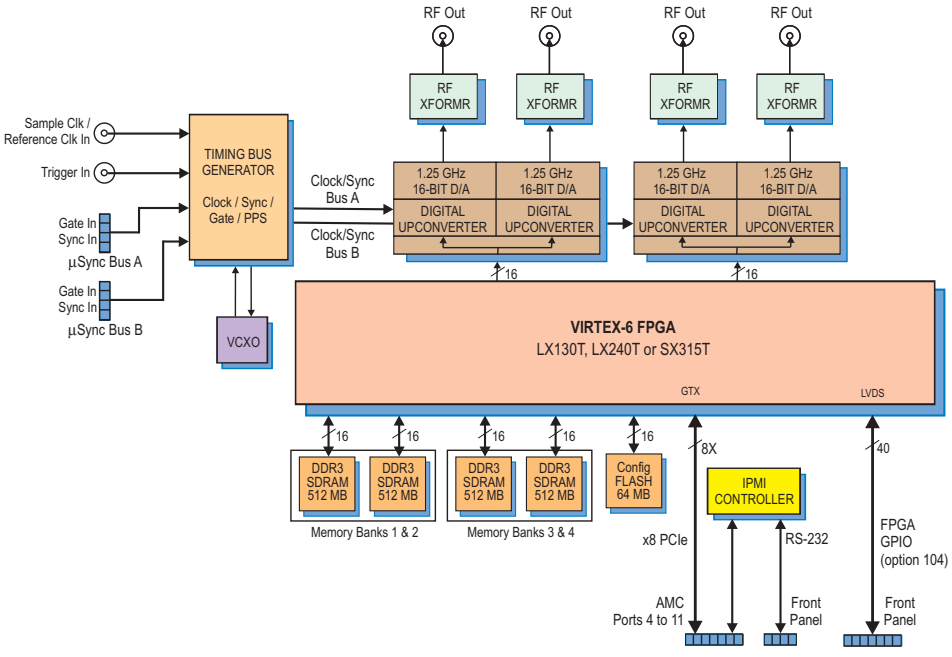
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



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4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5692 or 9192 Cobalt Synchronizers can drive multiple 56670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 56670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

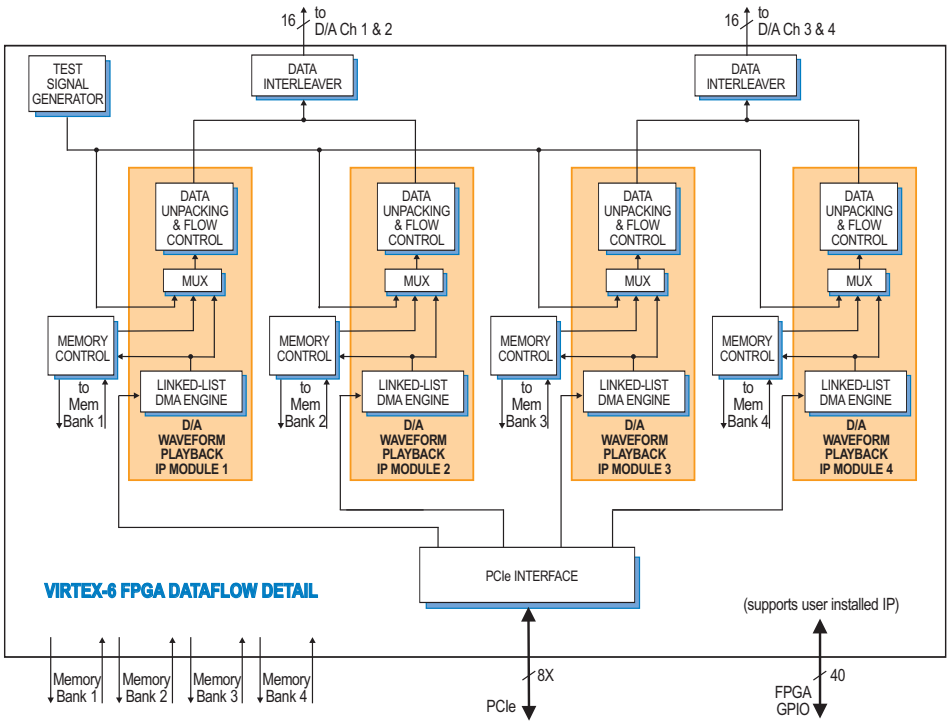
The Model 56670 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ➤

D/A Waveform Playback IP Module

The Model 56670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Model 56670 — 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

➤ PCI Express Interface

The Model 56670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC

General Information

Model 56671 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56671 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

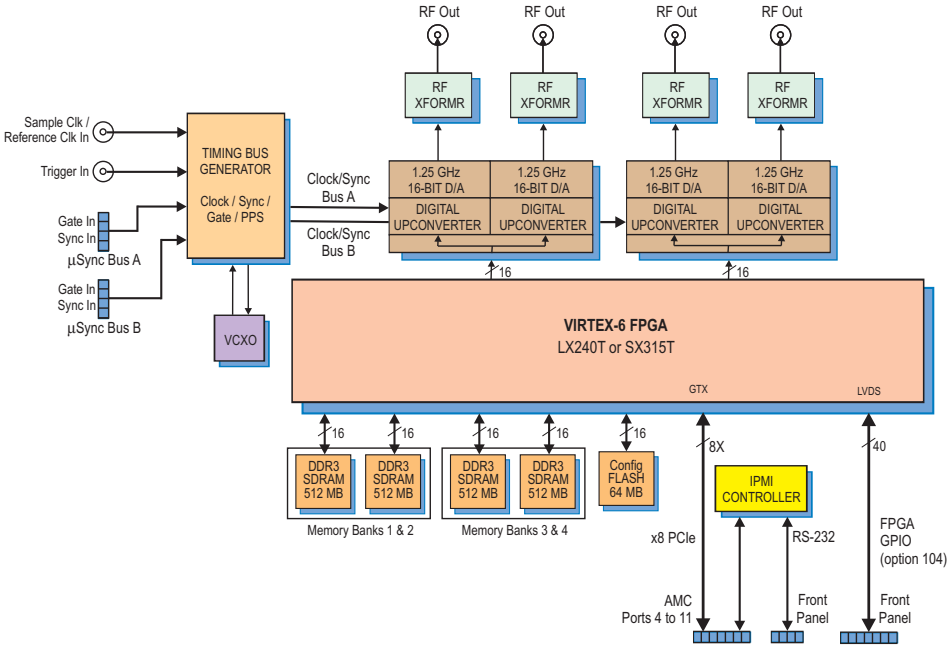
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Model 56671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 56671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5692 or 9192 Cobalt Synchronizers can drive multiple 56671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 56671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

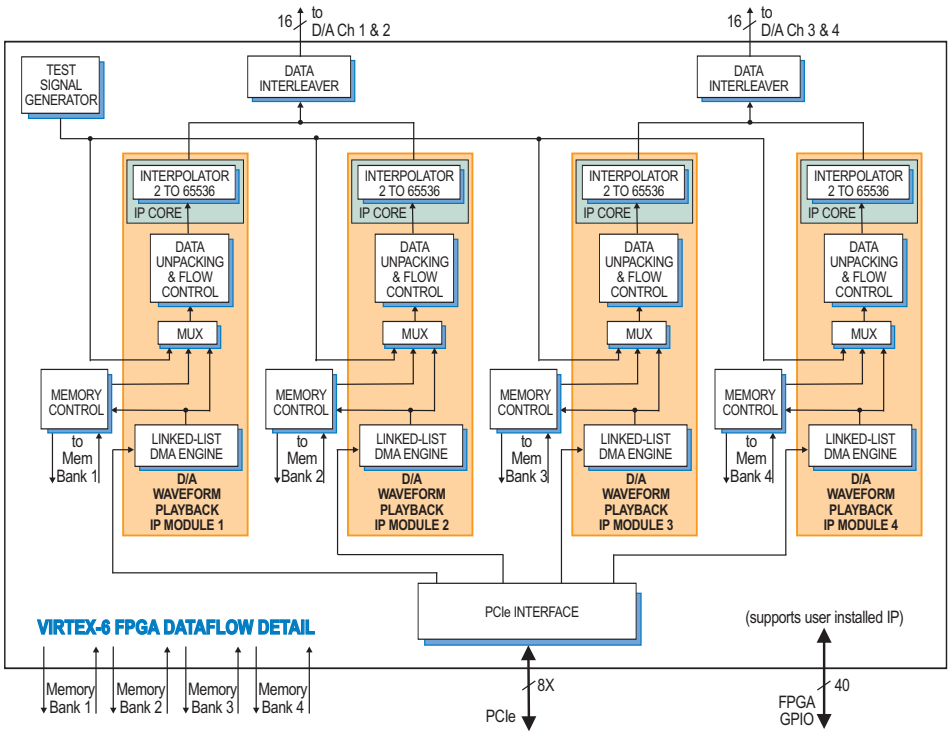
D/A Waveform Playback IP Module

The Model 56671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Model 56671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC

➤ AMC Interface

The Model 56671 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds digitize the I + Q signals synchronously
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 56690 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56690 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

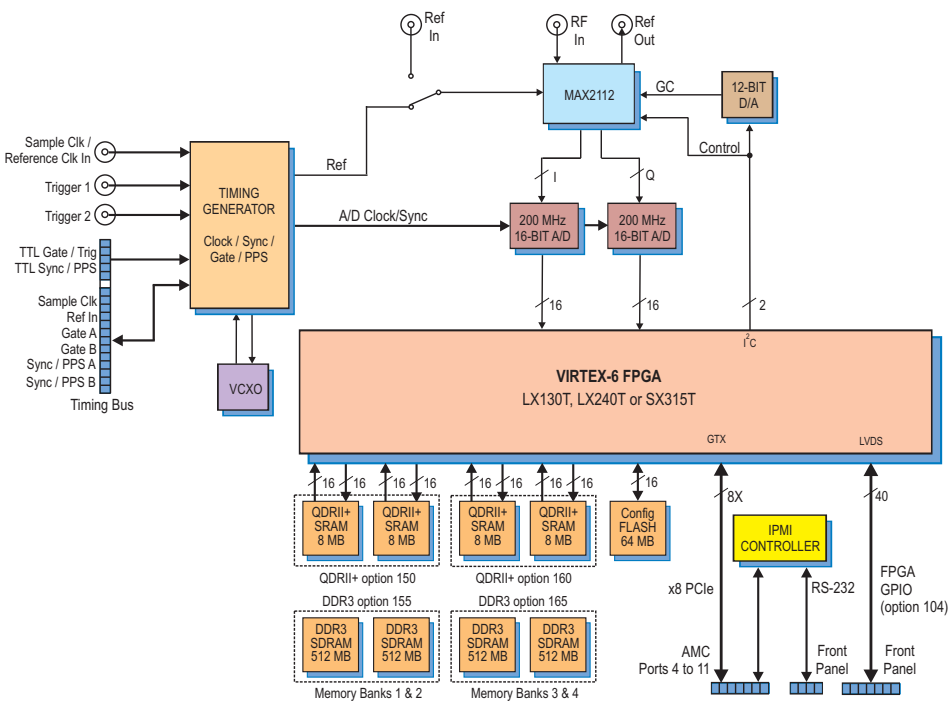
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



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L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC

➤ RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

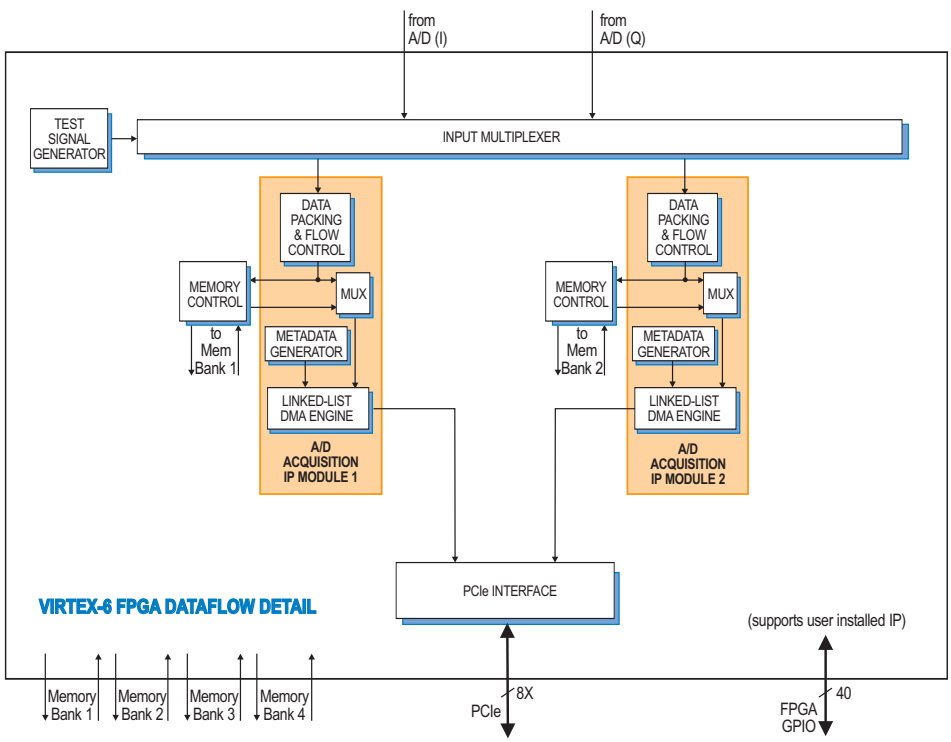
The 56690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤

A/D Acquisition IP Modules

The 56690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

AMC Interface

The Model 56690 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- ***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2 x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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Model 56720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - AMC

General Information

Model 56720 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56720 includes a front panel general-purpose connector for application-specific I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56760 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56720 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

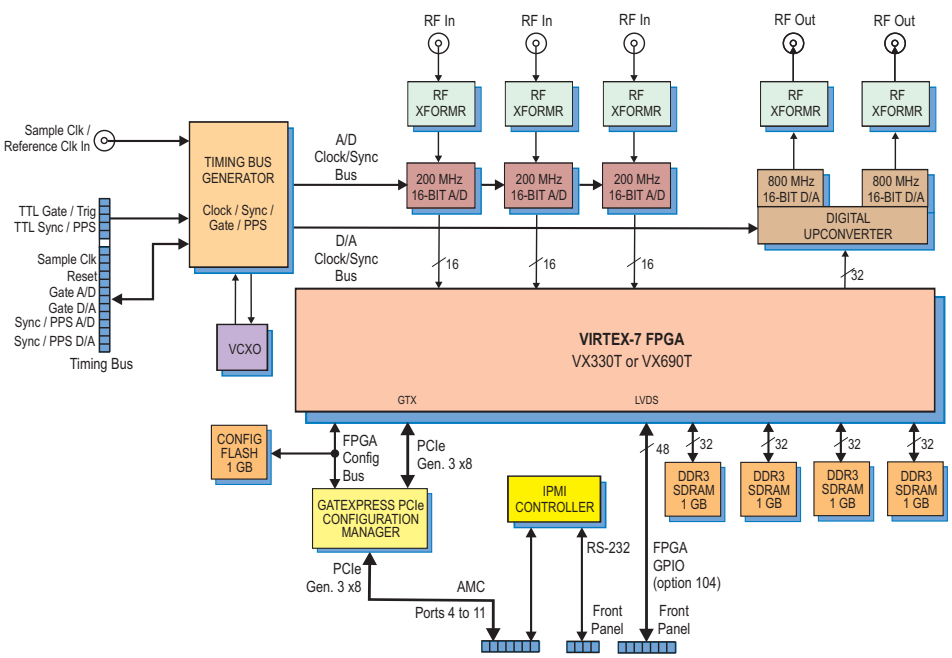
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - AMC

A/D Acquisition IP Modules

The 56720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

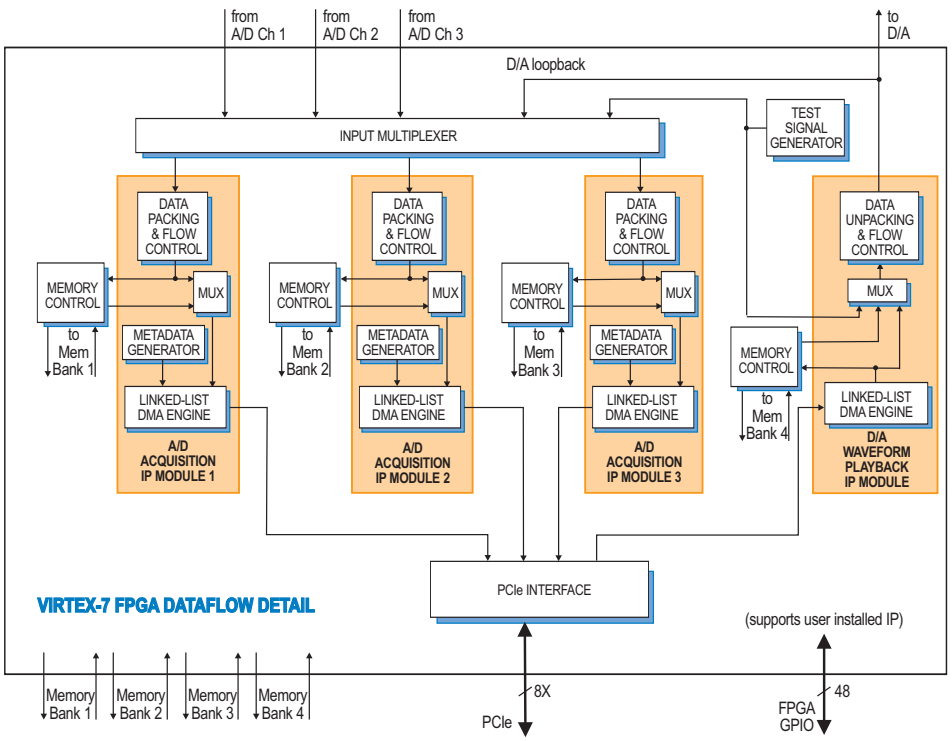
A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56720 — 3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - AMC

Memory Resources

The 56720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56720 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

Model	Description
56720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - AMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through front panel connector

Contact Pentek for availability of rugged and conduction-cooled versions

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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Model 56721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC

General Information

Model 56721 is a member of the Onyx® family of high performance AMC boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for Gen. 1 and 2 PCI Express.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

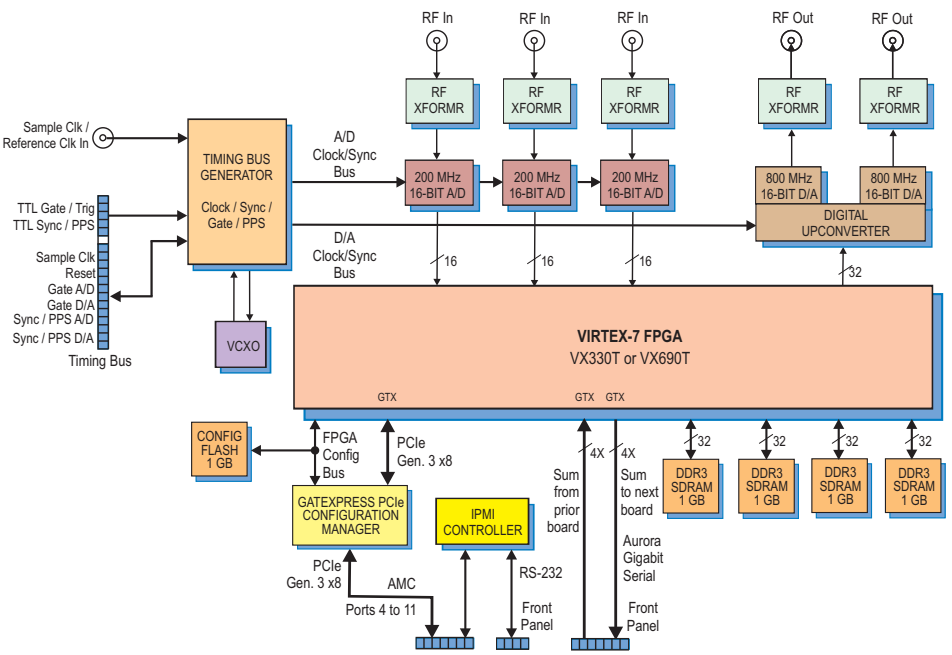
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)



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Model 56721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC

A/D Acquisition IP Modules

The 56721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

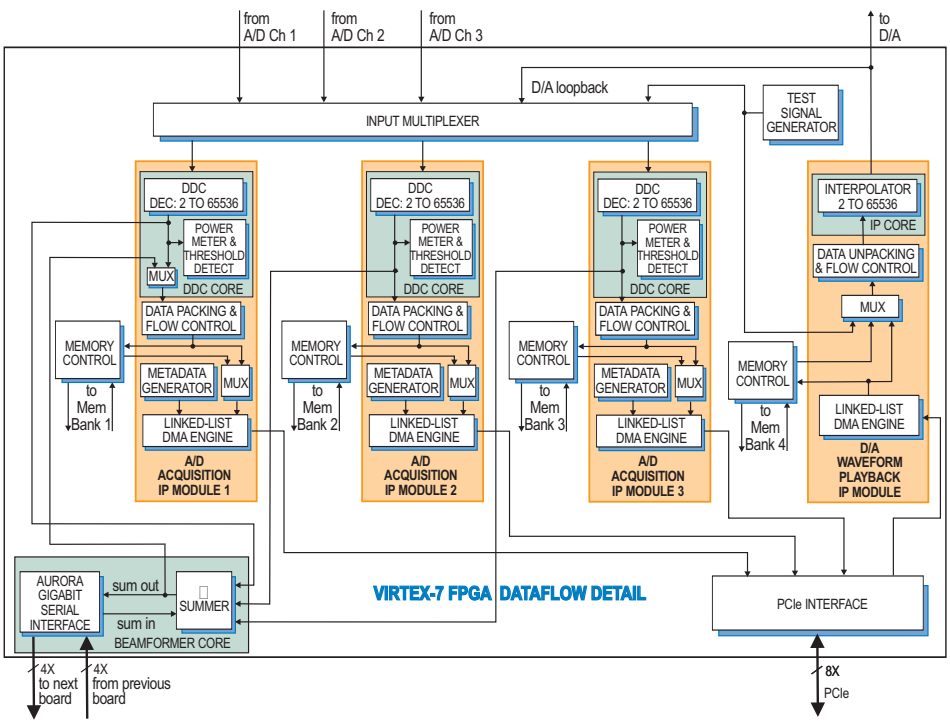
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56721's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 56721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56721's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

AMC Interface

The Model 56721 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ➤

Model 56721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC

➤ Memory Resources

The 56721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56721 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC
Option:	
-076	XC7VX690T-2 FPGA

Contact Pentek for availability of rugged and conduction-cooled versions

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - AMC

General Information

Model 56730 is a member of the Onyx® family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen.3 as a native interface, the Model 56730 includes a front panel general-purpose connector for application-specific I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

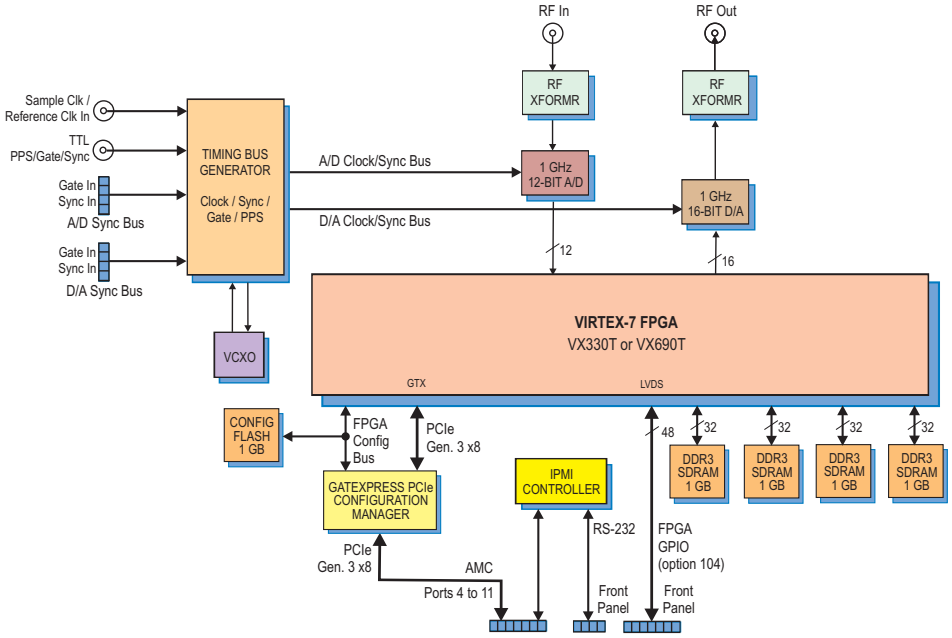
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - AMC

A/D Acquisition IP Module

The 56730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

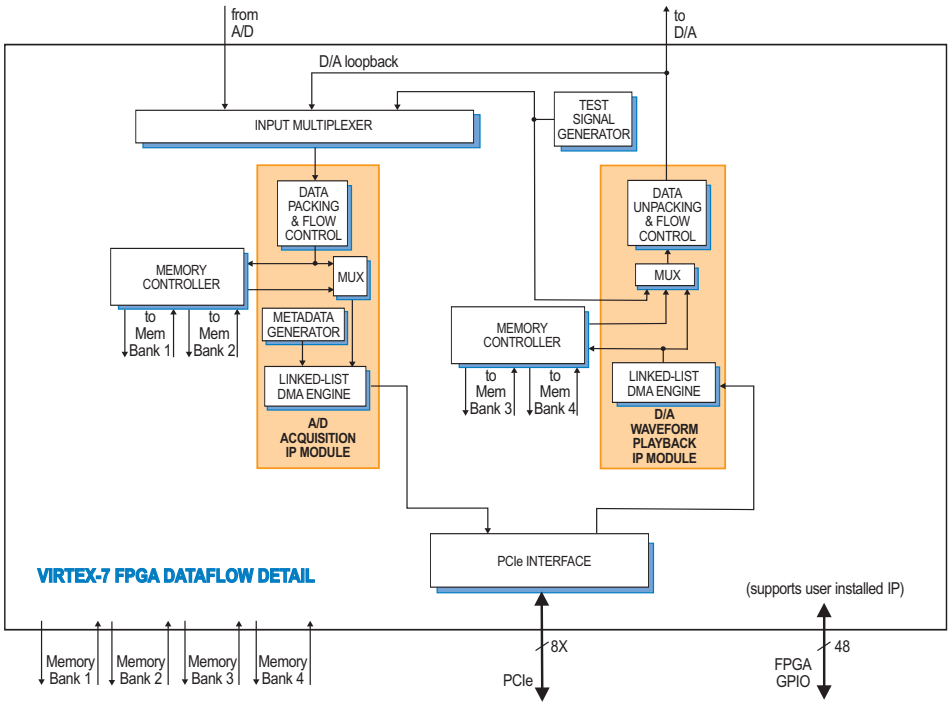
A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 56730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56730 — 1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - AMC

AMC Interface

The Model 56730 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

Model	Description
56730	1 GHz A/D and D/A, Virtex-7 FPGA - AMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to front pannel connector

Contact Pentek for availability of rugged and conduction-cooled versions

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 5692 and Model 9192 Cobalt Synchronizers can drive multiple 56730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 56730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user- installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

General Information

Model 56741 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56741 includes an optional front-panel connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

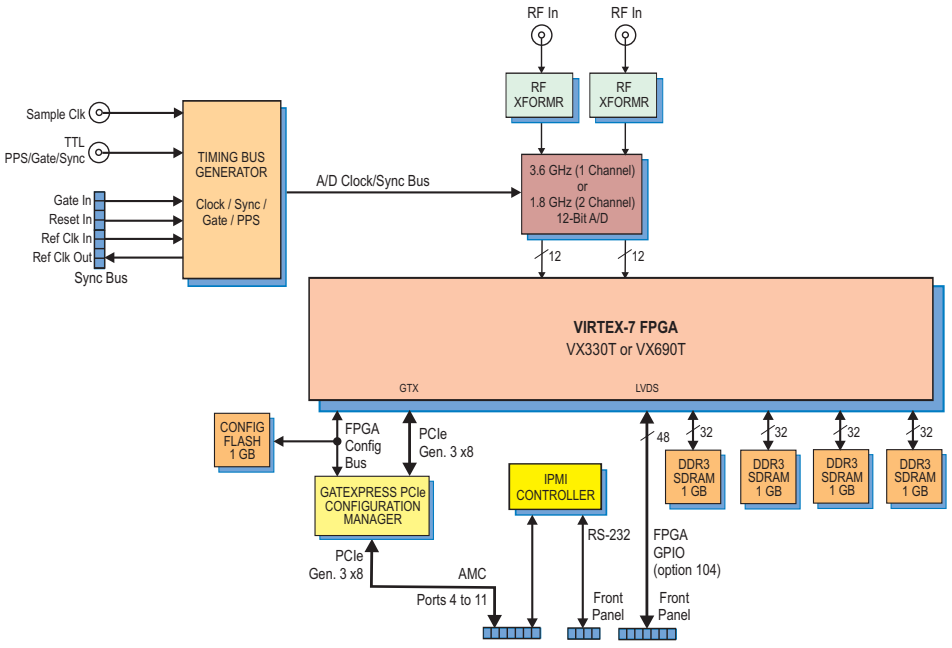
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

A/D Acquisition IP Module

The 56741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

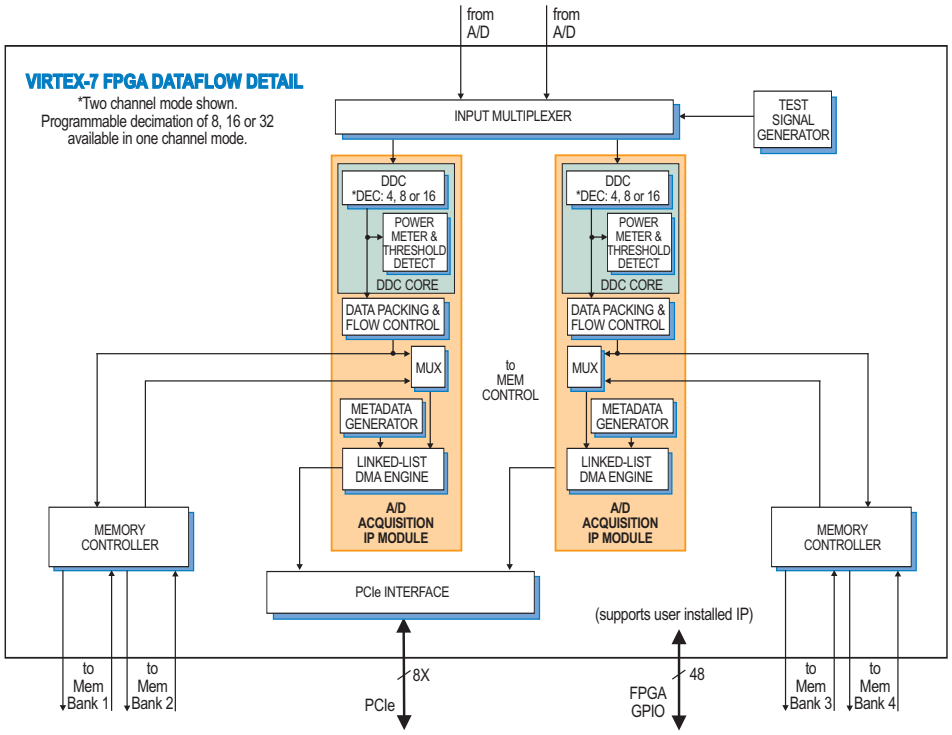
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored ➤



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Model 56741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

Memory Resources

The 56741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

AMC Interface

The Model 56741 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

Model	Description
56741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - AMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to front panel connector

Contact Pentek for availability of rugged and conduction-cooled versions

➤ on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 56741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boardss.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

The 56741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 56741's can be synchronized with a simple cable. For larger systems, multiple 56741's can be synchronized using the Model 5692 high-speed sync board to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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Model 56751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC

General Information

Model 56751 is a member of the Onyx® family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56751 includes a general-purpose front-panel connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

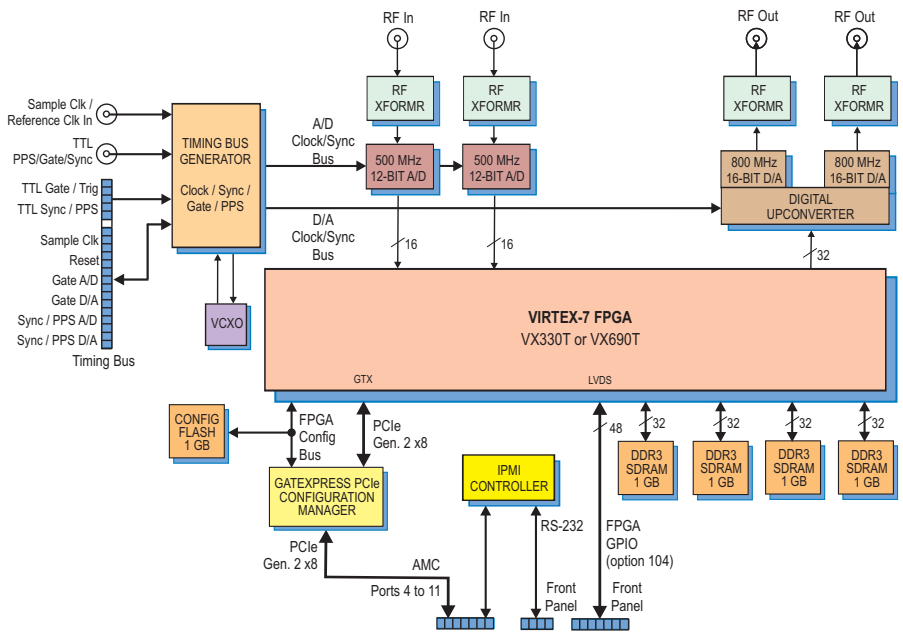
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds



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Model 56751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC

A/D Acquisition IP Modules

The 56751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 56751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

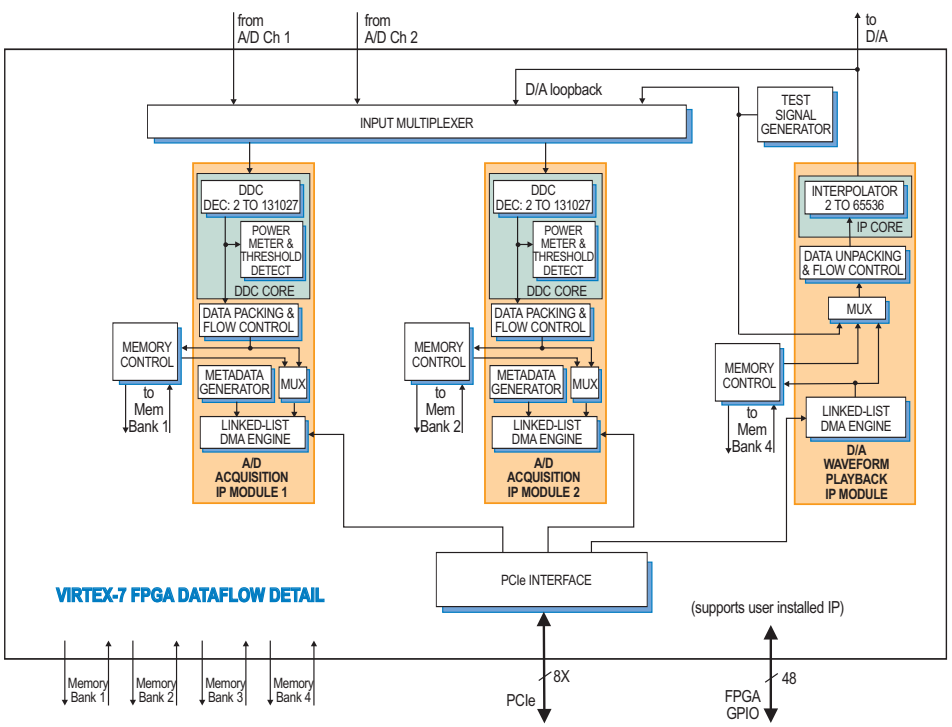
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56751's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56650 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56751 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

Model 56751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen.1 or Gen.2, x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - AMC
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - AMC

General Information

Model 56760 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56760 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

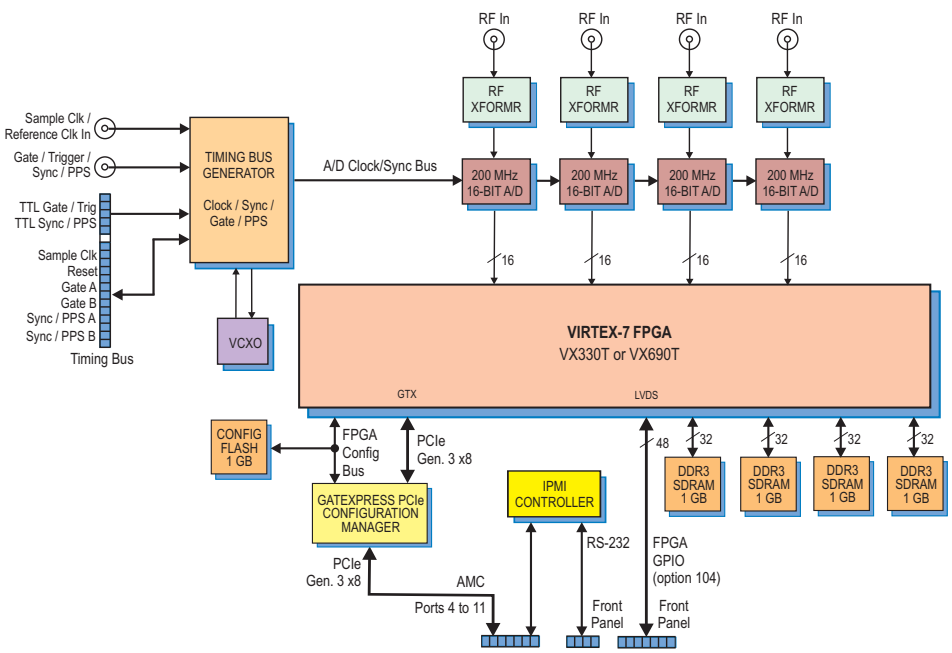
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-7 FPGA for custom I/O



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➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

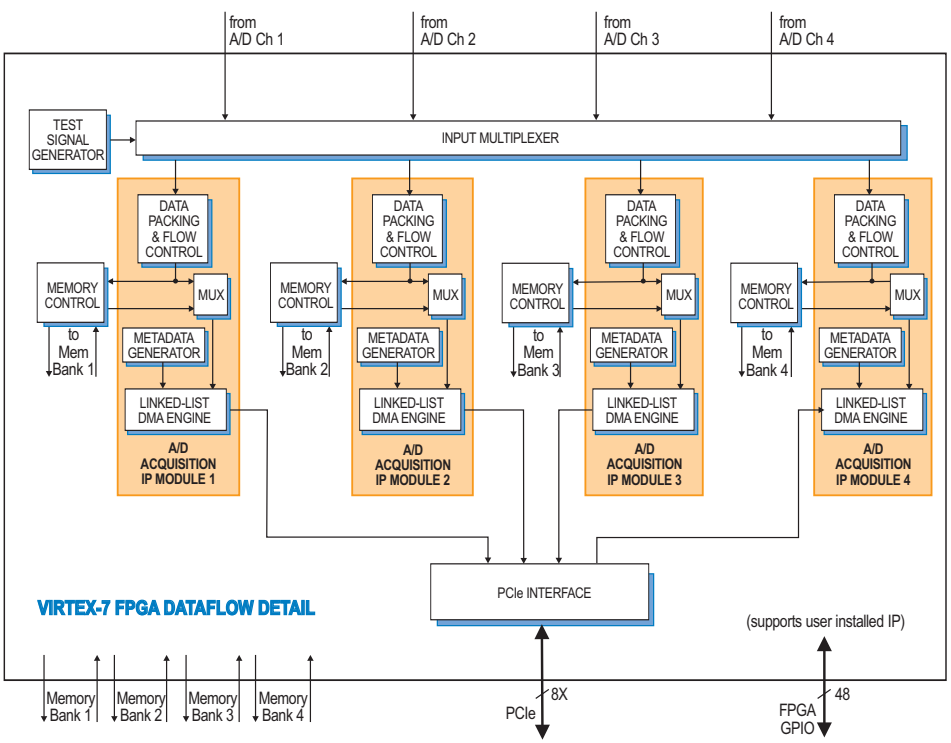
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives ➤

A/D Acquisition IP Modules

The 56760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - AMC

➤ an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56760's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user- installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56760 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56760	4-Channel 200 MHz A/D with Virtex-7 FPGA - AMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through front panel connector

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 56761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - AMC

General Information

Model 56761 is a member of the Onyx® family of high-performance AMC boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. It features built-in support for Gen. 1 and 2 PCI Express.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

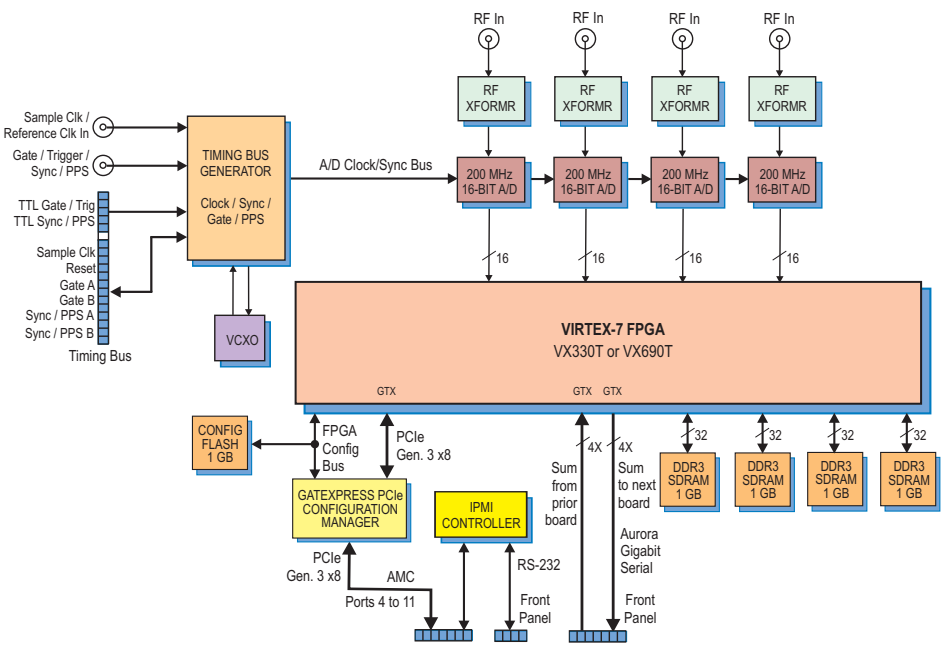
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)



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Model 56761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - AMC

A/D Acquisition IP Modules

The 56761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 56761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

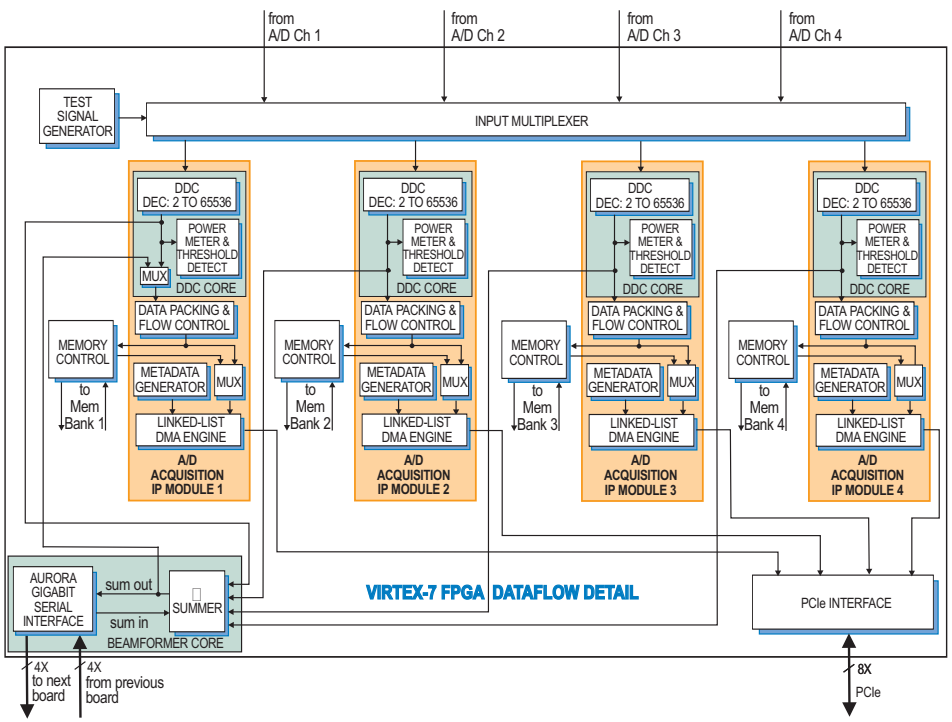
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56761's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

AMC Interface

The Model 56761 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Memory Resources

The 56761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56761 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 56761 — 4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - AMC
Options:	
-076	XC7VX690T-2 FPGA

Contact Pentek for availability of rugged and conduction-cooled versions

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New!

Model 56791

L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC

General Information

Model 56791 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56791 includes general purpose and gigabit serial connectors for application-specific I/O .

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 56791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 56791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

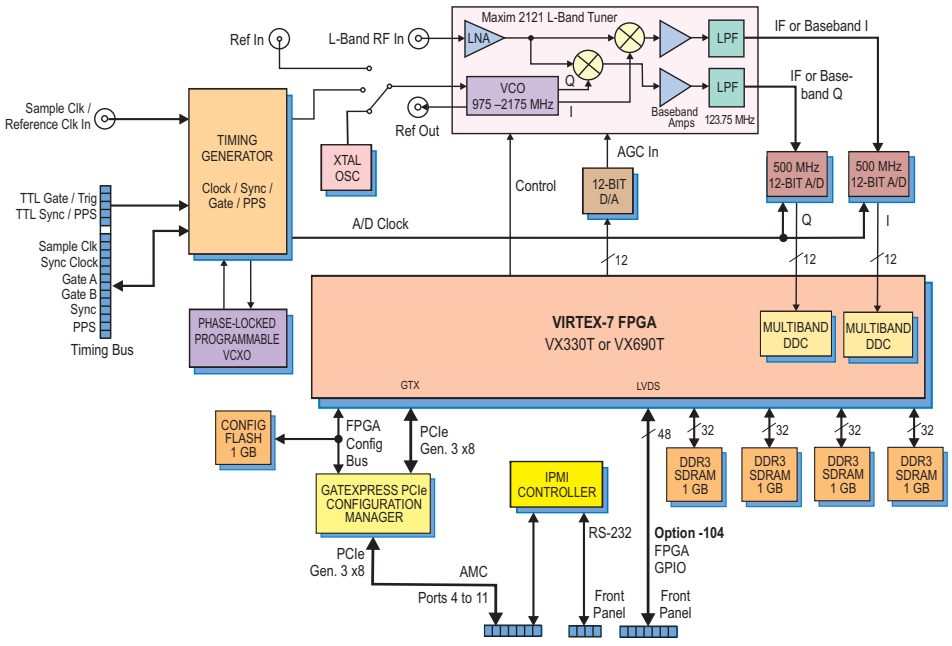
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC

A/D Acquisition IP Modules

The 56791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

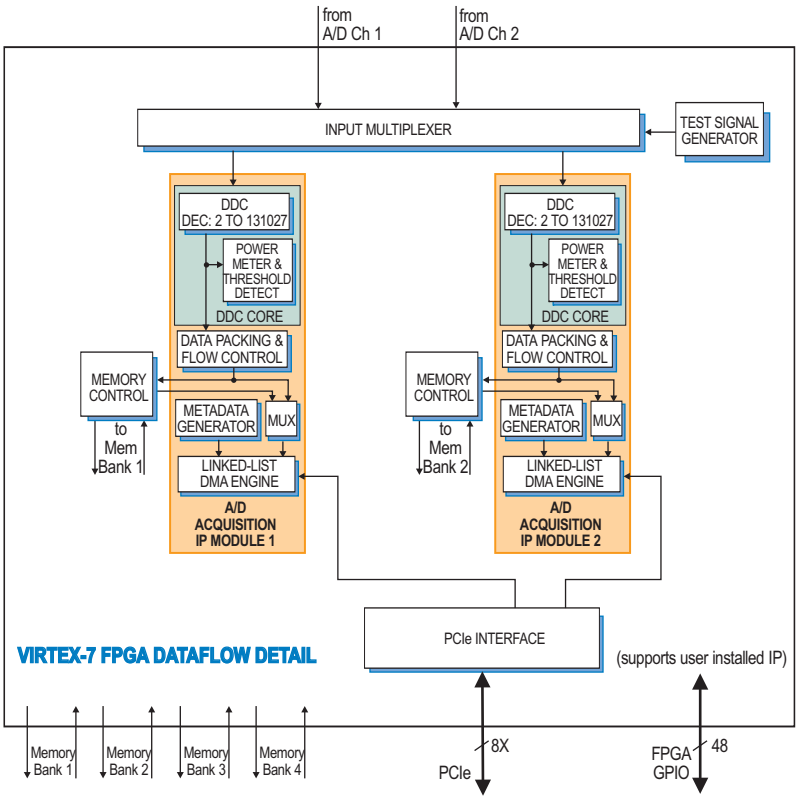
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

AMC Interface

The Model 56791 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 56791 L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC

➤ Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** –97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference ($freq_{REF}$):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** 3 dB cutoff frequency: 123.75 MHz

A/D Converters
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3*: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
56791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - AMC
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through front-panel connector

Contact Pentek for availability of rugged versions

* Gen 3 requires a compatible backplane and SBC

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New!

Model 56131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56131 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

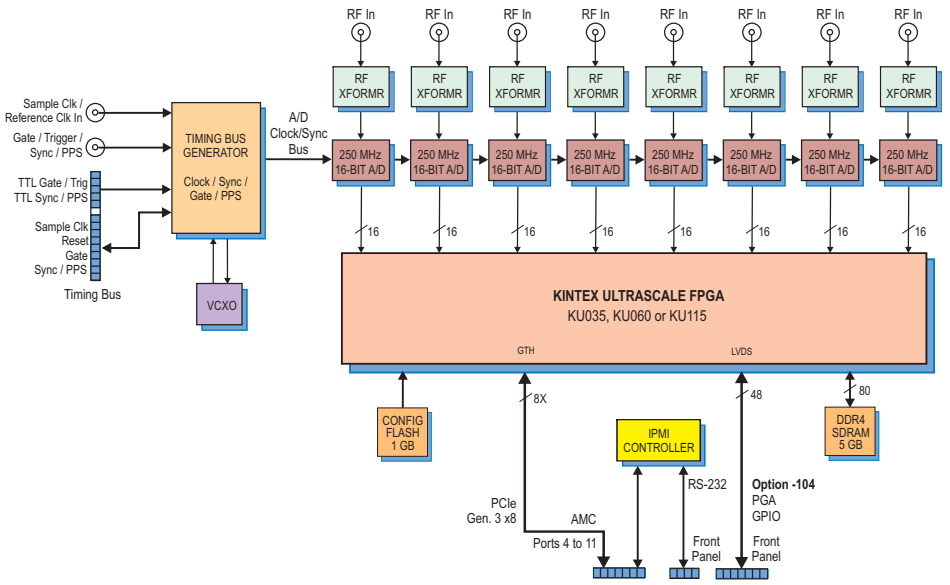
Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through ➤



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Model 56131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 56131 features eightA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

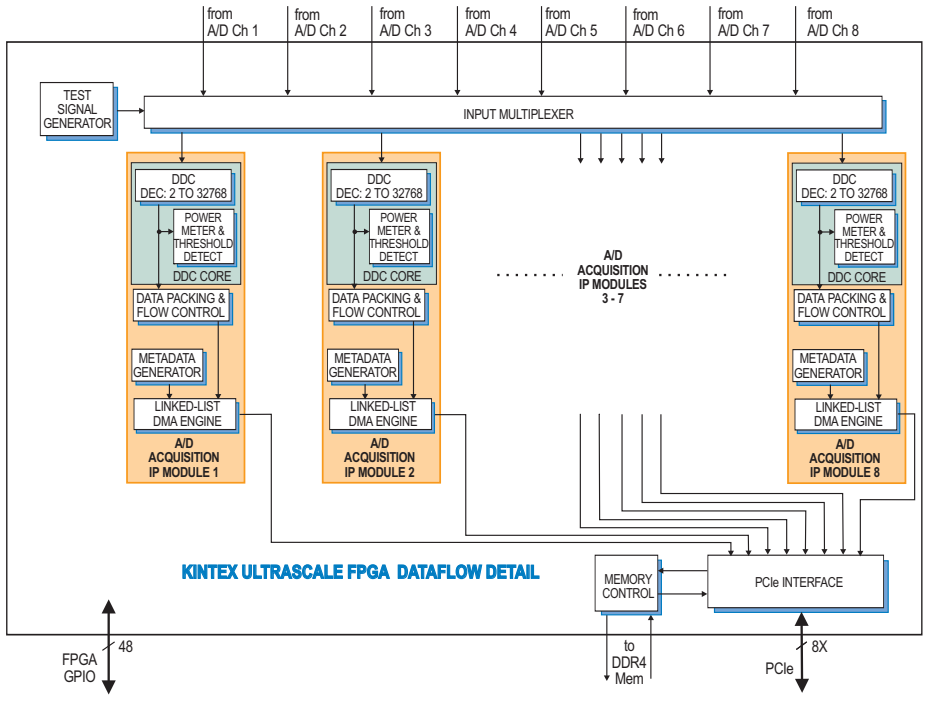
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 56131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56131 complies with the AMC 1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New!

Model 56132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56132 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

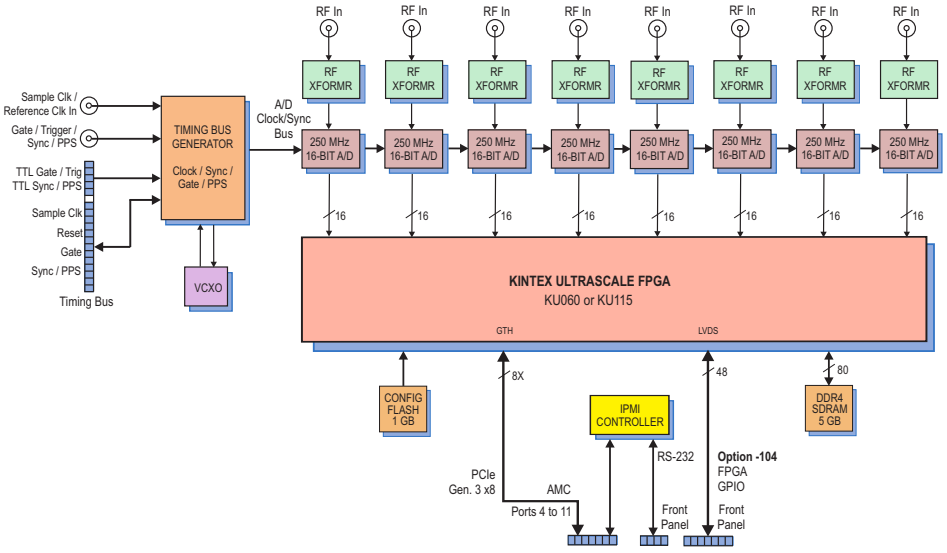
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 566862 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downonversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

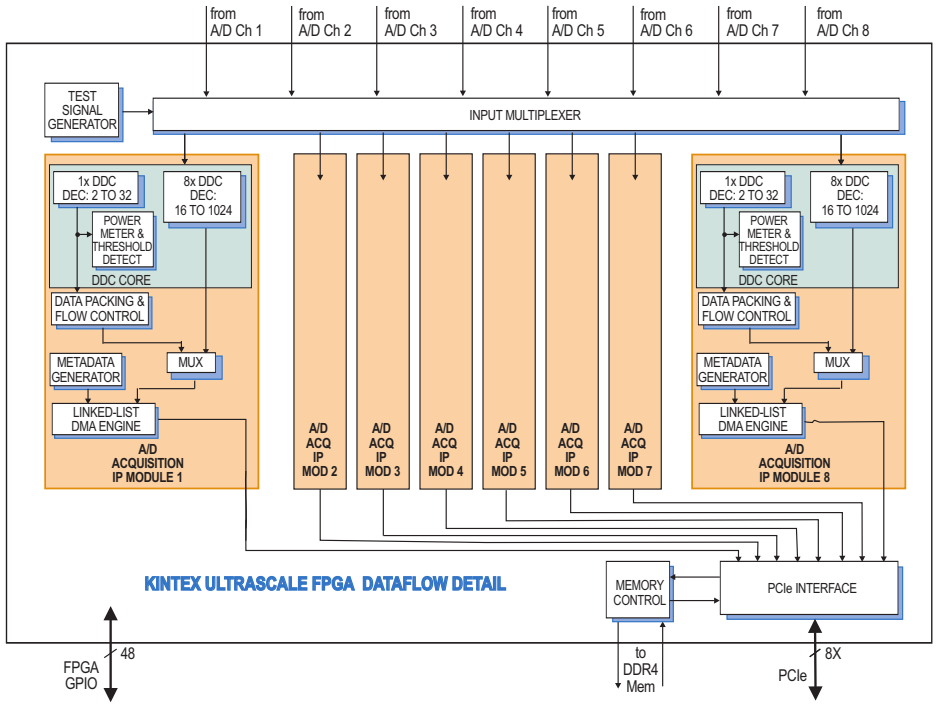
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected b oards. For larger systems, the Model 5693 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ➤



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Model 56132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56132 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Eight banks, 8 channels per bank
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front- panel connector for custom I/O

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

Ordering Information

Model	Description
56132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New

Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

Model 56141

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56141 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

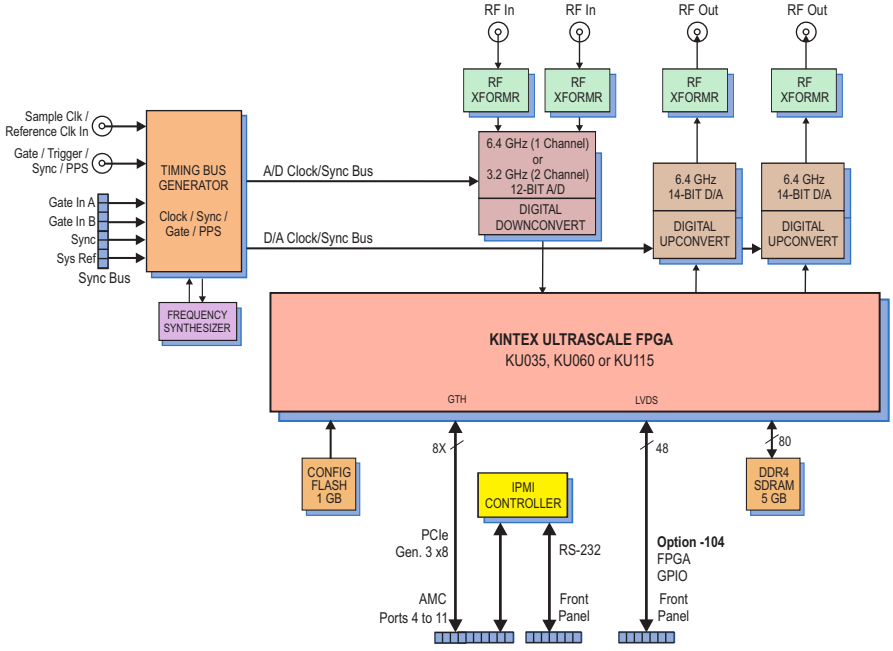
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

A/D Acquisition IP Module

The 56141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 56141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 56141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

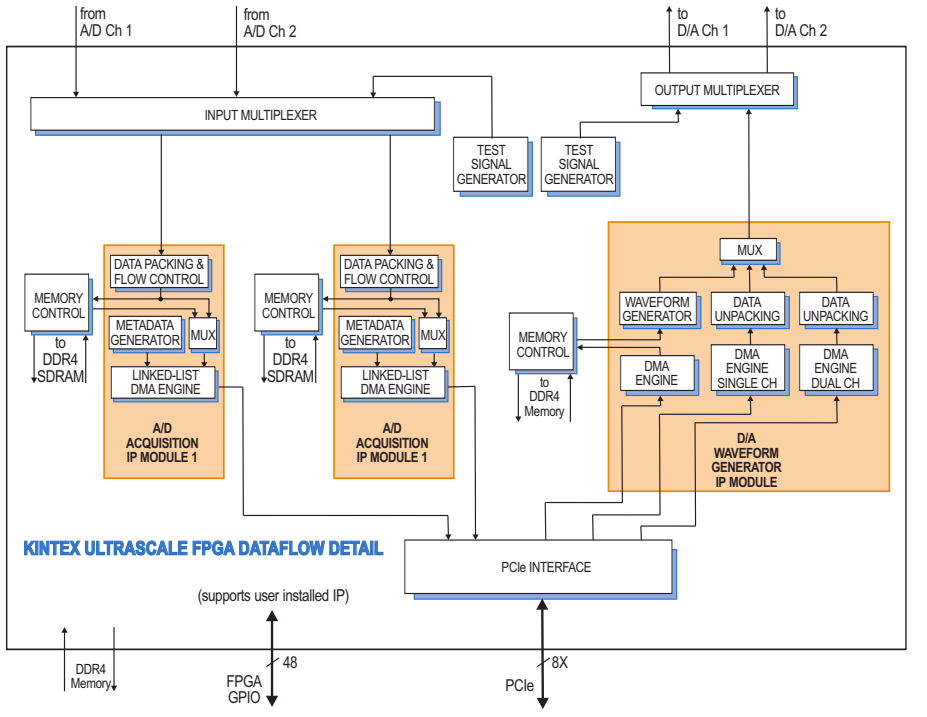
PCI Express Interface

The Model 56141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 56141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5692 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

➤ AMC Interface

The Model 56141 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front- panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module
2.890 in x 7.110 in
(73.40 mm x 180.60 mm)

Ordering Information

Model	Description
56141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Chan. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 702	Air cooled, Level L2
- 713	Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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New!

Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56821 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 56821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

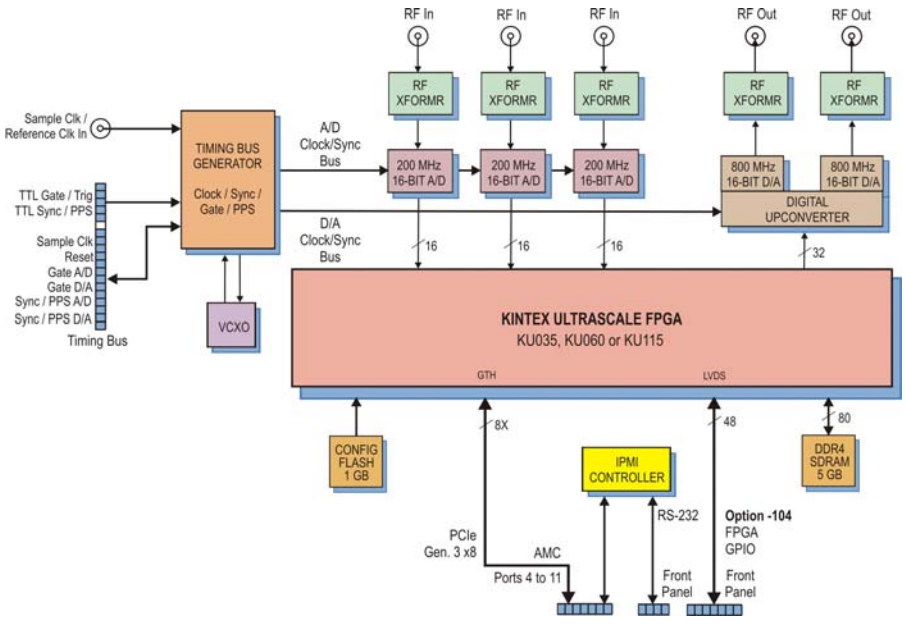
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 56821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



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Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 56821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 56821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

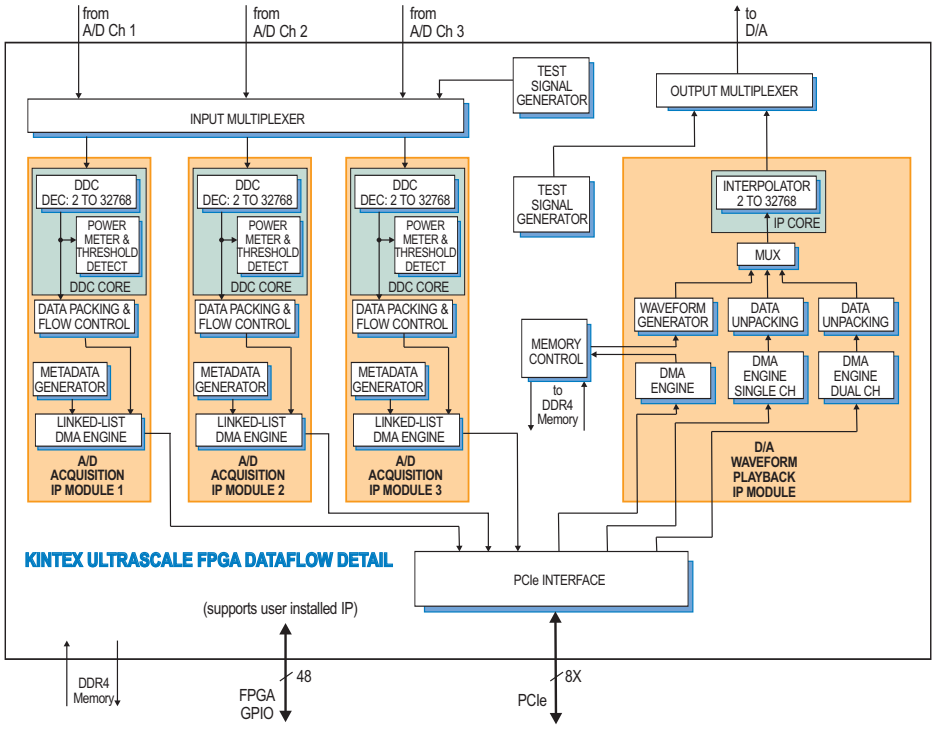
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

AMC Interface

The Model 56821 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module
2.890 in x 7.110 in
(73.40 mm x 180.60 mm)

Ordering Information

Model	Description
56821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - AMC
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New!

Model 56841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Down-converter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56841 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56841 is a high-speed data converter with programmable DDCs (digital down-converters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

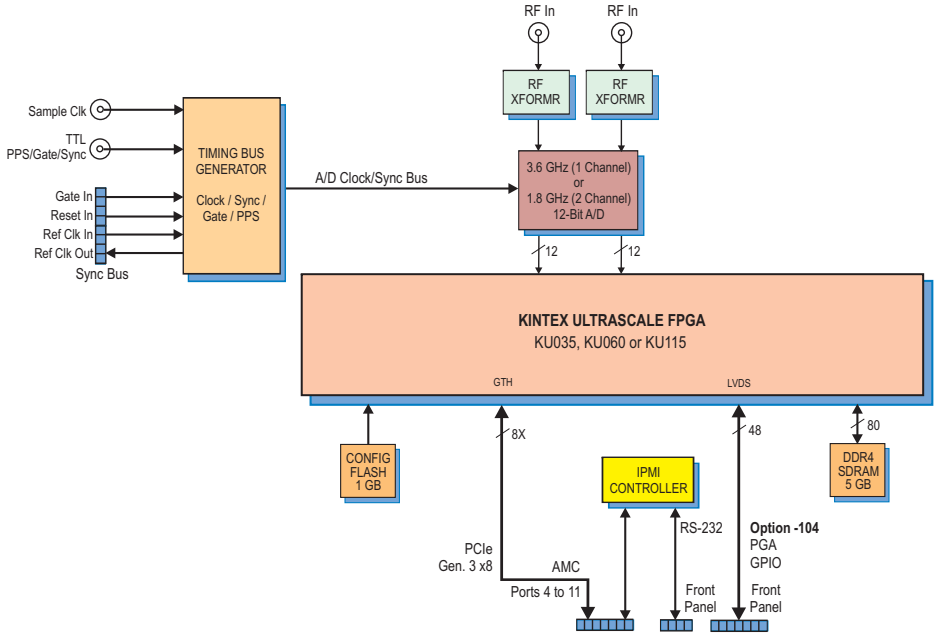
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Model 56841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - AMC

A/D Acquisition IP Module

The 56841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

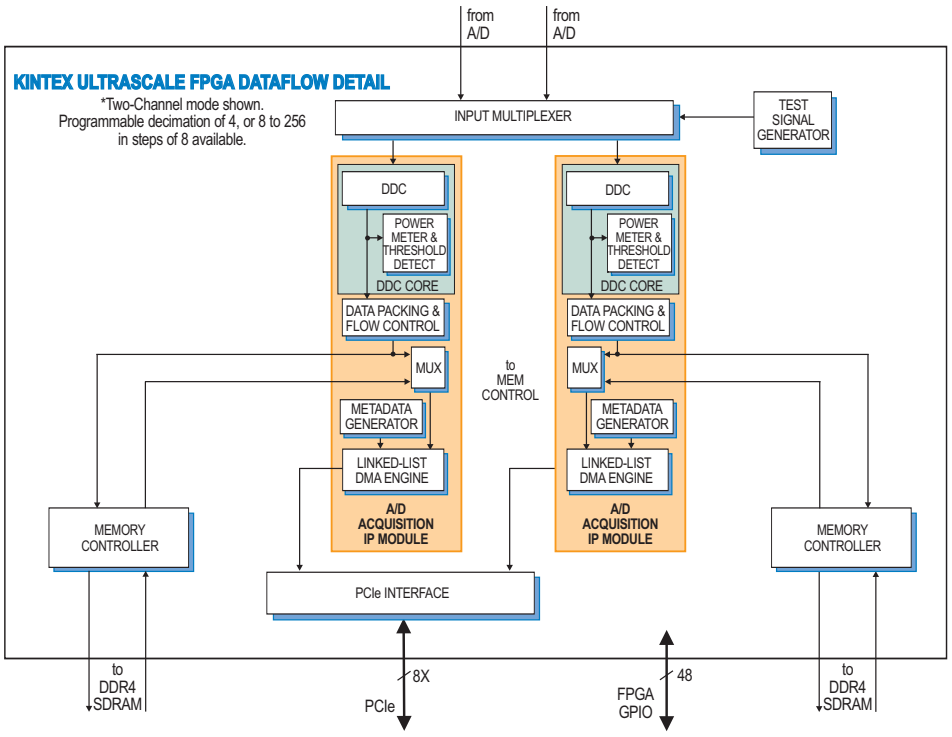
Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boardss.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources. ➤



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Model 56841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - AMC

Memory Resources

The 56841 architecture supports 5 GB of DDR4 SDRAM memory. The memory is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

AMC Interface

The Model 56841 complies with the AMC 1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Ordering Information

Model	Description
56841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O through front panel connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Clocking and Synchronization

The 56841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 56841's can be synchronized with a simple cable. For larger systems, multiple 56841's can be synchronized using the Model 5692 high-speed sync board to drive the sync bus.

PCI Express Interface

The Model 56841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input Level:** may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Single-channel mode:** decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** the DDC can be bypassed completely
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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www.pentek.com

New!

Model 56851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Model 56851 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

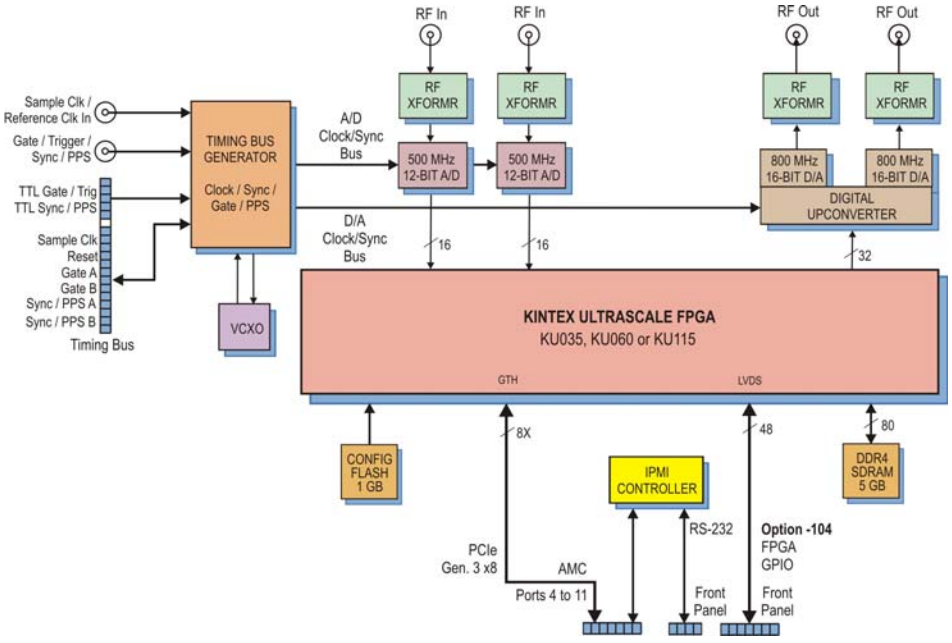
The 56851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 56851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 56851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 56851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

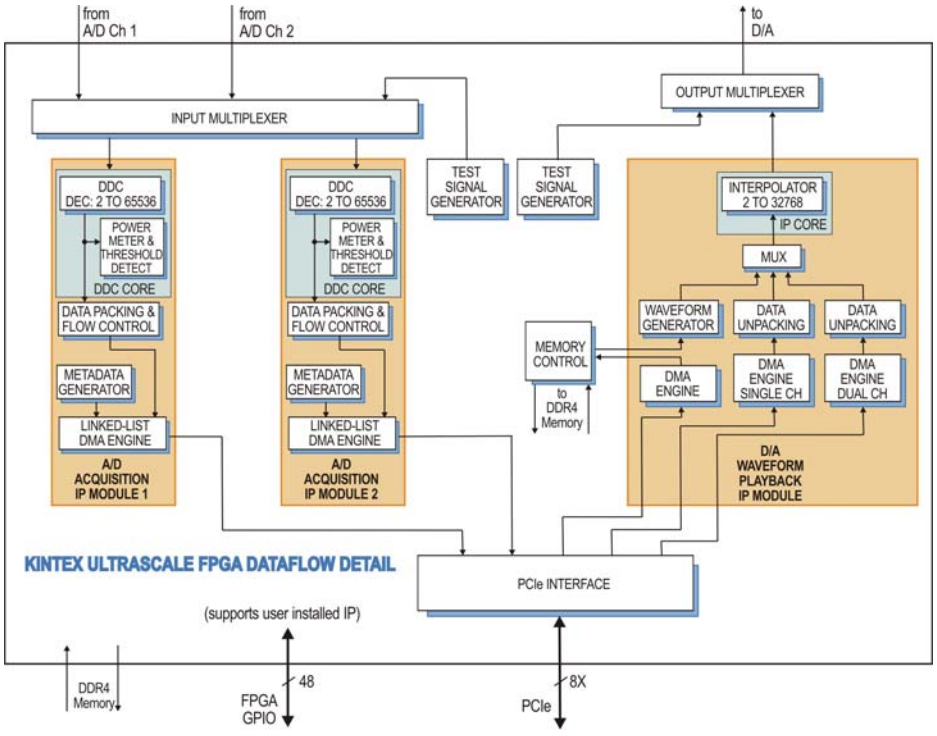
Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 71851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

AMC Interface

The Model 56851 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

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Model 56851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module
2.890 in x 7.110 in
(73.40 mm x 180.60 mm)

Ordering Information

Model	Description
56851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - AMC
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New!

Model 56861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56861 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

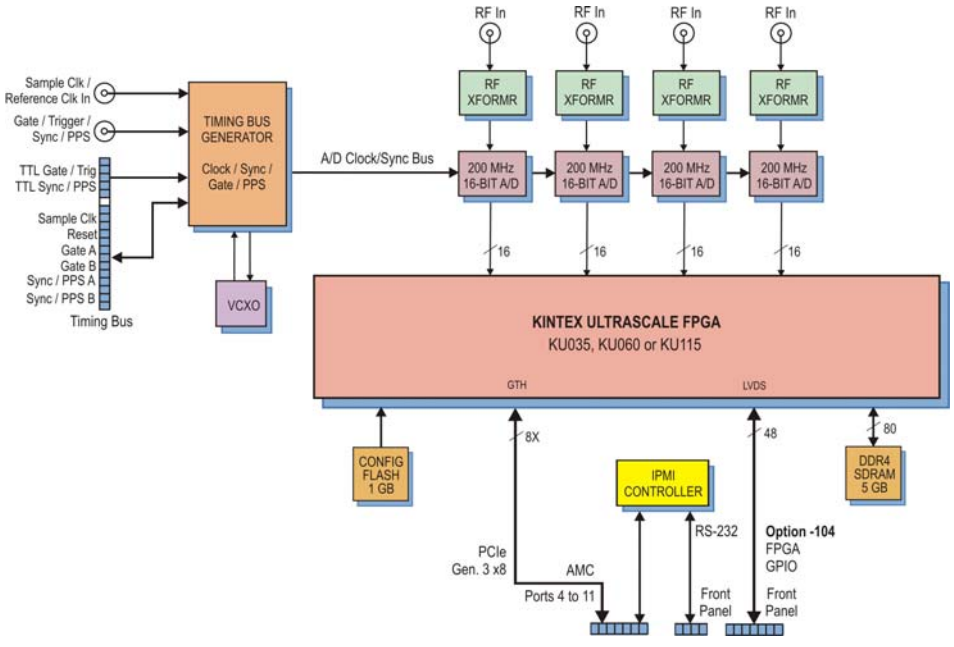
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Model 56861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 56861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

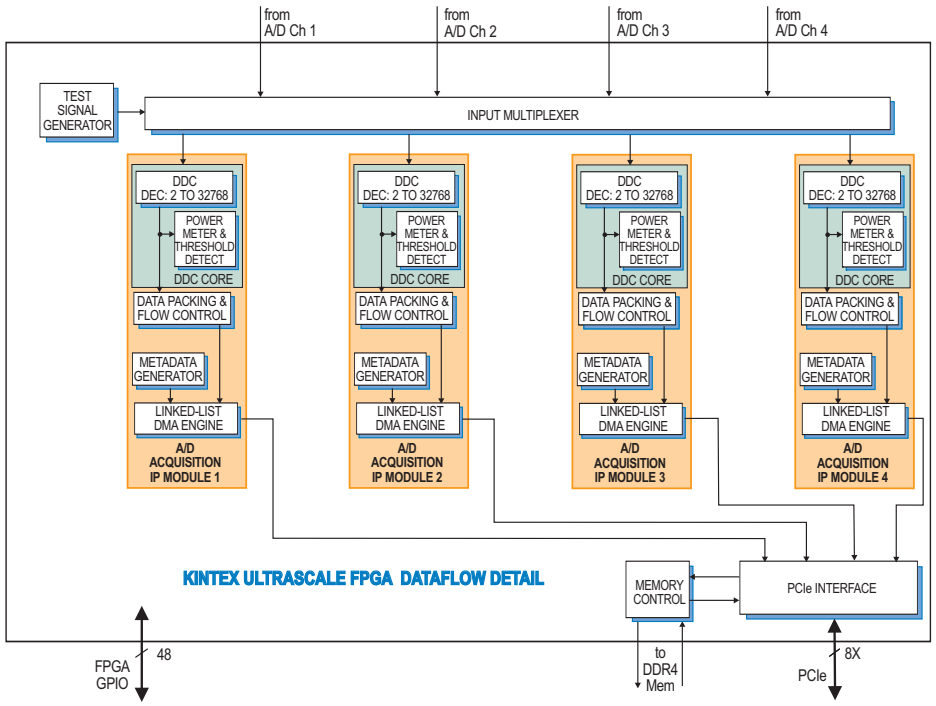
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Model 56861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56861 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module
2.890 in x 7.110 in
(73.40 mm x 180.60 mm)

Ordering Information

Model	Description
56861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to front-panel connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New!

Model 56862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56862 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

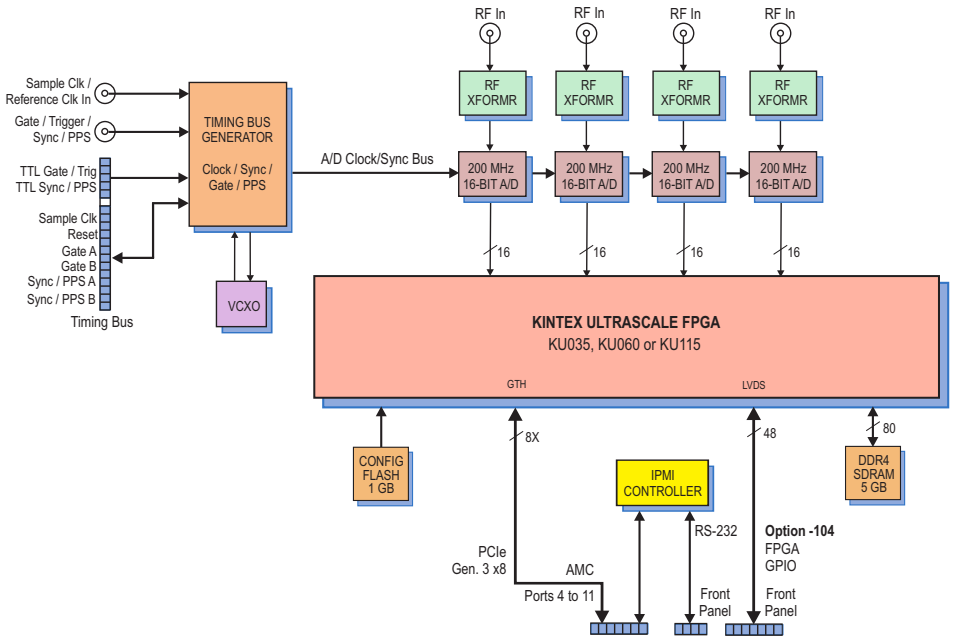
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 56862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

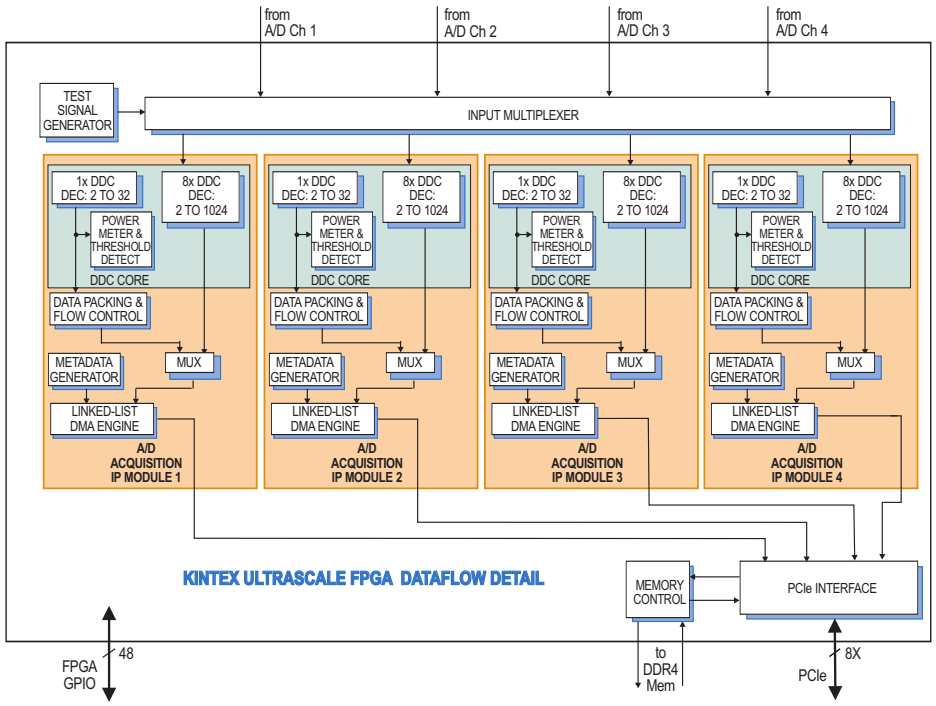
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 56862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56862 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity:** Four banks, 8 channels per bank
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, idependent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in 73.40 mm x 180.60 mm

Ordering Information

Model	Description
56862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to front-panel connector
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New!

Model 56800

Kintex UltraScale FPGA Coprocessor- AMC

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS to the FPGA for custom I/O
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56800 is a member of the Jade™ family of high-performance AMC modules. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 56800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

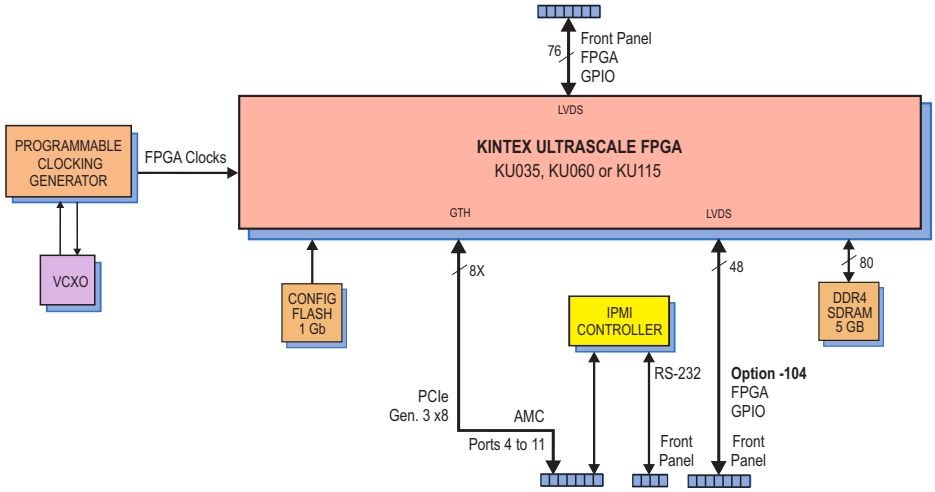
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Front Panel Digital I/O Interface

The 56800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 56800

Kintex UltraScale FPGA Coprocessor- AMC

Memory Resources

The 56800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

➤ PCI Express Interface

The Model 56800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56862 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

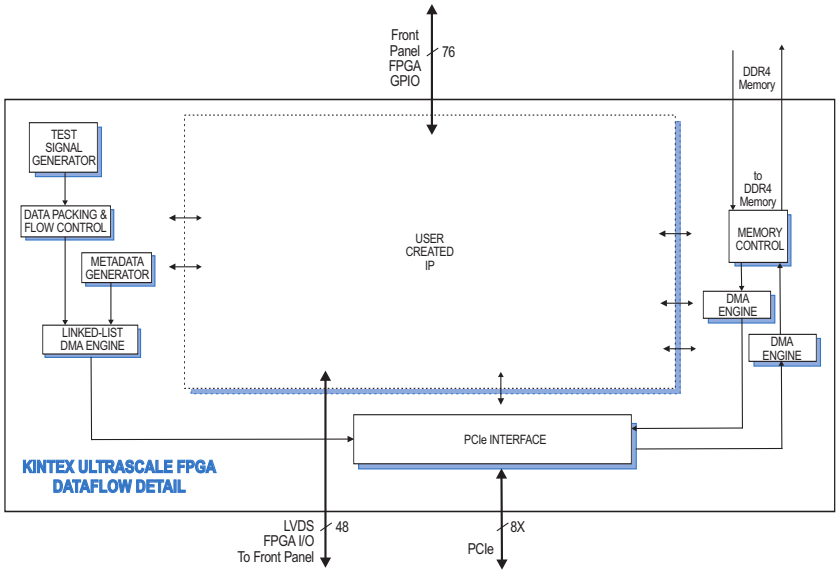
Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9

Ordering Information

Model	Description
56800	Kintex UltraScale FPGA Coprocessor - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions



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Model 5620

Bandit Two-Channel Analog RF Wideband Downconverter - AMC

Bandit

ReadyFlow Board Support Package

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

General Information

The Bandit® Model 5620 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded AMC board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5620 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5620 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5620 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5620 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

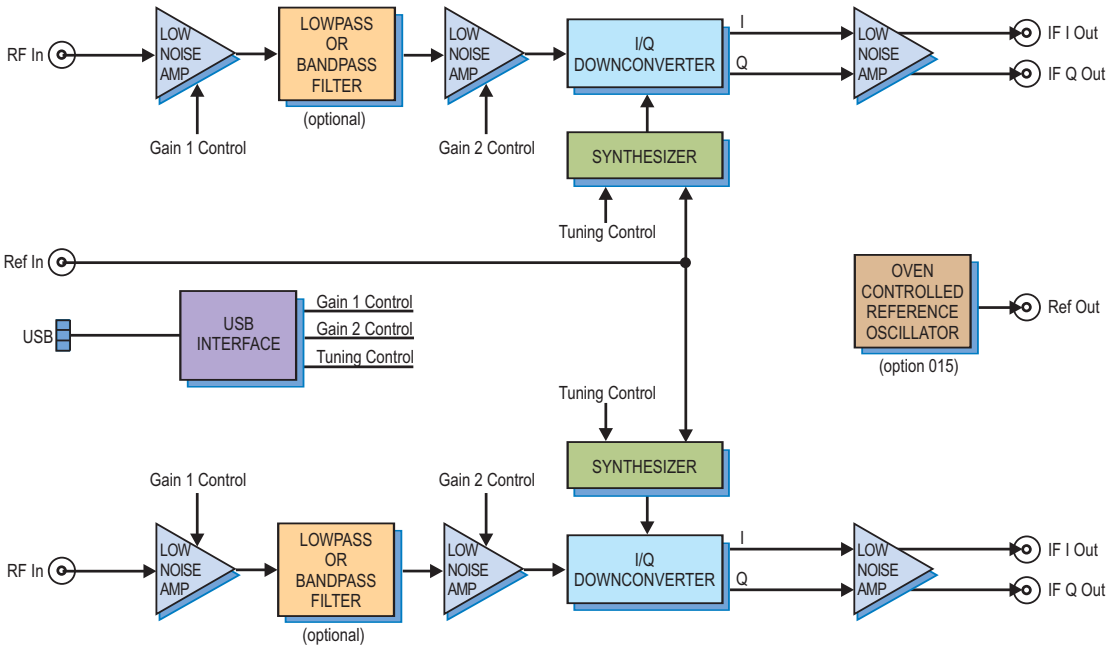
On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5620 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤



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Model 5620

Bandit Two-Channel Analog RF Wideband Doanconverter - AMC

➤ Specifications

RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** –60 dBm to –20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

Phase Noise
- **1 kHz:** –90 dBc/Hz
- **100 kHz:** –110 dBc/Hz
- **1 MHz:** –130 dBc/Hz

Noise Figure (referred to input)
- **60 dB gain:** 2.6 dB

Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedence:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

Reference Output Signal
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm
- **Aging**
  - **Daily:** ±10 ppb/day
  - **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm
- **Phase Noise**
  - **1 Hz Offset:** –67 dBc/Hz
  - **10 Hz Offset:** –100 dBc/Hz
  - **100 Hz Offset:** –130 dBc/Hz
  - **1 KHz Offset:** –148 dBc/Hz
  - **10 KHz Offset:** –154 dBc/Hz
  - **100 KHz Offset:** –155 dBc/Hz

IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8, power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
5620	Bandit Two-Channel Analog RF Wideband Downconverter - AMC

Option	Description
-015	Oven Controlled Reference Oscillator
-145	1.45 GHz lowpass input filter
-280	2.80 GHz lowpass input filter

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RADAR & SDR I/O - 3U VPX - FORMAT 2

MODEL	DESCRIPTION
Cobalt 52620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX
Cobalt 52621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, 3U VPX
Cobalt 52624	Dual-Channel, 34-Signal Adaptive IF Relay - 3U VPX
Cobalt 52630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Cobalt 52640	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX
Cobalt 52641	1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 3U VPX
Cobalt 52650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Cobalt 52651	2-Chan 500 MHz A/D with DDC, DUC with 2-Chan 800 MHz D/A, Virtex-6 FPGA - 3U VPX
Cobalt 52660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX
Cobalt 52661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
Cobalt 52662	4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - 3U VPX
Cobalt 52663	1100-Channel GSM Channelizer with Quad A/D - 3U VPX
Cobalt 52664	4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 3U VPX
Cobalt 52670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX
Cobalt 52671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX
Cobalt 52690	L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX
Onyx 52720	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 52721	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 52730	1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX
Onyx 52741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC,Virtex-7 FPGA - 3U VPX
Onyx 52751	2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX
Onyx 52760	4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 3U VPX
Onyx 52761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 3U VPX
Onyx 52791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 3U VPX
Jade 52131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Jade 52132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX
Jade 52141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - 3U VPX
Jade 52821	3-Channel 200 MHz A/D, DDC, DUC 2_Channel 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX
Jade 52841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - 3U VPX
Jade 52851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX
Jade 52861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - 3U VPX
Jade 52862	4-Channel 200 MHz A/D with Multiband DDcs and Kintex UltraScale FPGA - 3U VPX
Jade 52800	Kintex UltraScale FPGA Coprocessor- 3U VPX Format 2
Bandit 5220	Two-Channel Analog RF Wideband Downconverter - 3U VPX
8267	3U VPX Development System for Cobalt, Onyx, Flexor, and Jade boards
	Customer Information

RADAR & SDR I/O - PMC/XMC

Click Here for the PRODUCT SELECTOR

RADAR & SDR I/O - CompactPCI

RADAR & SDR I/O - x8 PCI Express

RADAR & SDR I/O - AMC

RADAR & SDR I/O - 3U VPX - FORMAT 1

RADAR & SDR I/O - 6U VPX

RADAR & SDR I/O - FMC

Last updated: March 2018

Model 52620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

Model 52620 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52620 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52620 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

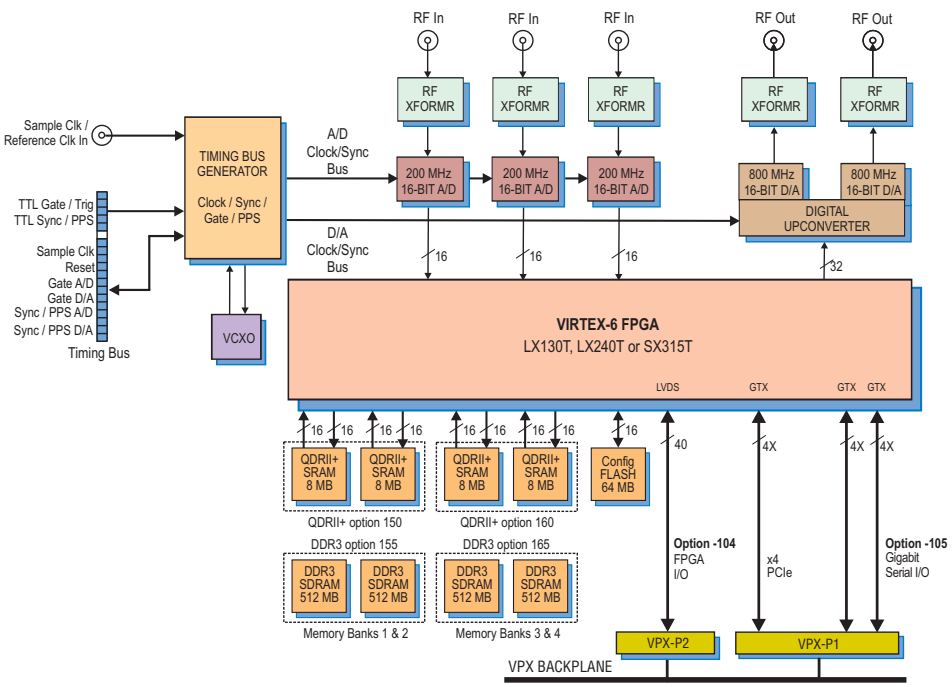
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

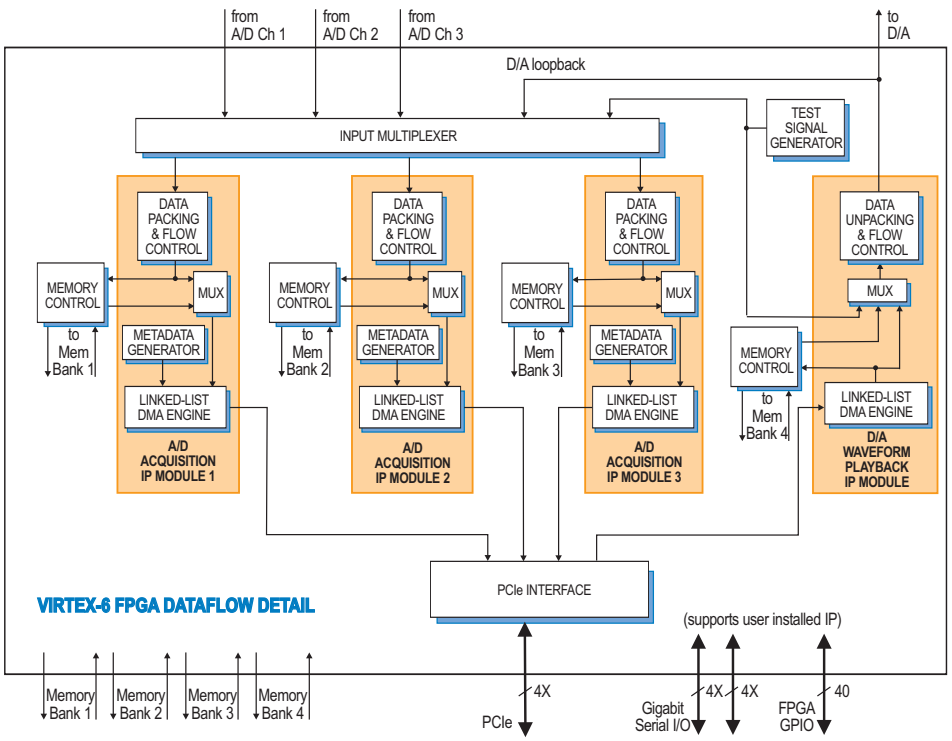
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 52621 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Optional LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52621 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

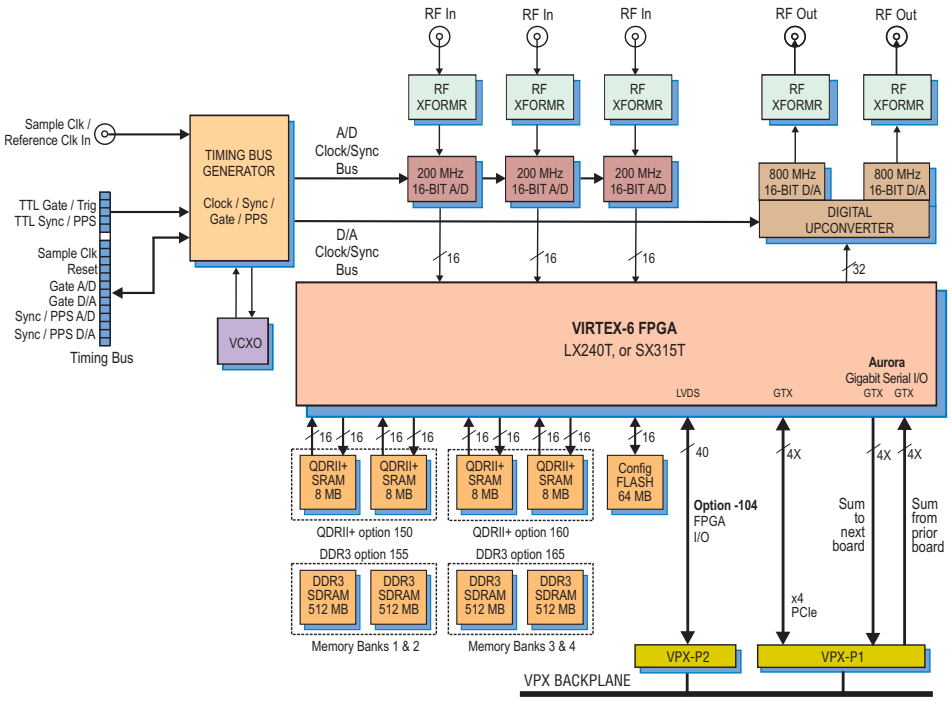
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Model 52621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

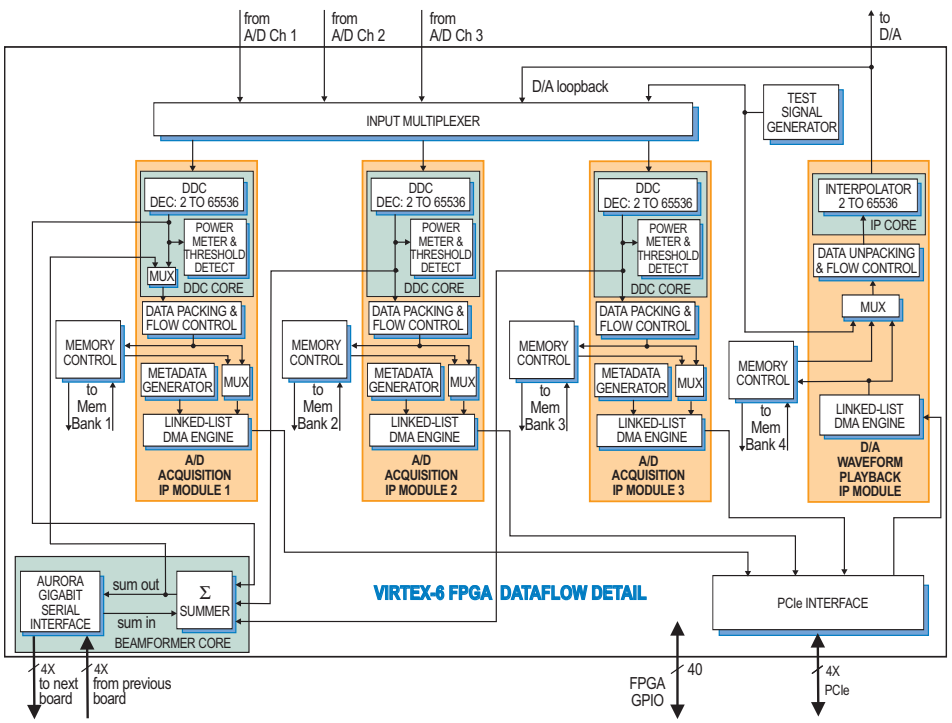
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 52621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Model 52621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to crate a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Model 52621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 52624

Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

Model 52624 COTS (left) and rugged version

Features

- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/As
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8,

General Information

Model 52624 is a member of the Cobalt® family of high-performance 3U OpenVPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 52624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 52624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

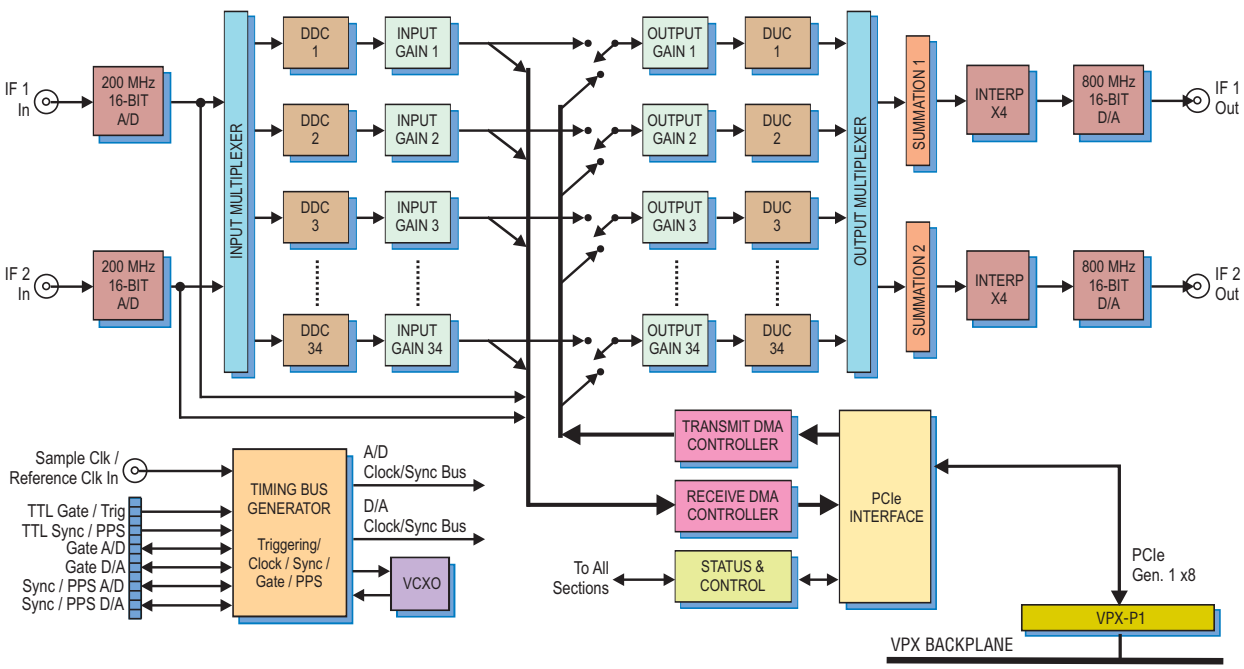
Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 52624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two summation blocks, each ➤



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➤ associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 52624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 52624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 52624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz. ➤

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52624's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

The Model 52624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Quantity: Two
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

Model 52624 — Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52624	Dual-Channel 34-Signal Adaptive IF Relay - 3U OpenVPX

Options:

-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	Development System See 8267 Datasheet for Options

Digital Downconverters
Quantity: 34
Decimation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >100 dB
Phase Offset: 1 bit, 0 or 180 degrees
FIR Filter: 18-bit coefficients
Output: Complex, 16-bit I + 16-bit Q
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
Quantity: 34
Data: Complex, 16-bit I + 16-bit Q
Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
Quantity: 34
Data: Complex, 16-bit I + 16-bit Q
Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
Quantity: 34
Interpolation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
FIR Filter: 18-bit coefficients, 16-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Analog Output Channels: 2
Type: Texas Instruments DAC5688
Input Data Rate: 200 MHz max.
Output Signal: Real
Output Sampling Rate: 800 MHz max. with 4x interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Required: Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8;

Environmental
Standard:
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Option 702 L2 Extended Temp (air-cooled):
Operating Temp: -20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-cond.
Option 712 L2 Extended Temp (conduction-cooled):
Operating Temp: -20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U VPX board, 100 x 160 mm (3.937 x 6.299 in.)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

Model 52630 COTS (left) and rugged version

General Information

Model 52630 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

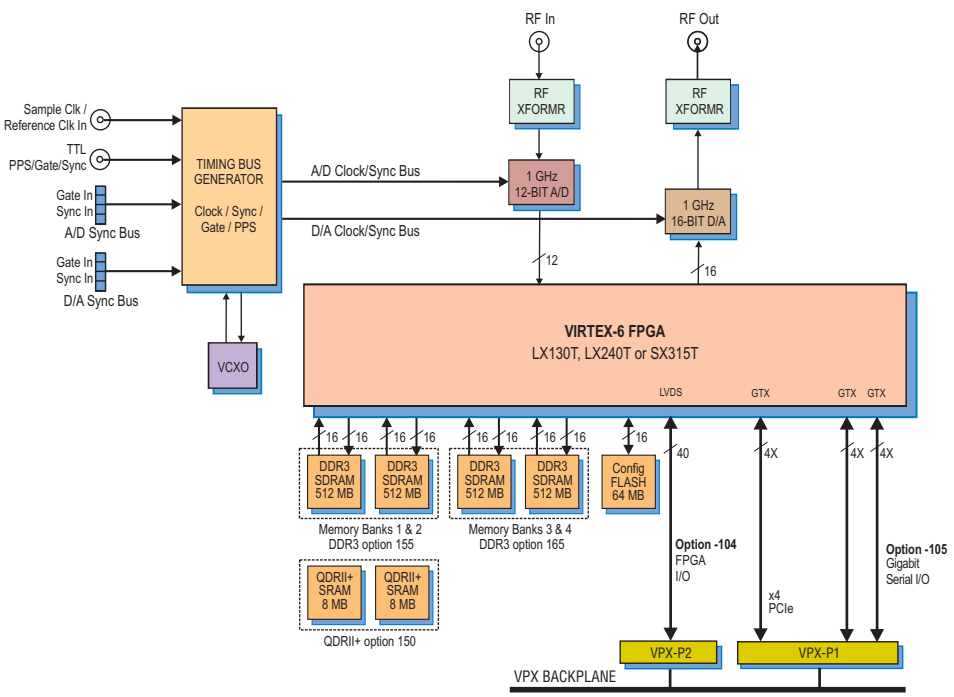
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Model 52630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Module

The 52630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 52630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

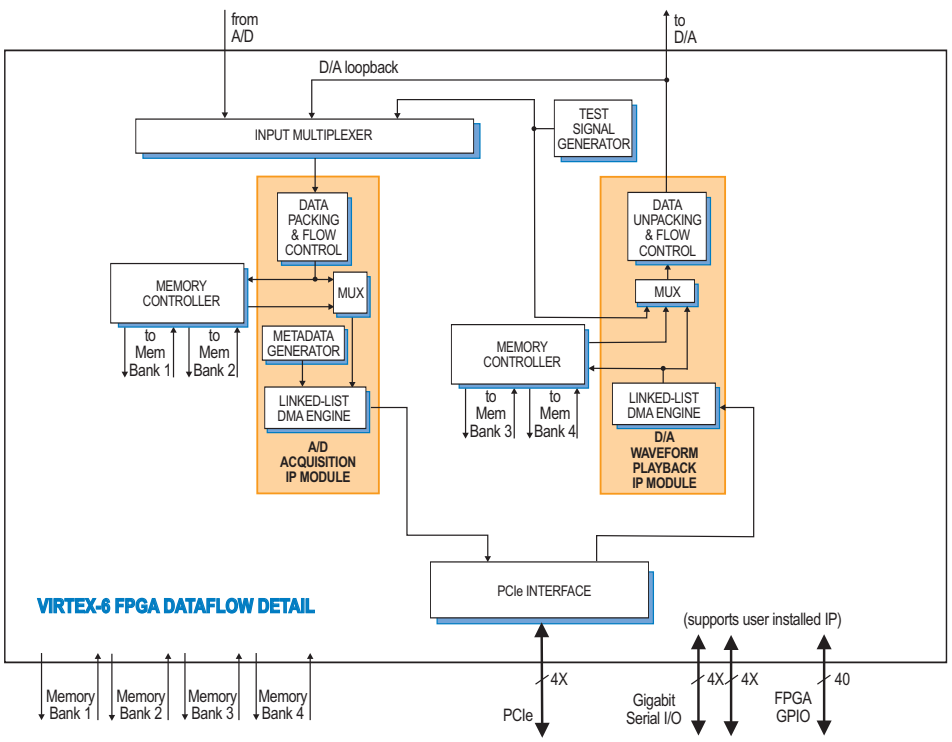
A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 5292 and Model 9192 Cobalt Synchronizers can drive multiple 52630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 52630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

PCI Express Interface

The Model 52630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen 2: x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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www.pentek.com

Model 52640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

Model 52640 COTS (left) and rugged version

General Information

Model 52640 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

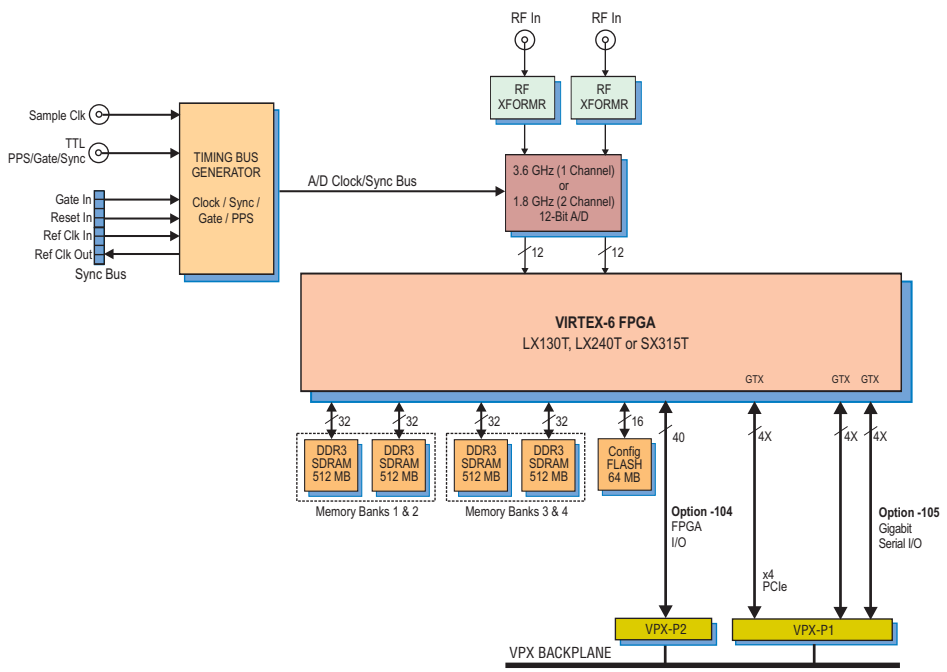
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 52640 accepts an 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 52640's can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 52640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

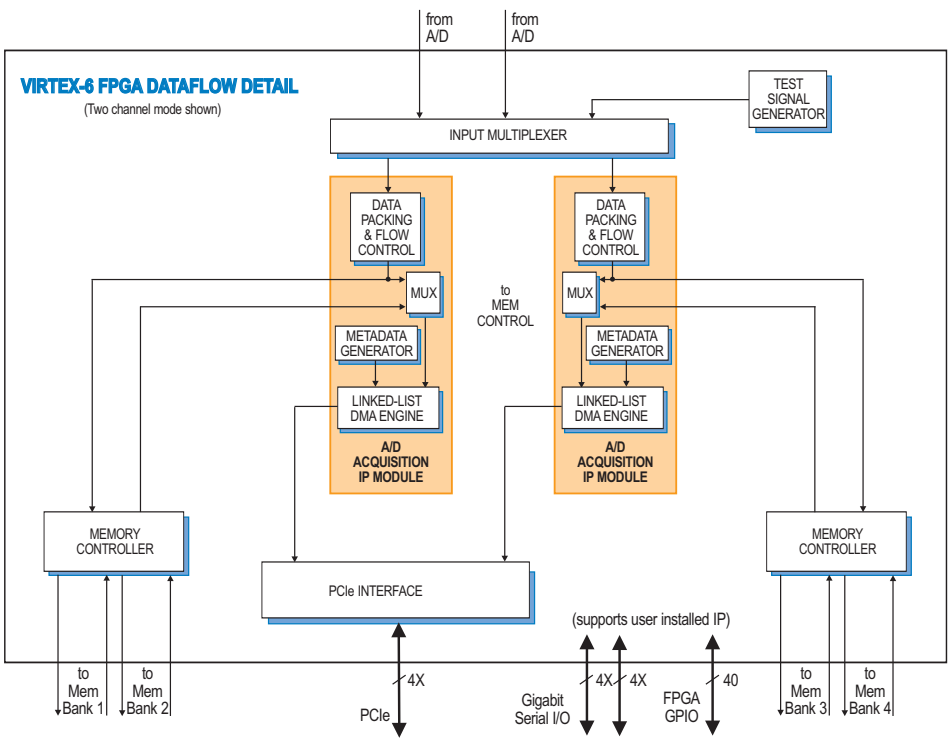
The Model 52640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Module

The 52640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Model 52640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Sample Clock Sources: Front panel SSMC connector
Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out reference clock
External Trigger Input
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm).

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Model 52641 COTS (left) and rugged version

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programmable one- or two-channel DDC (Digital Downconverter)
- PCI Express (Gen. 1 & 2) interface, up to x4
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52641 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 52641 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

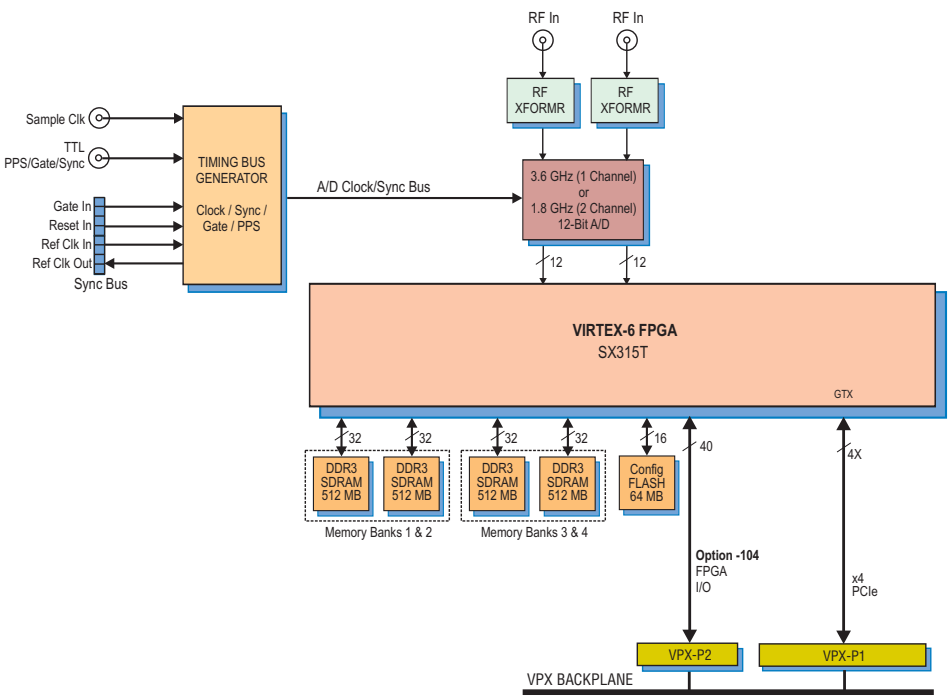
For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤



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Model 52641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Module

The 52641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

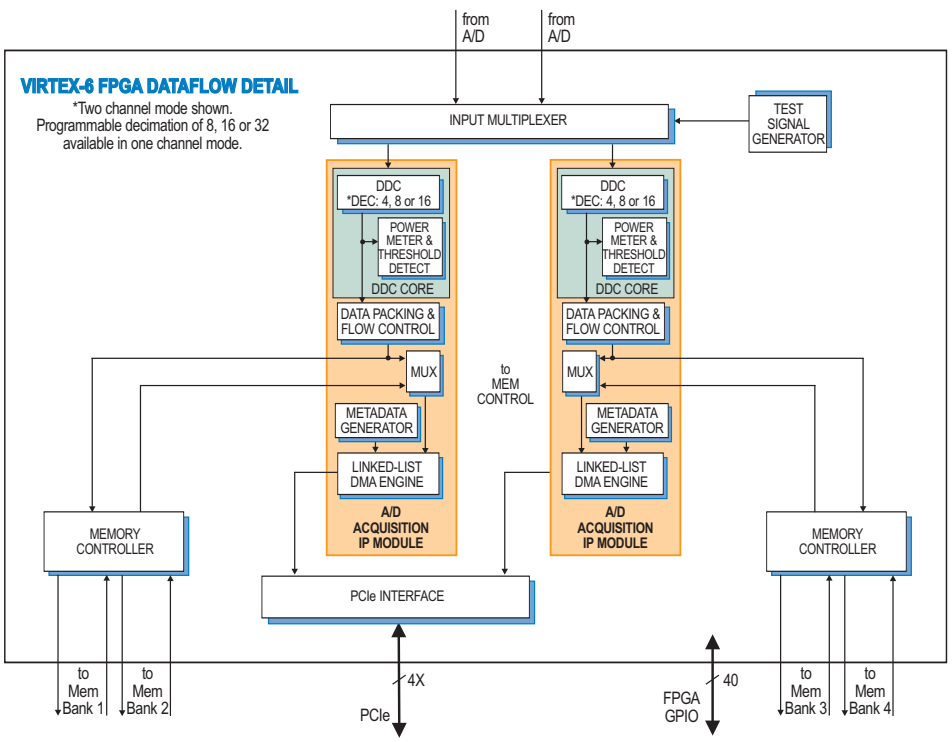
Clocking and Synchronization

The 52641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 52641's can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 52641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Model 52641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ PCI Express Interface

The Model 52641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

Model 52650 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52650 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52650 includes two A/Ds, one DUC (digital upconverter), two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

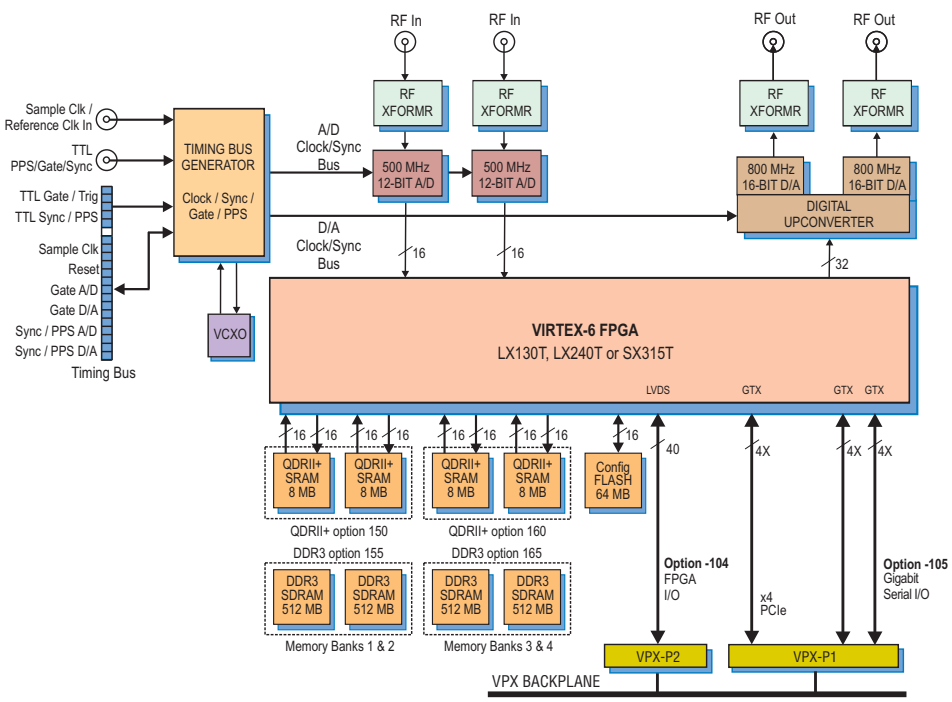
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

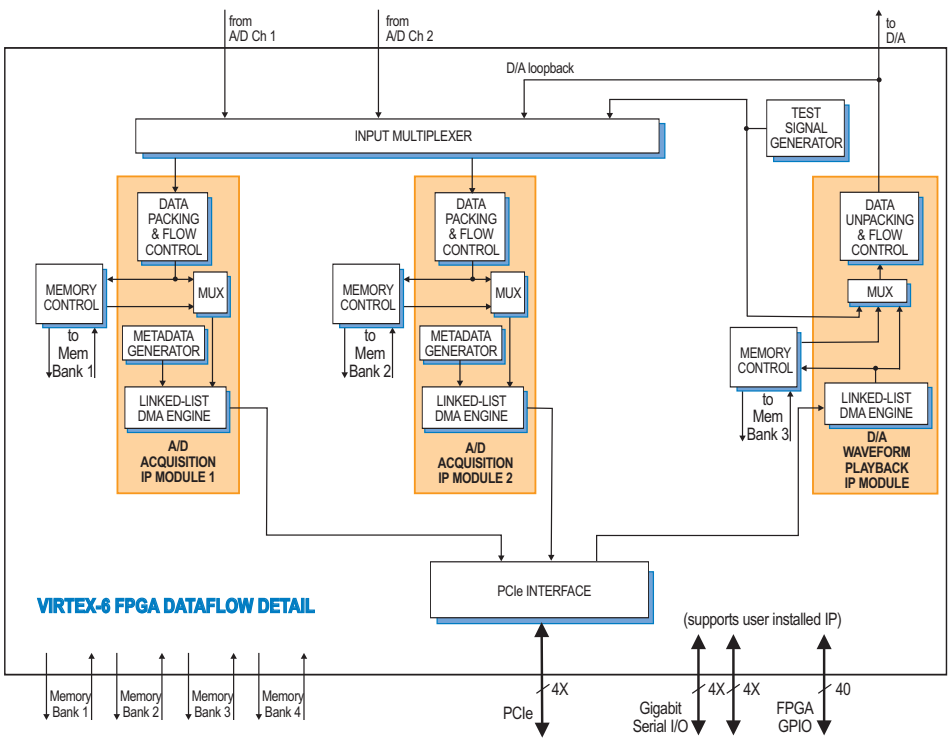
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Model 52650 — Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 52650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52650	Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 52651 COTS (left) and rugged version

Cobalt GateFlow ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52651 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52651 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

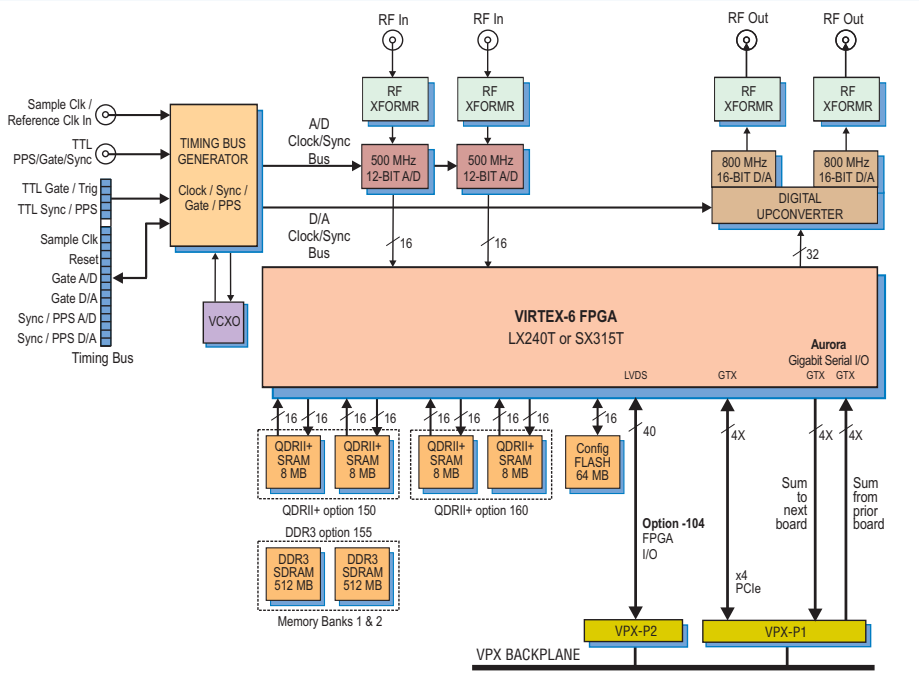
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Model 52651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

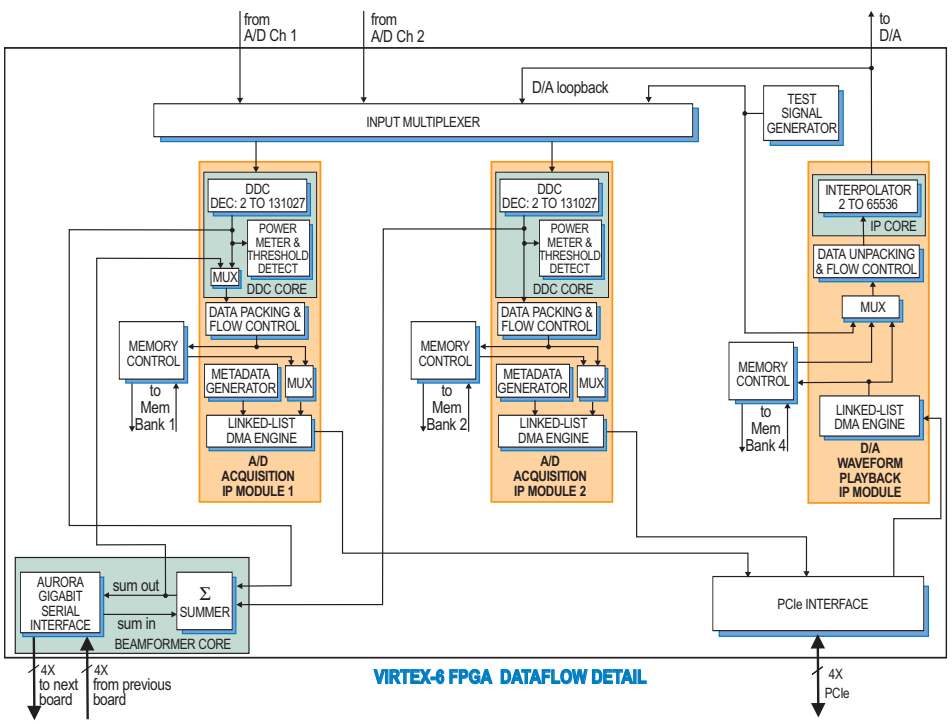
A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52651's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 52651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Model 52651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

Model 52651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240 FPGA
-064	XC6VSX315 FPGA
-104	LVDS FPGA I/O through the VPX P2 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ **A/D Converters (option -014)**
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link over the VPX P1connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-T2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Model 52660 COTS (left) and rugged version

General Information

Model 52660 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 52660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

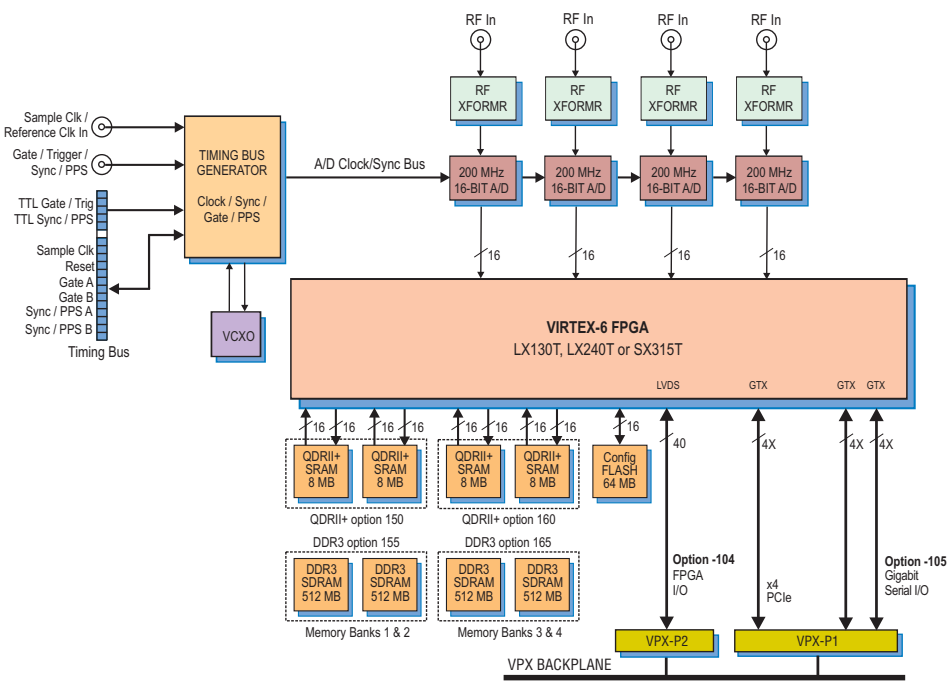
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

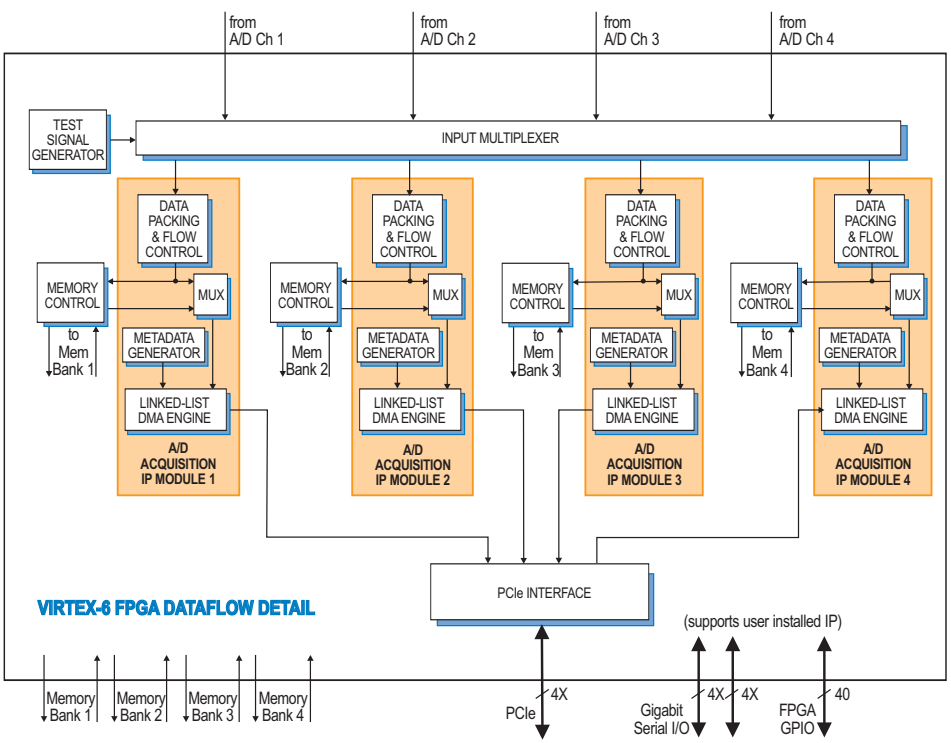
The Model 52660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Modules

The 52660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52660	4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

Model 52661 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52661 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52661 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

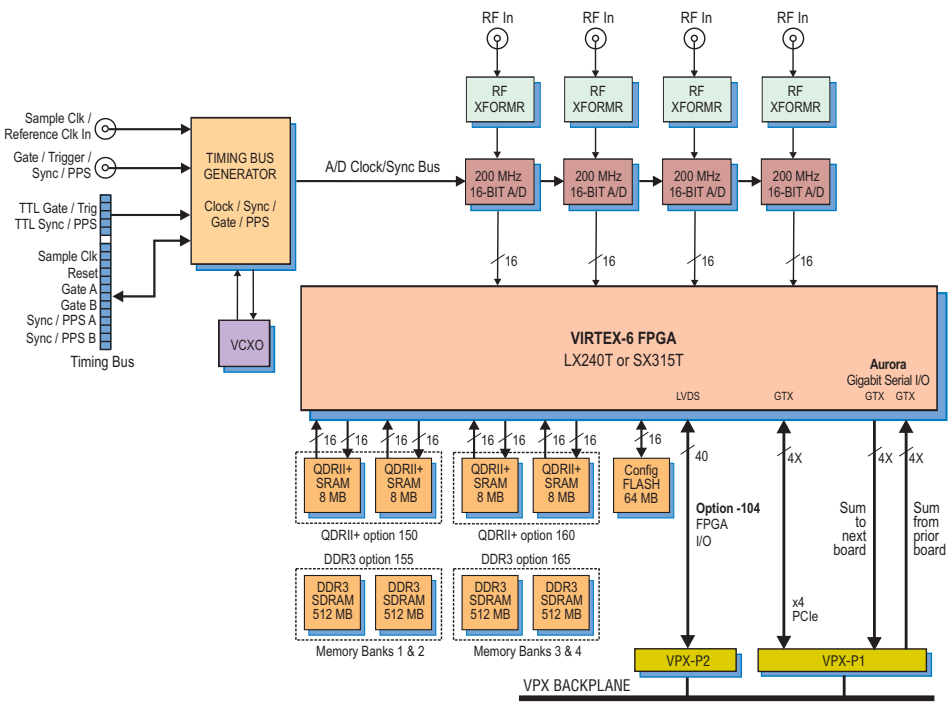
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

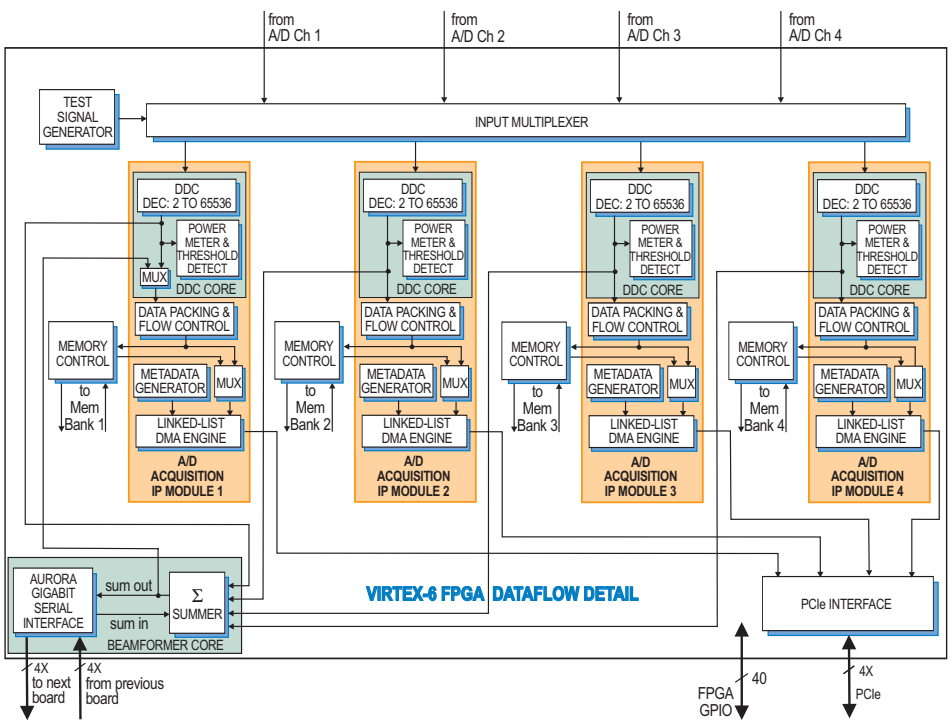
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 52661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Memory Resources

The 52661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For deeper memory resources, DDR3 SDRAM banks are 512 MB deep.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Sum Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

Model 52662 COTS (left) and rugged version

General Information

Model 52662 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

The 52662 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 52662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

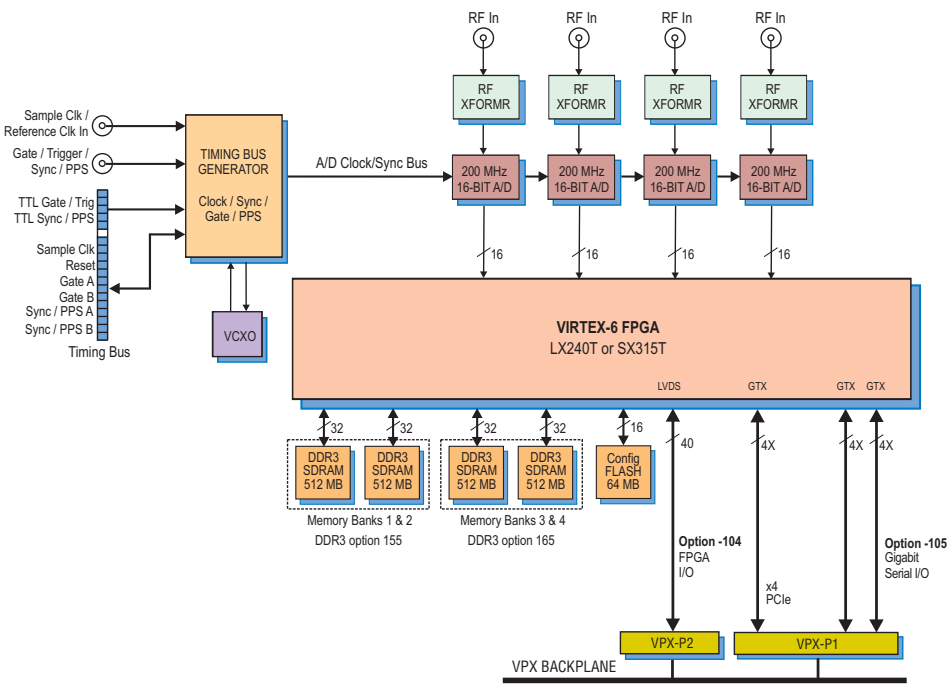
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

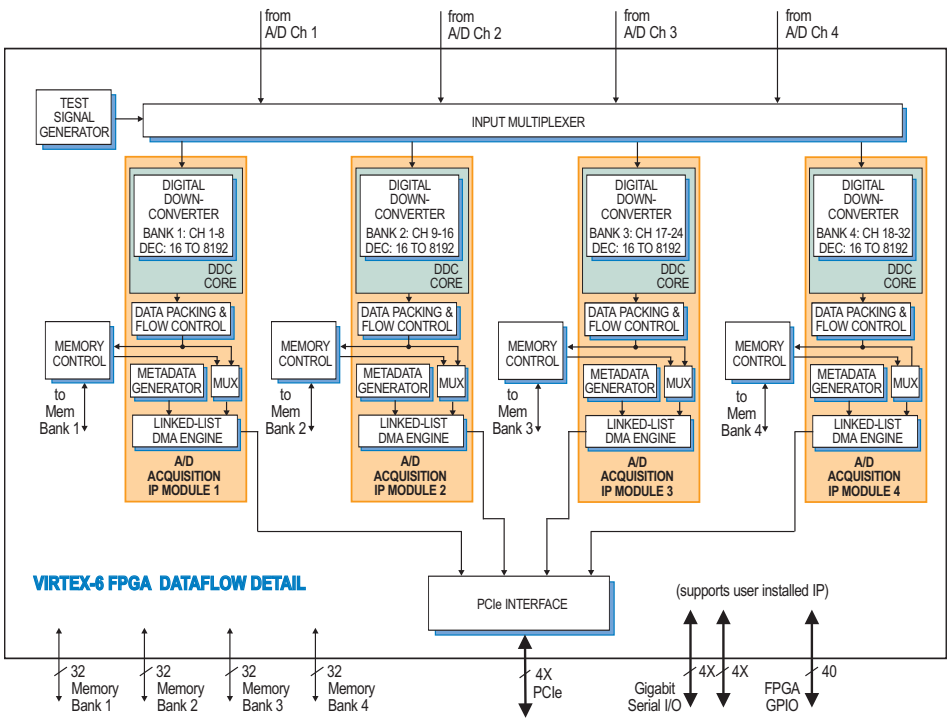
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52662 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52663

1100-Channel GSM Channelizer with Quad A/D - VPX

Model 52663 Commercial (left) and rugged version

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x4
- 3U VPX form factor provides a compact, rugged platform

General Information

Model 52663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 2 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 52663 is a complete, full-featured subsystem, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

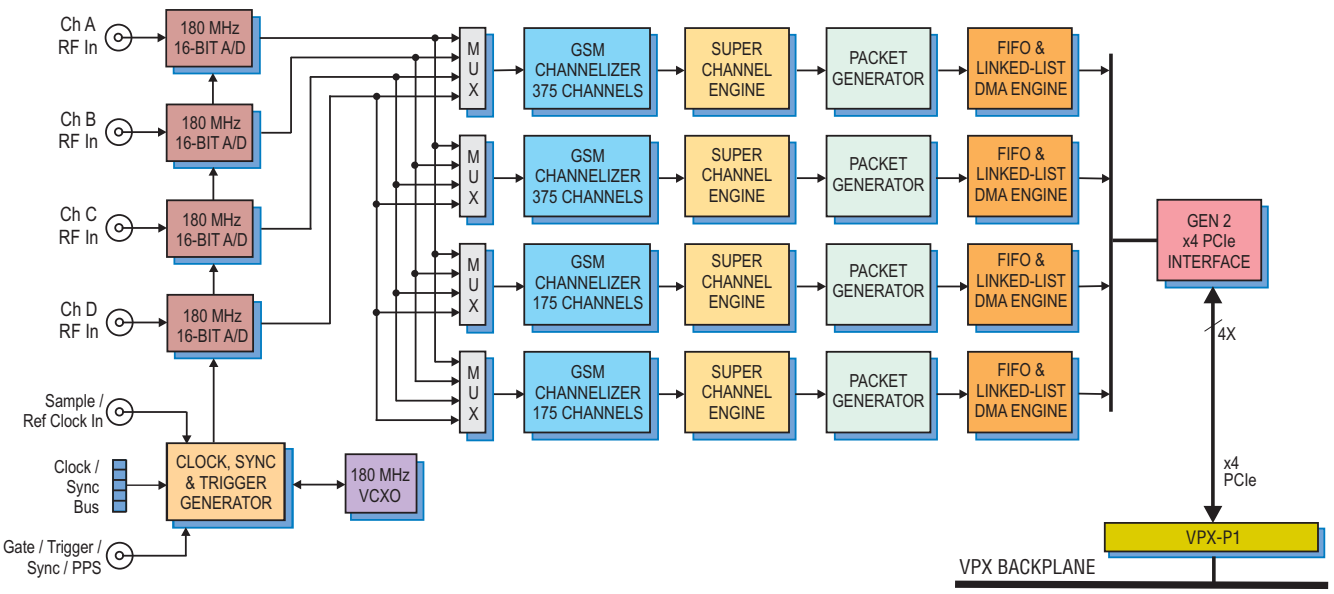
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 52663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤



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➤ The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 52663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 52663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 2 GB/sec peak rate of PCIe Gen 2 x4 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is slightly above the capability of the PCIe Gen 2 x4 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI Express Interface

The Model 52663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x4, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 52663 and host. ➤

Model 52663 — 1100-Channel GSM Channelizer with Quad A/D - VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52663	1100-Channel GSM Channelizer with Quad A/D - VPX

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing**: 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics:**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  First: $-f_s/4$ (-270.8333 kHz)
  Second: 0 Hz
  Third: $+f_s/4$ (+270.8333 kHz)
  Fourth: $+f_s/2$ (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q
- **Number of Superchannels per Bank:** 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

Model 52664 COTS (left) and rugged version

Cobalt GateFlow ReadyFlow Board Support Package

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52664 is a member of the Cobalt® family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 52664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

The 52664 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

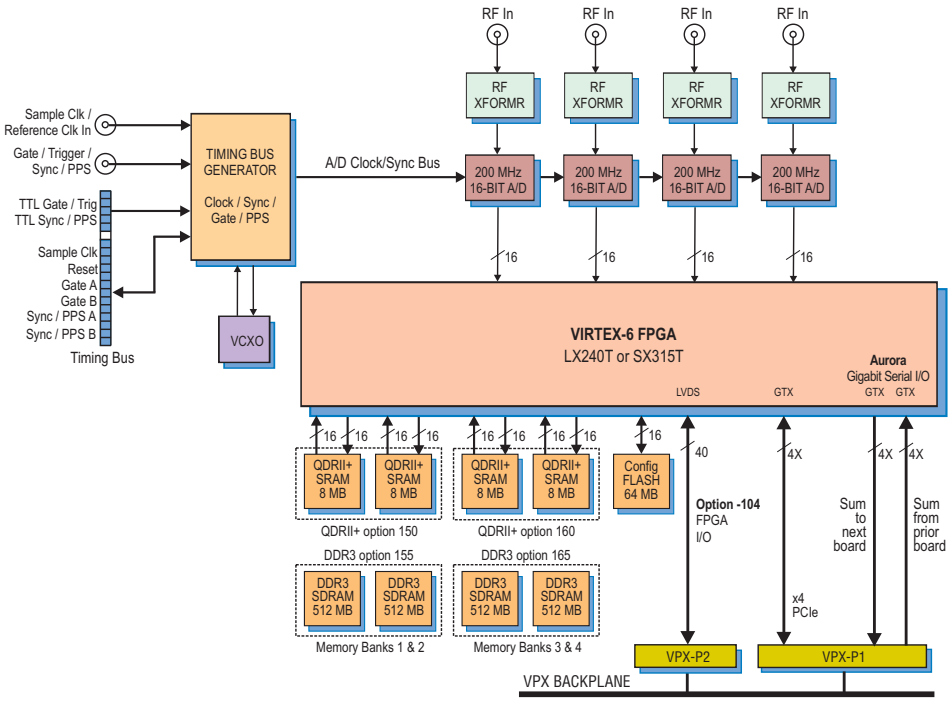
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

A/D Acquisition IP Modules

The 52664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52664 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

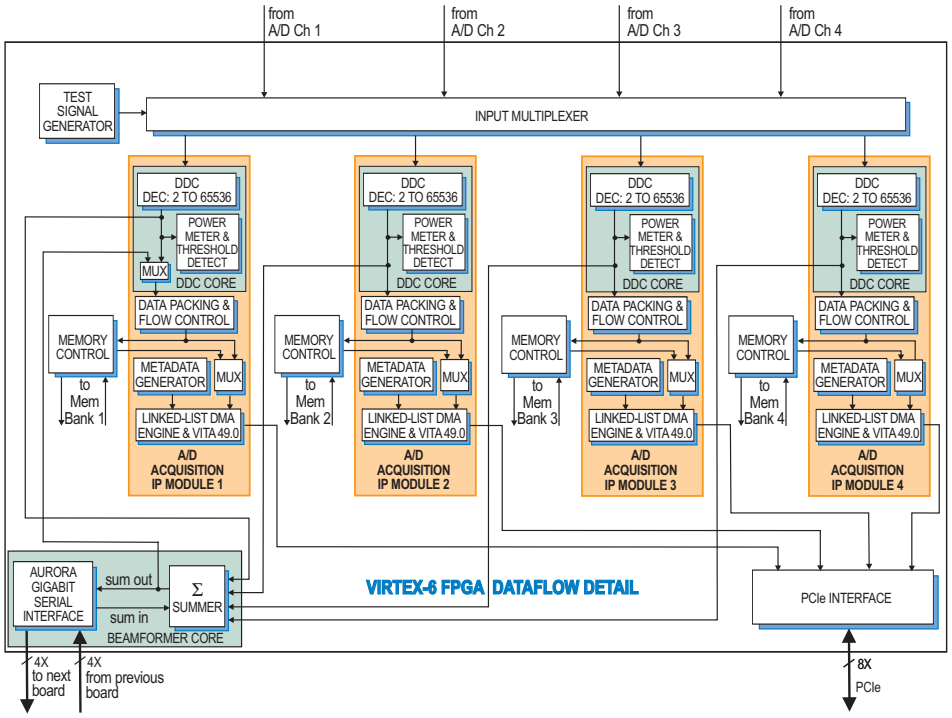
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52664's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA-49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 52664 supports fully the VITA 49.0 specification. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52664's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 52664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52664	4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Sum Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

➤

Model 52670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Model 52670 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- User-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 52670 includes general purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

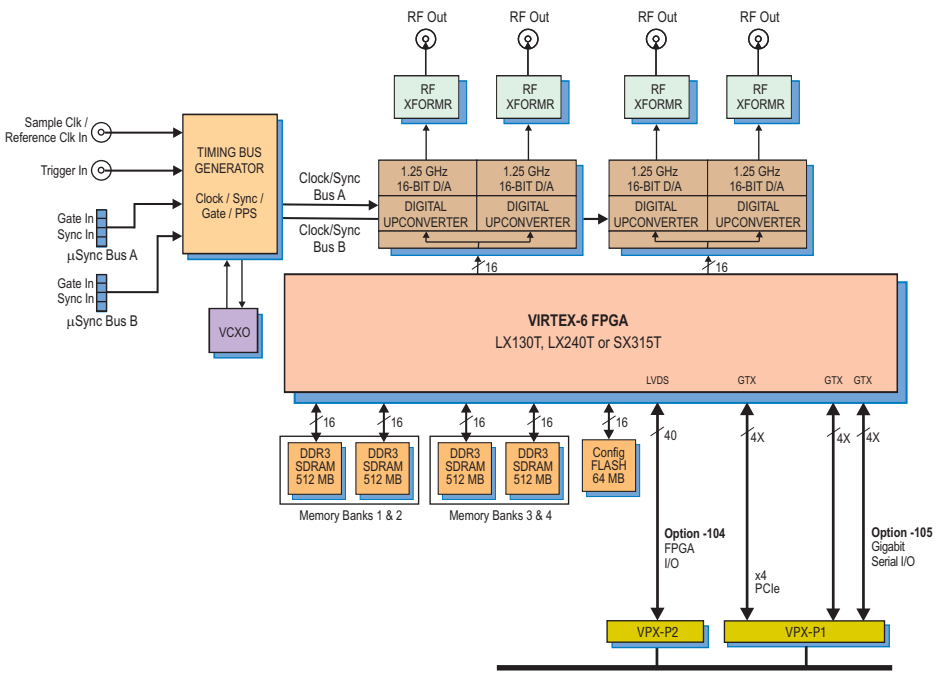
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5292 or 9192 Cobalt Synchronizers can drive multiple 52670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 52670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

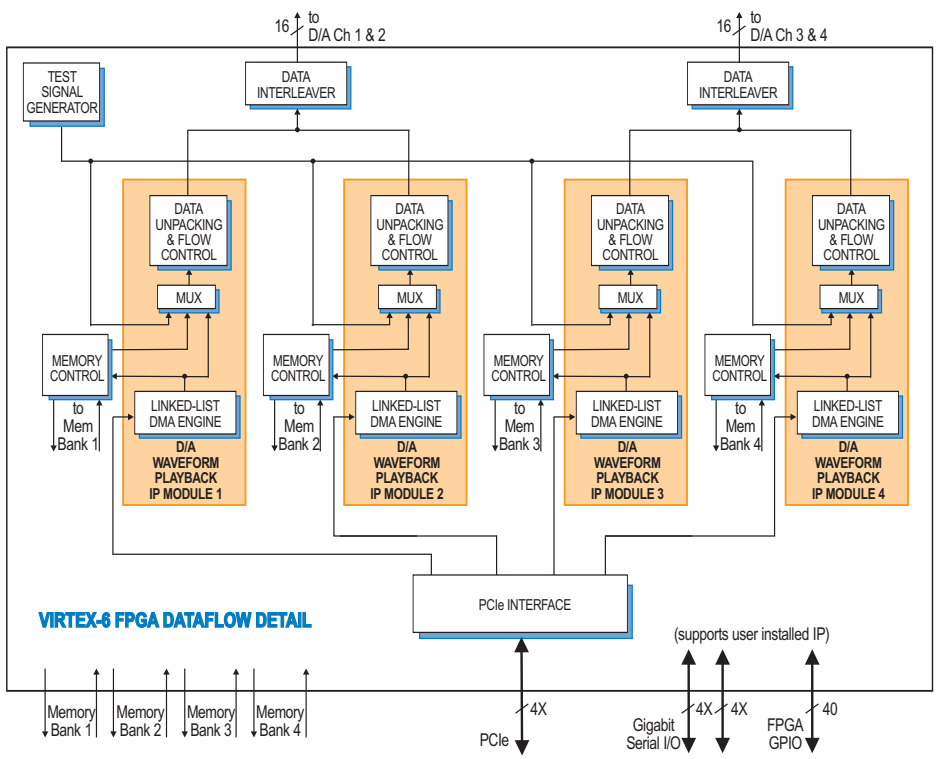
The Model 52670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x4 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

D/A Waveform Playback IP Module

The Model 52670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Model 52670 — 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Model 52671 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- Extended interpolation range from 2x to 1,048,576x
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52671 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 52671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

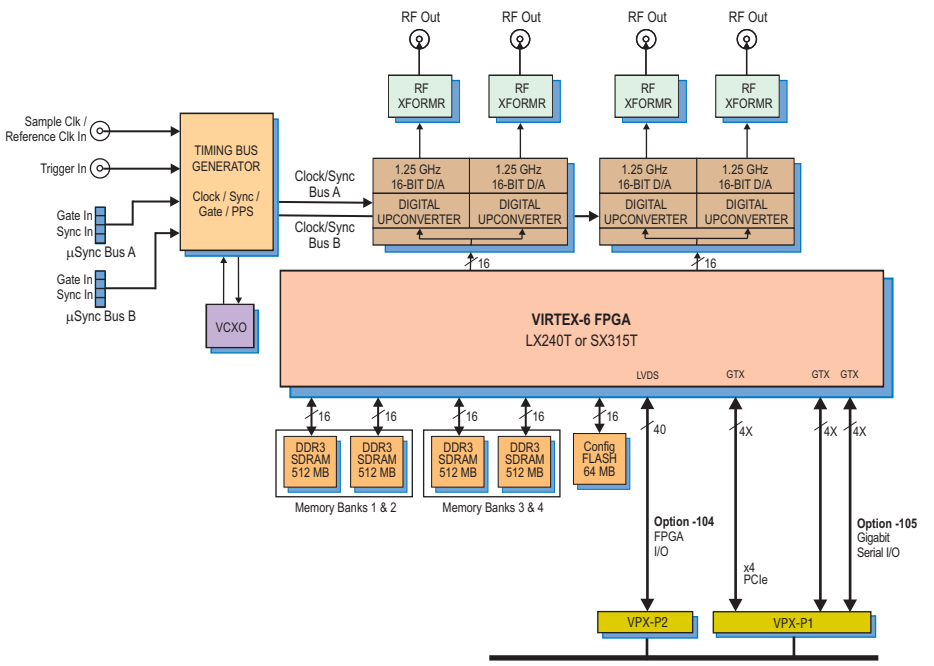
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 52671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 5292 or 9192 Cobalt Synchronizers can drive multiple 52671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 52671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

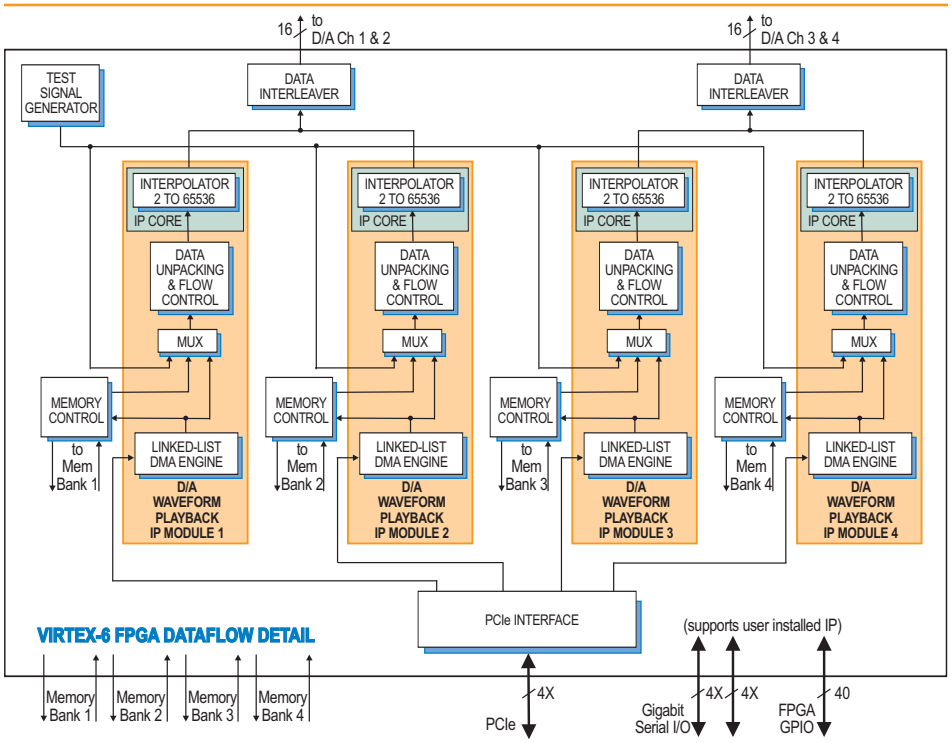
D/A Waveform Playback IP Module

The Model 52671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ PCI Express Interface

The Model 52671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x4 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array:
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

Model 52690 COTS (left) and rugged version

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 52690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

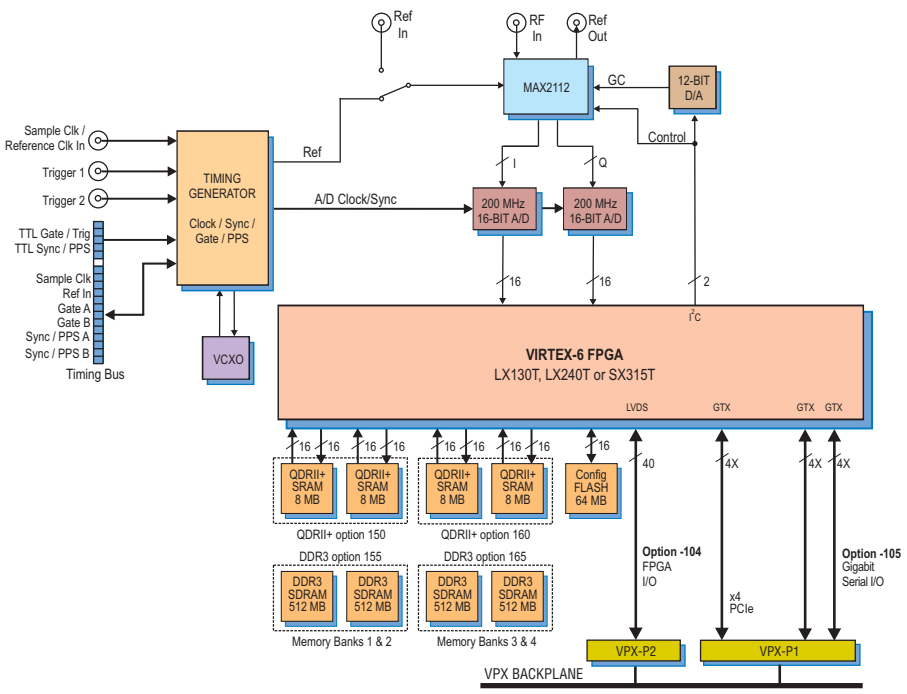
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

➤ RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

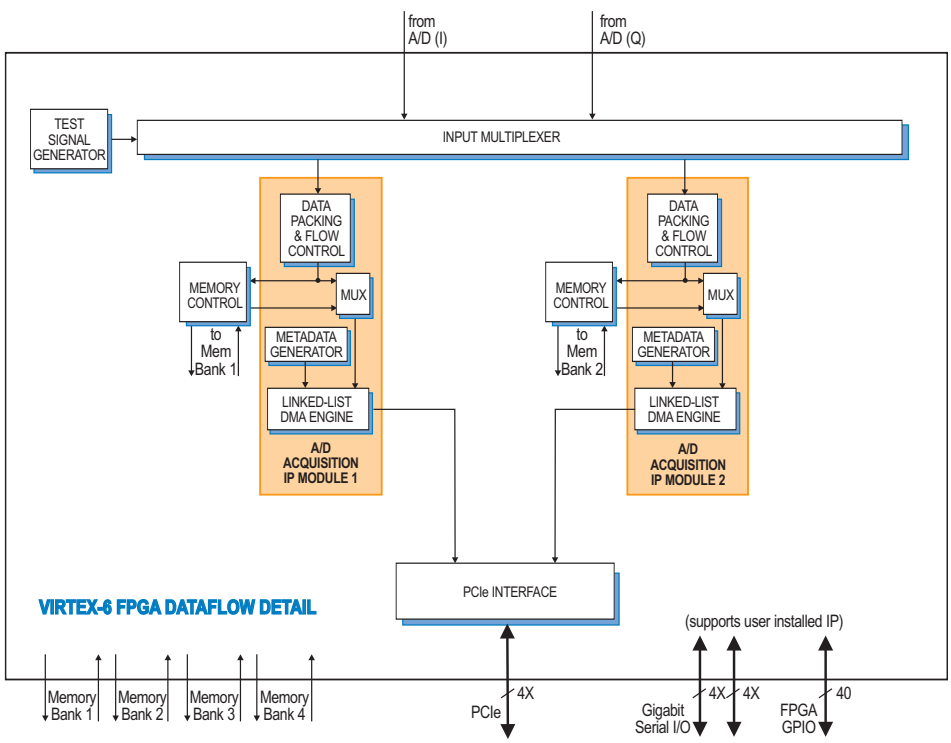
The 52690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤

A/D Acquisition IP Modules

The 52690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52690 — L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 52690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

Specifications

Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

L-Band Tuner
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference** ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- ***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

Model 52720 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x4
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52720 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52720 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

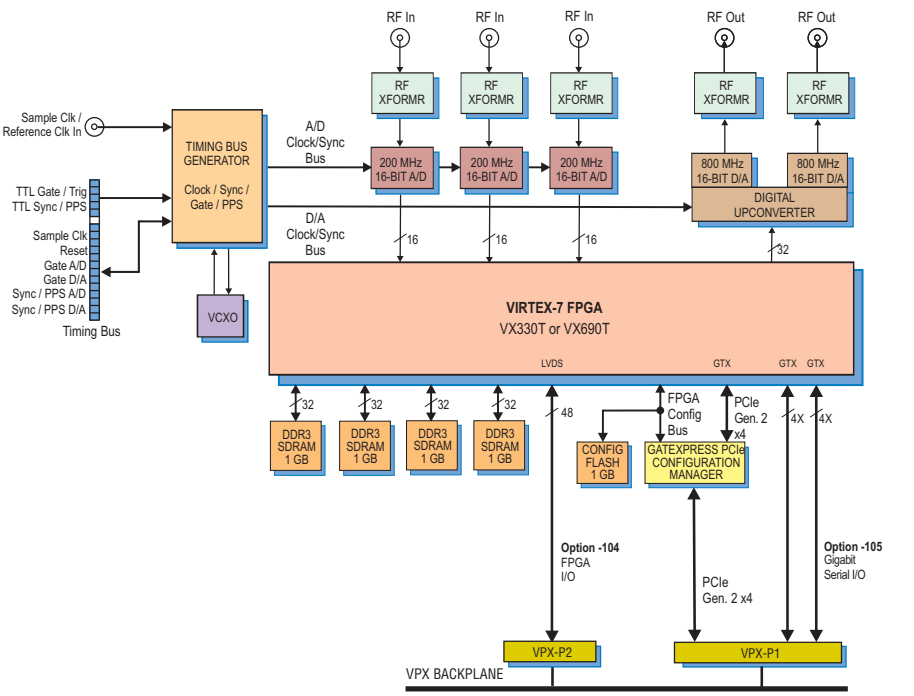
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

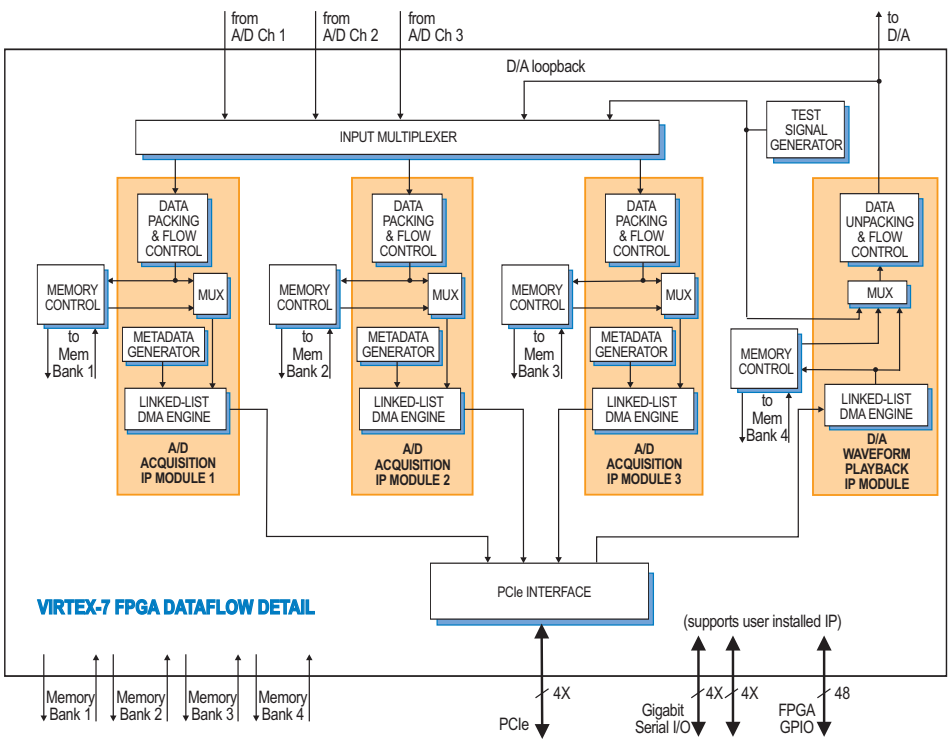
The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband ➤



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Model 52720

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

Memory Resources

The 52720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

PCI Express Interface

The Model 52720 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the VCXO.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Model 52721 COTS (left) and rugged version

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52721 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

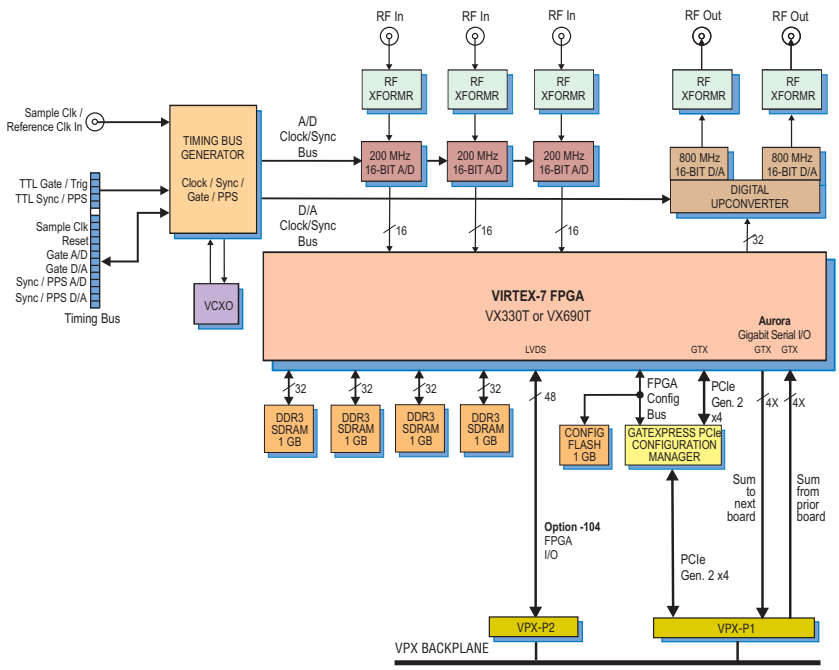
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Model 52721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

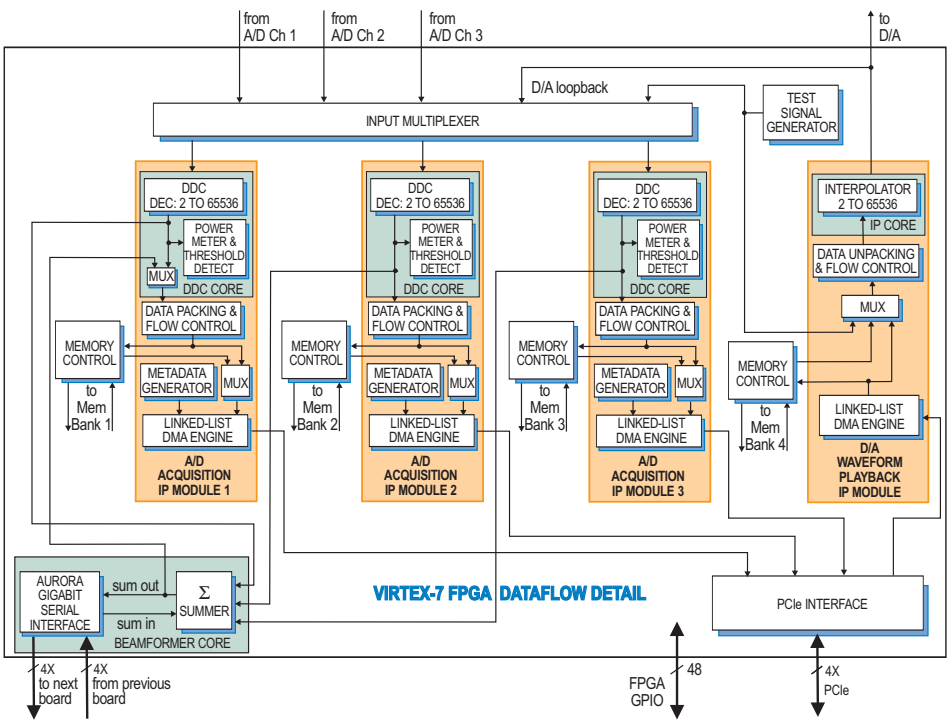
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52721's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 52721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Memory Resources

The 52721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52721's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤

Model 52721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
Input: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Model 52730 COTS (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52730 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

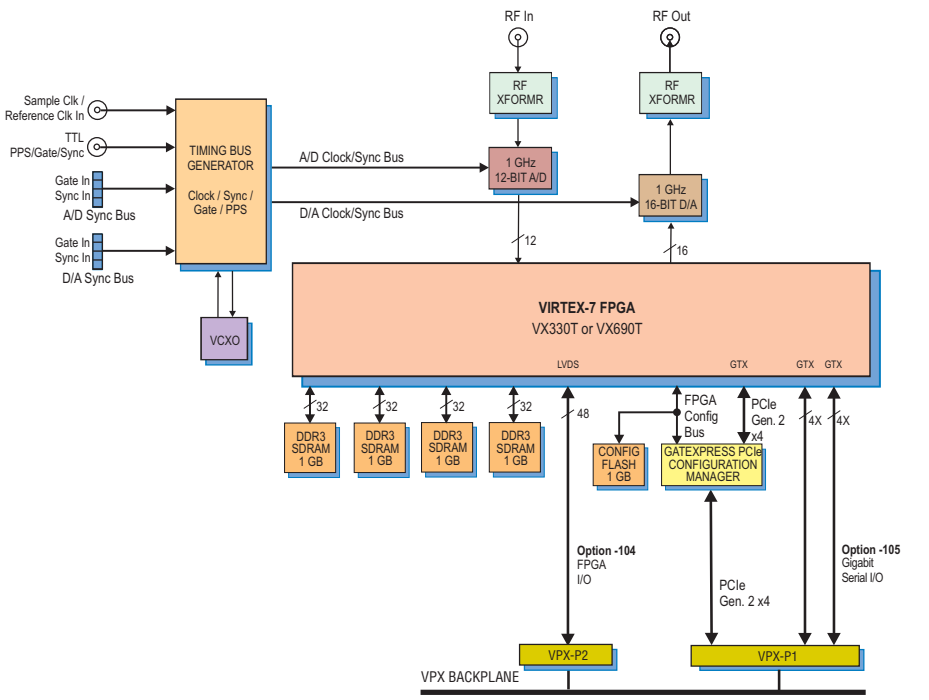
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Module

The 52730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off- board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

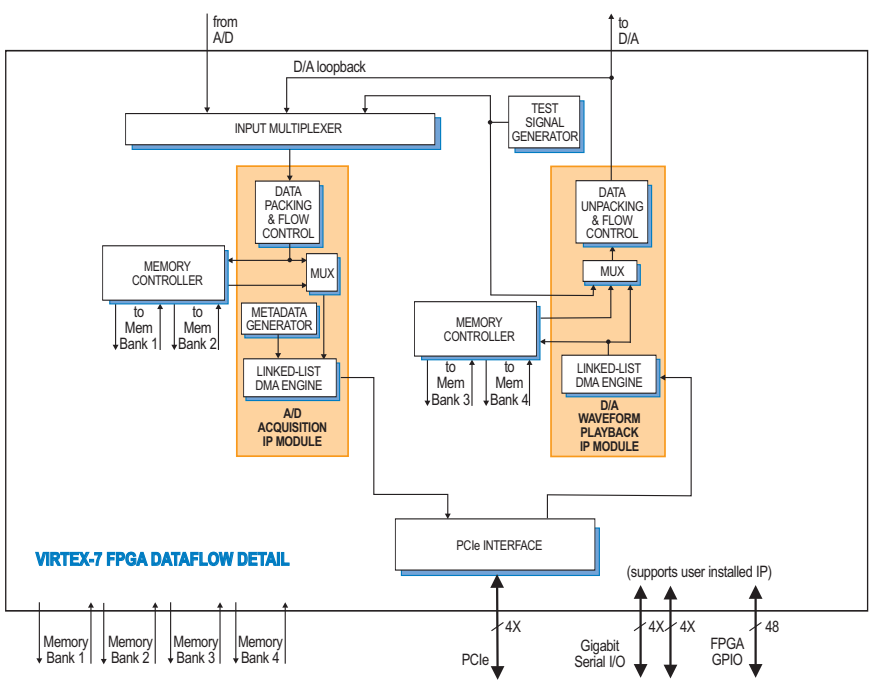
A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 52730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to acept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52730 — 1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Memory Resources

The 52730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface

The Model 52730 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52730	1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 5292 and Model 9192 Cobalt Synchronizers can drive multiple 52730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADS5400
- **Sampling Rate:** 100 MHz to 1 GHz
- **Resolution:** 12 bits

D/A Converter
- **Type:** Texas Instruments DAC5681Z
- **Input Data Rate:** 1 GHz max.
- **Interpolation Filter:** bypass, 2x or 4x
- **Output Sampling Rate:** 1 GHz max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Model 52741 COTS (left) and rugged version

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*

General Information

Model 52741 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

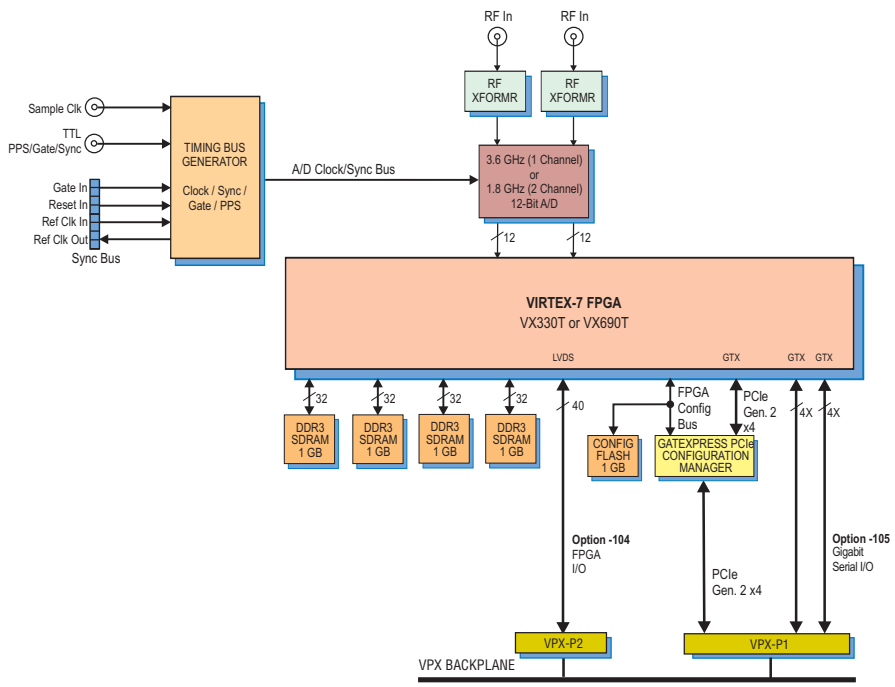
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Model 52741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Module

The 52741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

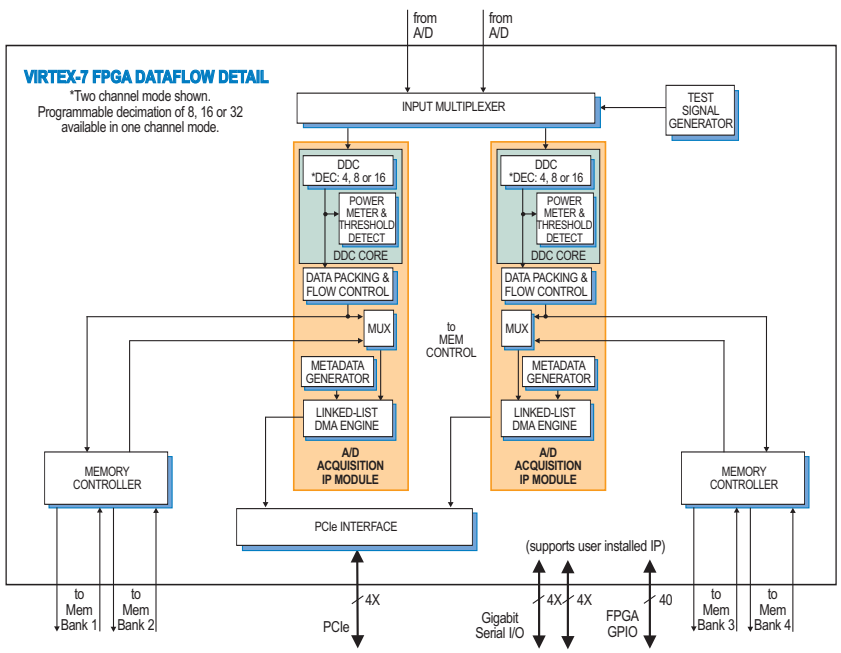
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Memory Resources

The 52741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface

The Model 52741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

Clocking and Synchronization

The 52741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 52741's can be synchronized with a simple cable. For larger systems, multiple 52741's can be synchronized using the Model 5292 high-speed sync board to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

Model 52751 commercial (left) and rugged version

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*

General Information

Model 52751 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52751 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

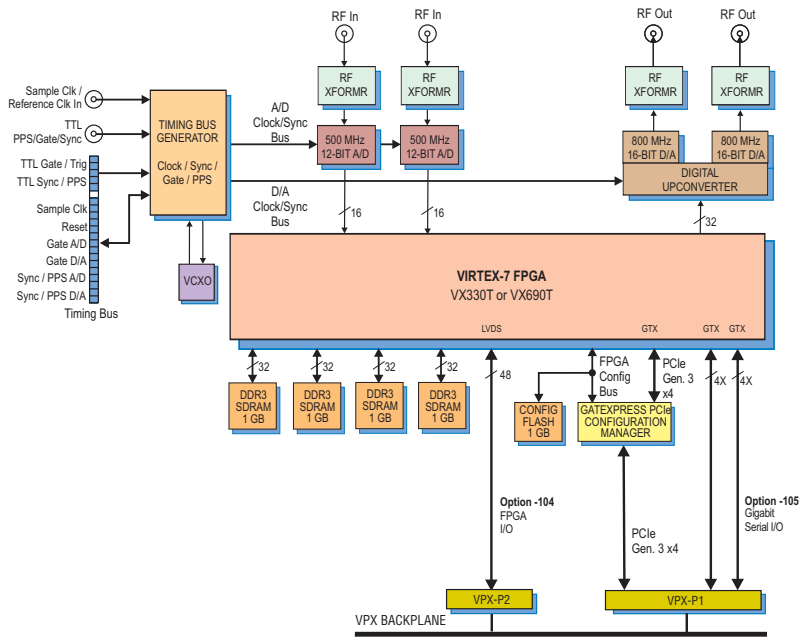
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 52751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

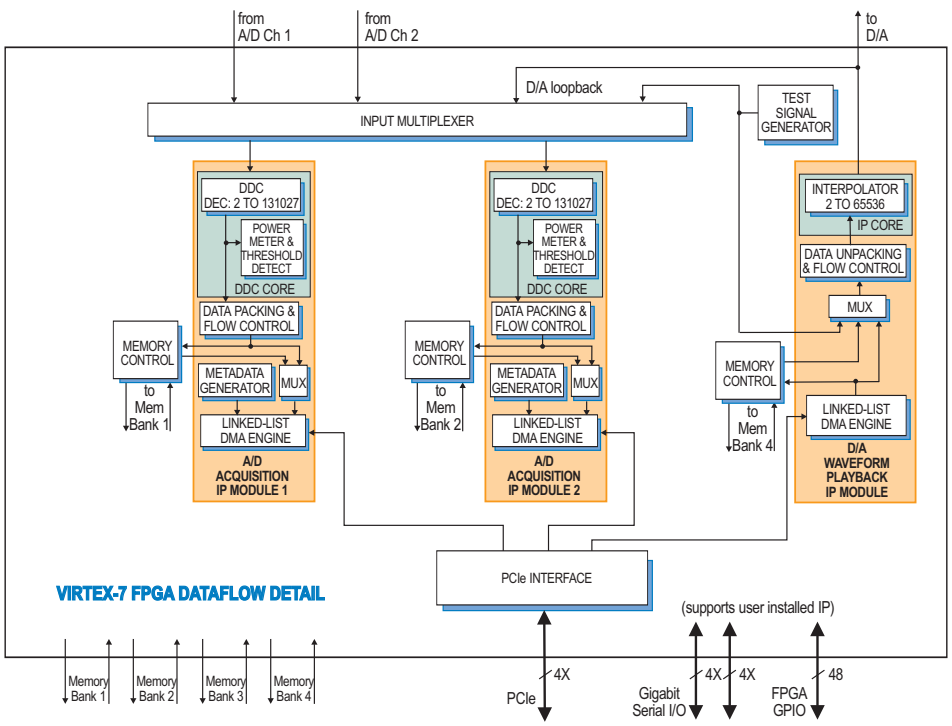
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52751's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3* bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

* Gen 3 requires a compatible backplane and SBC

Model 52751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3*: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

* Gen 3 requires a compatible backplane and SBC

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Model 52760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

Model 52760 COTS (left) and rugged version

General Information

Model 52760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52760 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

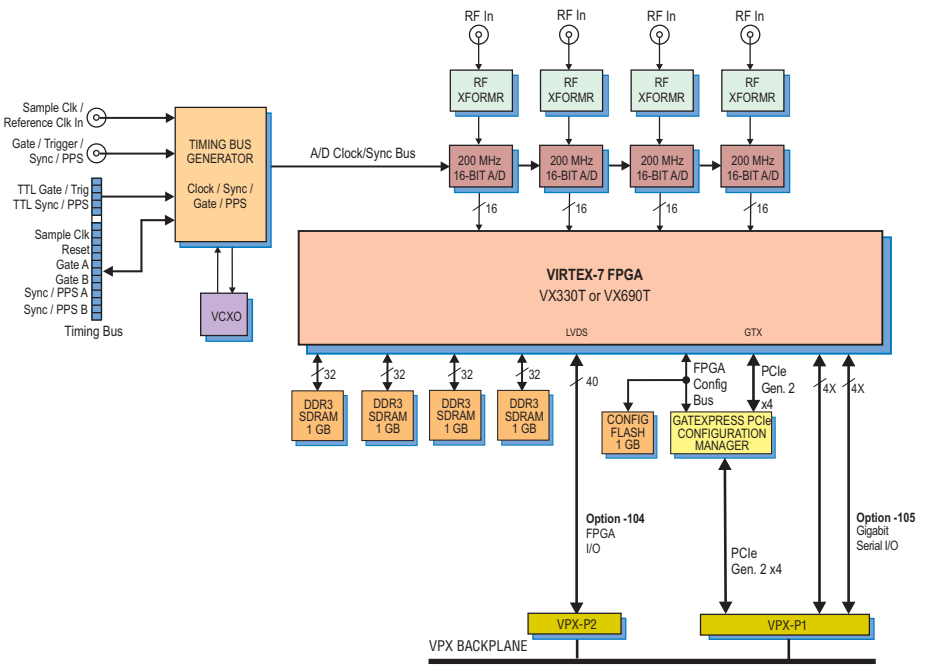
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

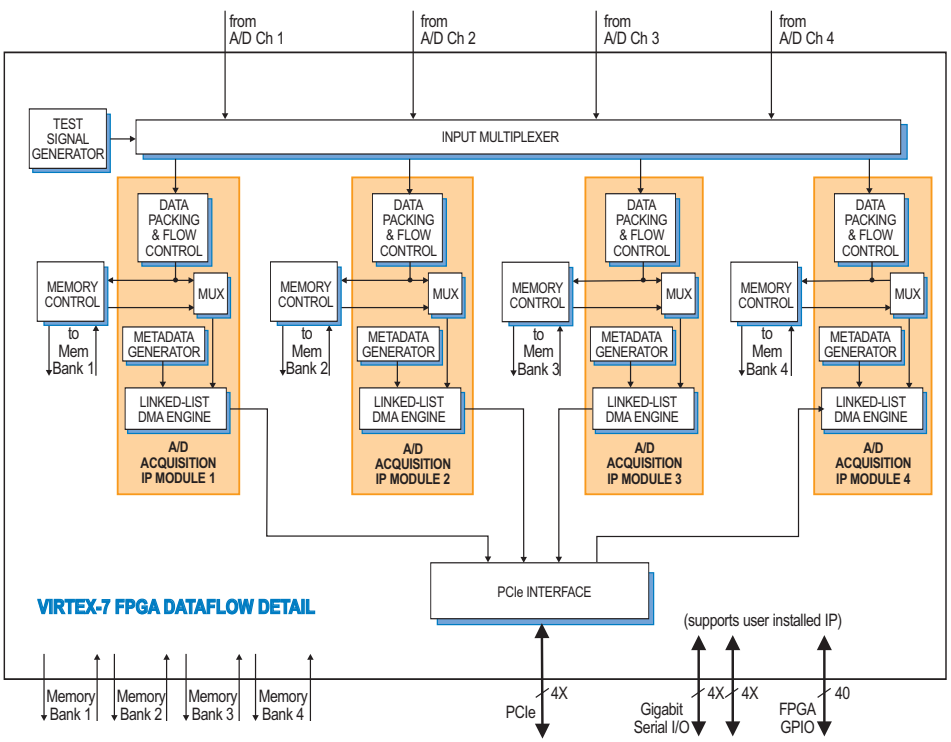
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel ➤

A/D Acquisition IP Modules

The 52760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Model 52760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

PCI Express Interface

The Model 52760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52760	4-Channel 200 MHz A/D with Virtex-7 FPGA - 3U VPX
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52760's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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Model 52761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Model 52761 COTS (left) and rugged version

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52761 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52761 includes an optional connection to the Virtex-7 FPGA for custom I/O .

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

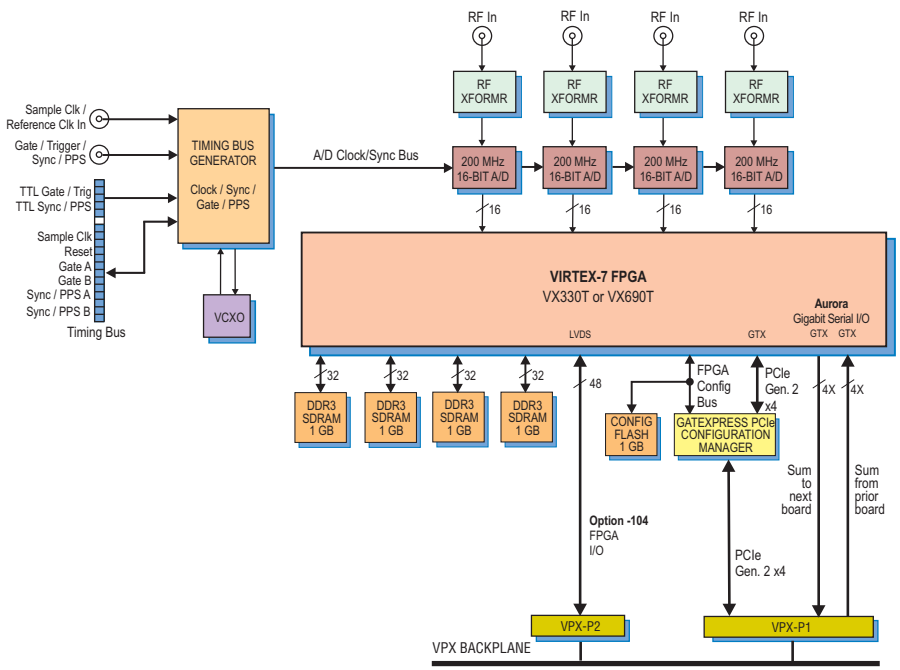
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Core

In addition to the DDCs, the 52761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

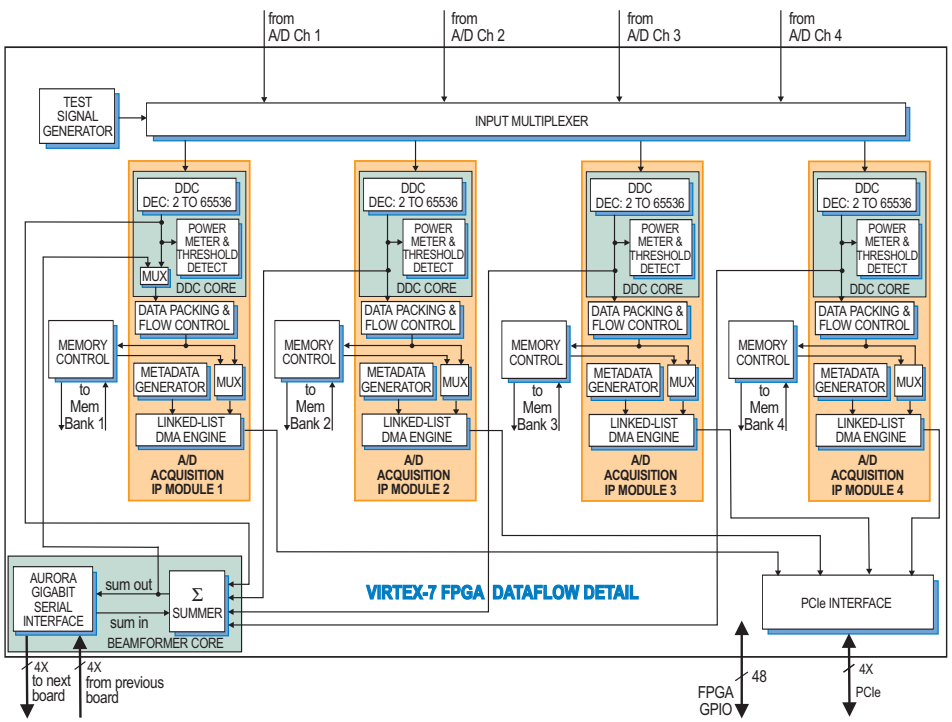
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52761's can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤



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➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 52761 — 4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52761	4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Model 52791 COTS (left) and rugged version

General Information

Model 52791 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 52791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 52791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

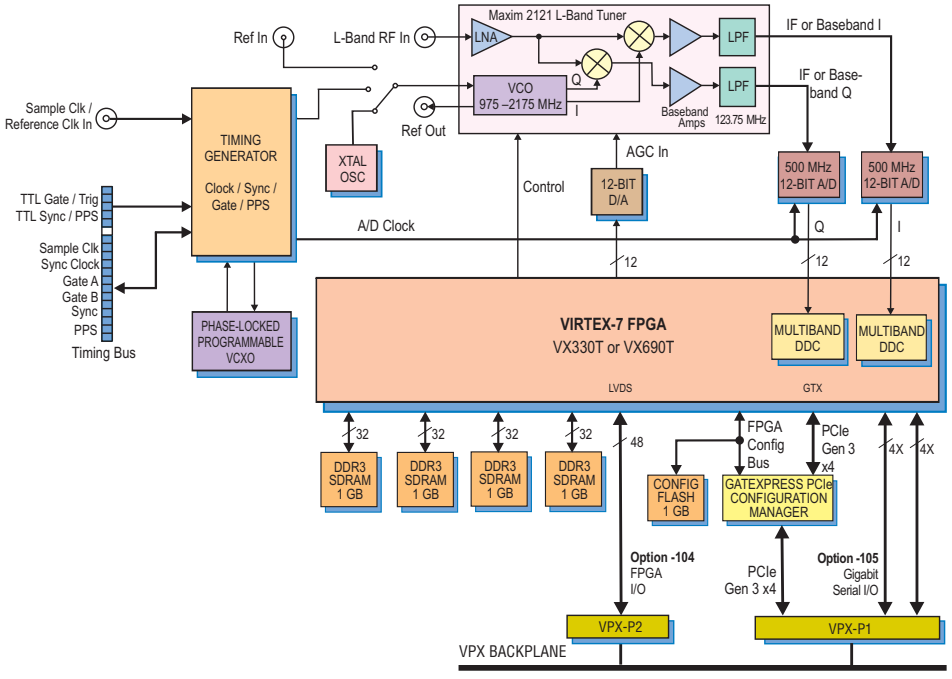
For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x4
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

A/D Acquisition IP Modules

The 52791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

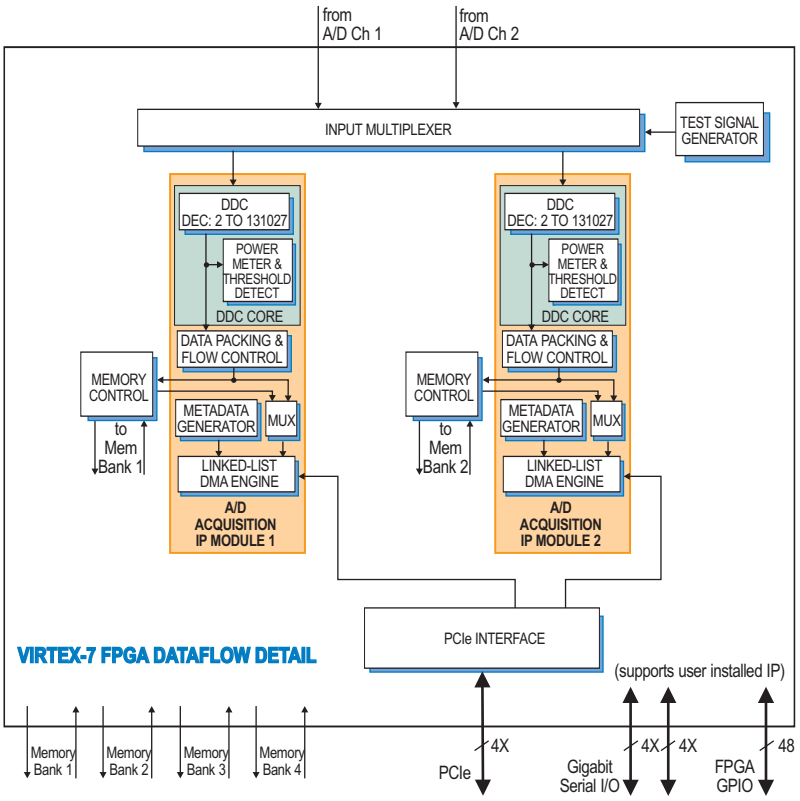
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front-panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA .

PCI Express Interface

The Model 52791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 52791

L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
52791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:

-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuner
Type: Maxim MAX2121
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: $freq_{VCO}$ = (N.F.) x $freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters
Type: Texas Instruments ADS5463
Sampling Rate: 10 MHz to 500 MHz
Resolution: 12 bits
Option -014: 400 MHz, 14-bit A/Ds

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Quantity: 2
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3*: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

* Gen 3 requires a compatible backplane and SBC

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New!

Model 52131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Model 52131 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52131 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

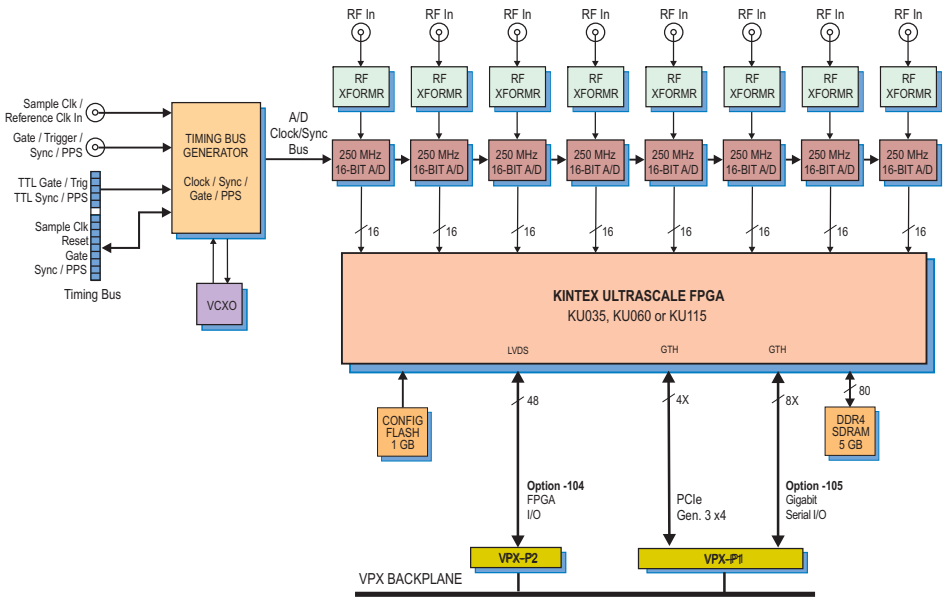
Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52131 features eightA/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

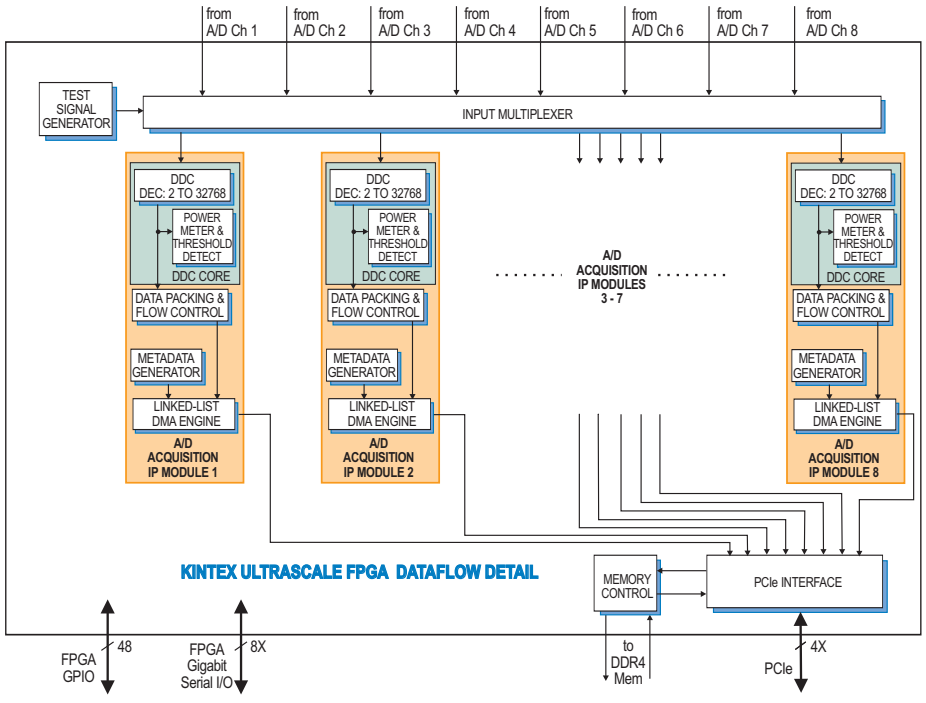
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 52131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 52131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Connects 24 LVDS pairs between the FPGA and VPX P2
- **Option -105:** Connects eight gigabit serial lanes between the FPGA and VPX P1

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100.00 mm x 170.60 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

Model 52132 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 52132 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

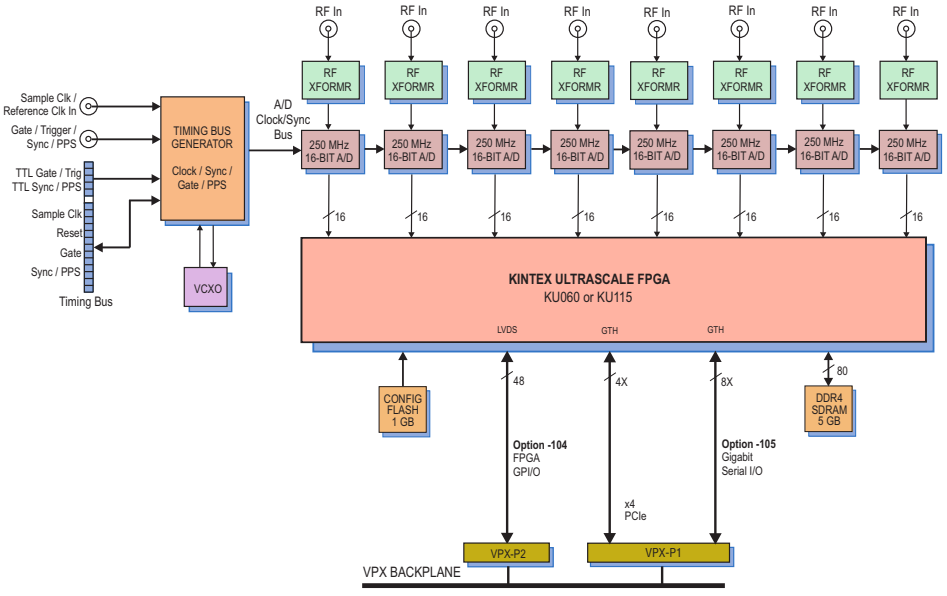
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52132 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downonversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

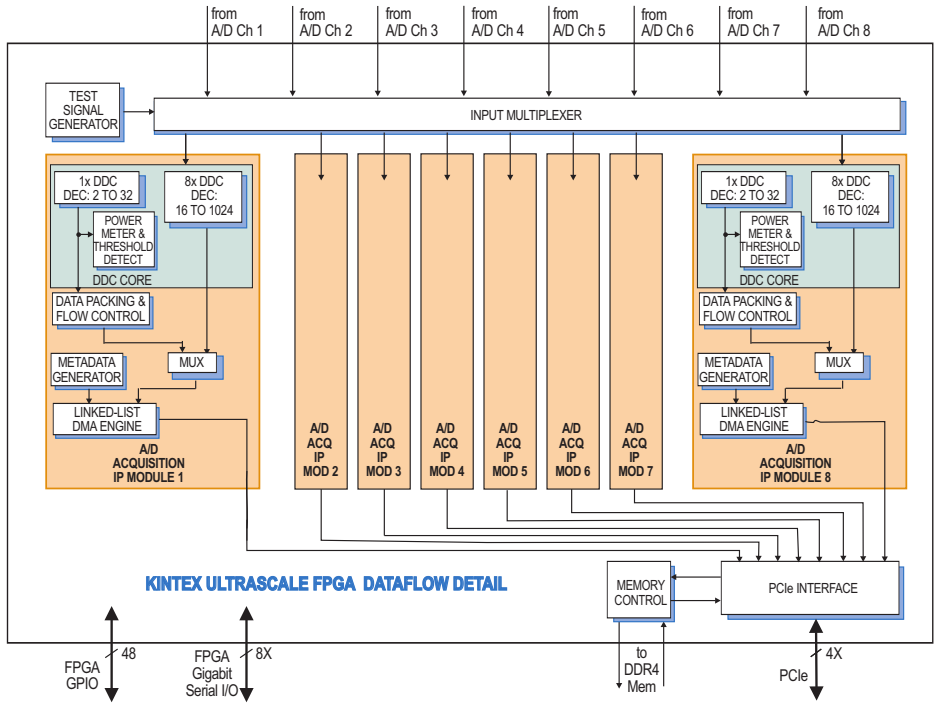
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 5293 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

➤ PCI Express Interface

The Model 52132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Eight banks, 8 channels per bank
Decimation Range: 2x to 1024x in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female MMCX connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity in all cases: 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New

Model 52141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Model 52141CORS (left) and Rygged versions

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52141 is a member of the Jade™ family of high-performance PCIe modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

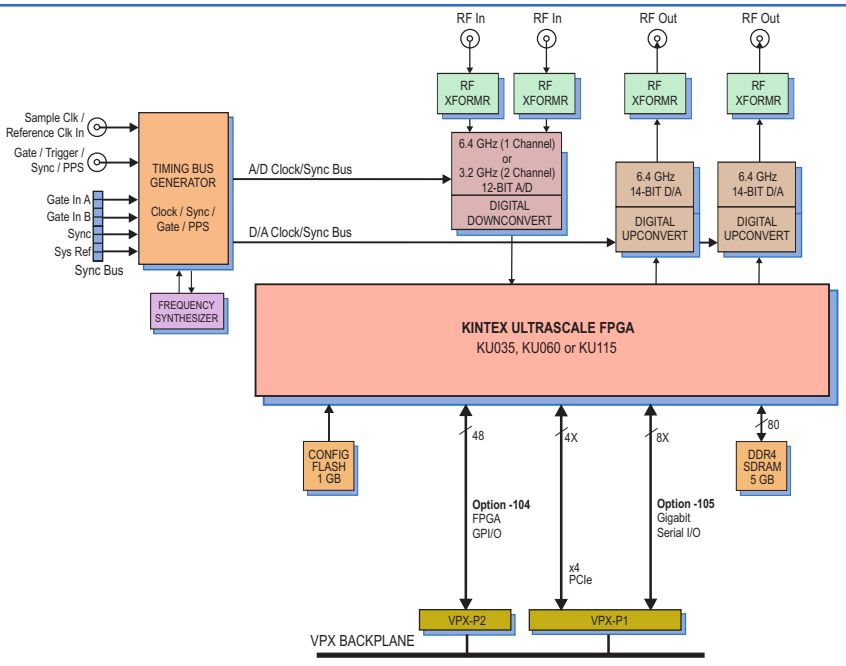
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Module

The 52141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 52141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 52141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

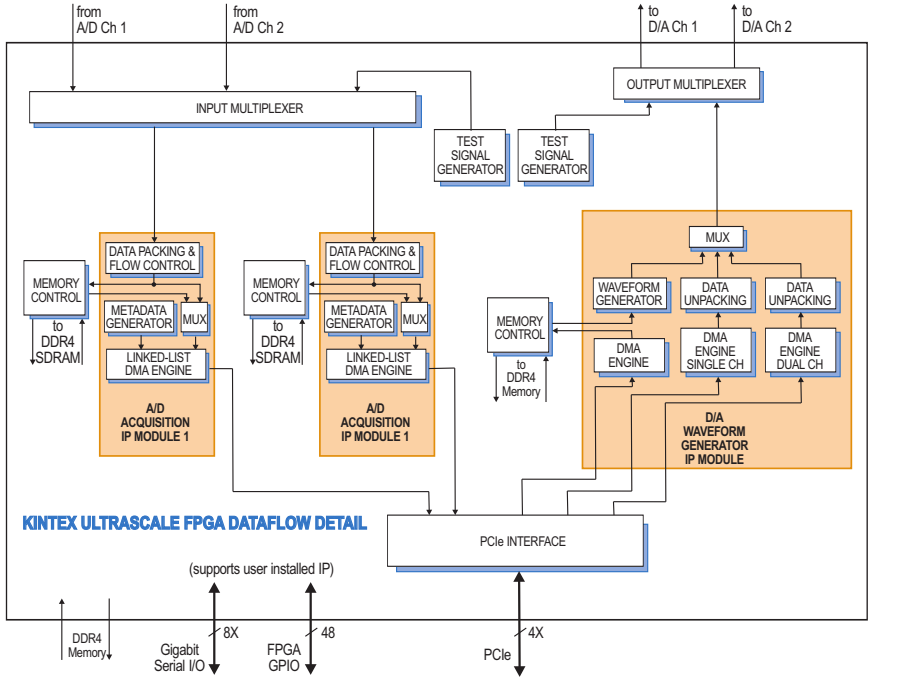
PCI Express Interface

The Model 52141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 52141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Ordering Information

Model	Description
52141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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New!

Model 52821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Model 52821 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52821 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 52821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

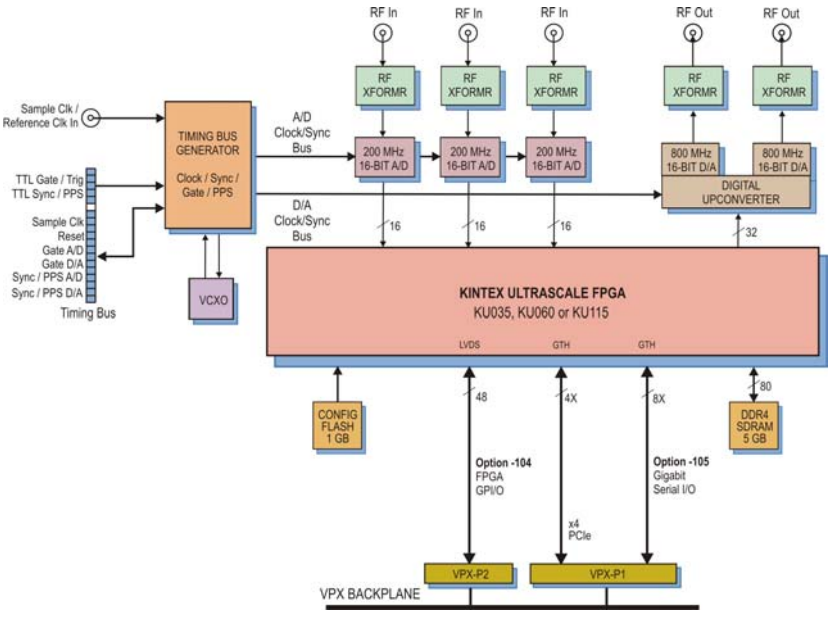
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 52821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

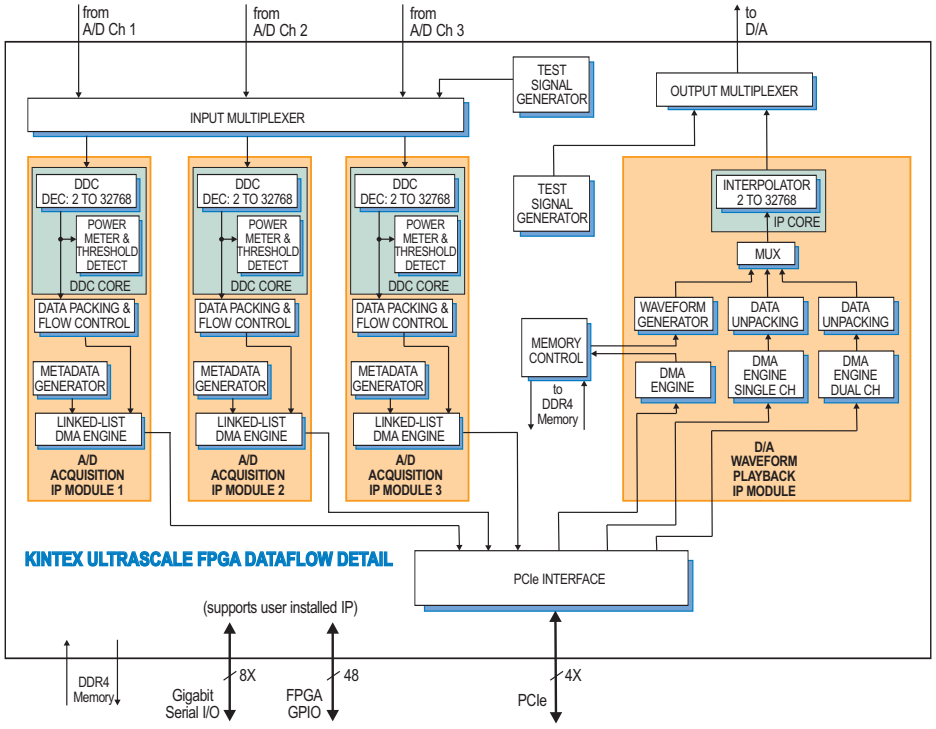
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

➤ Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

Model 52821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Digital Downconverters
Quantity: Two channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core
Interpolation Range: 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3U VPX board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

New!

Model 52841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Model 52841 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Down-converter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52841 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52841 is a high-speed data converter with programmable DDCs (digital down-converters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

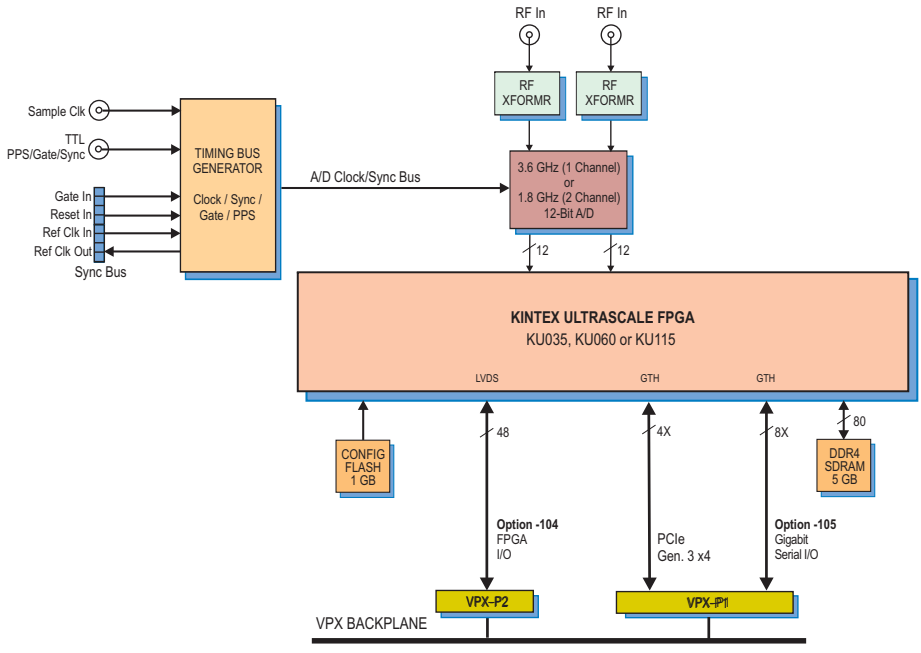
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Module

The 52841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has an associated 5 GB memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

A/D Converter Stage

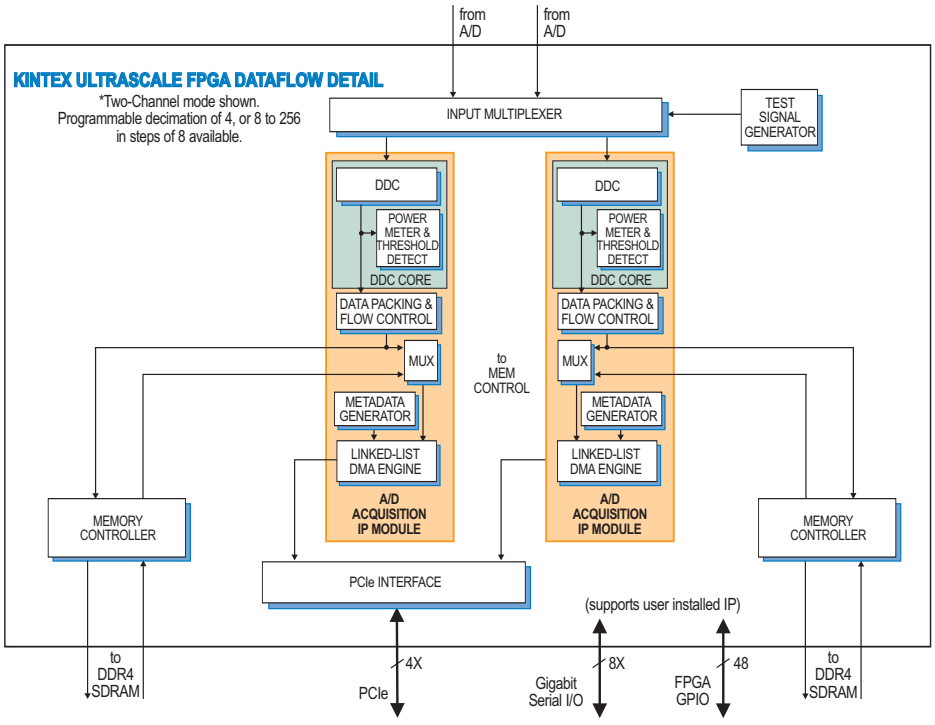
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

PCI Express Interface

The Model 52841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤



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Model 52841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Memory Resources

The 52861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Ordering Information

Model	Description
52841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Clocking and Synchronization

The 52841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 52841's can be synchronized with a simple cable. For larger systems, multiple 52841's can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input Level:** may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Single-channel mode:** decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** the DDC can be bypassed completely
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Connects 24 LVDS pairs between the FPGA and VPX P2
- **Option -105:** Connects eight gigabit serial lanes between the FPGA and VPX P1

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4; Subject to speed limitations of backplane and SBC

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Model 52851 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Model 52851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

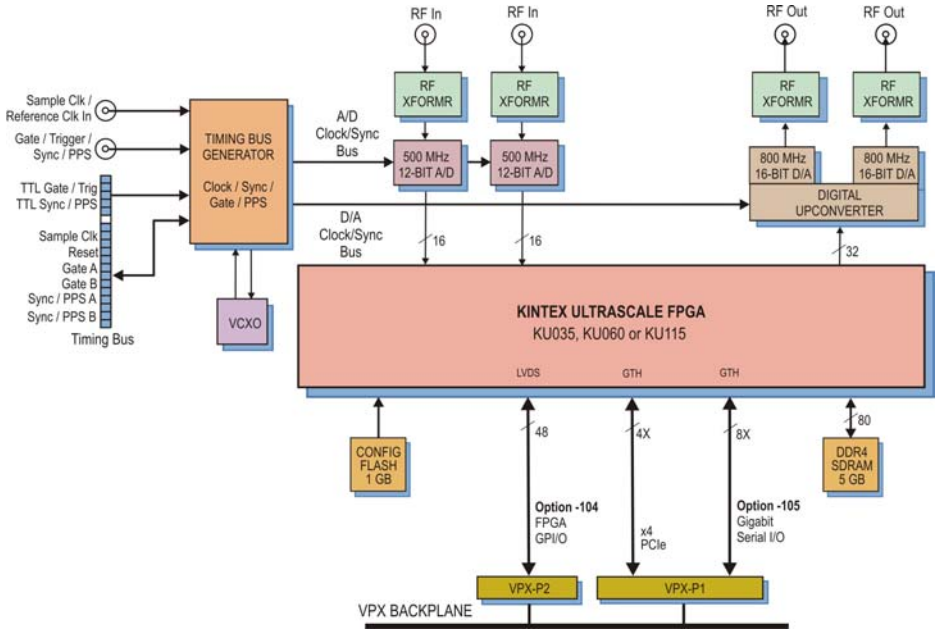
The 52851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Model 52851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The Model 71851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

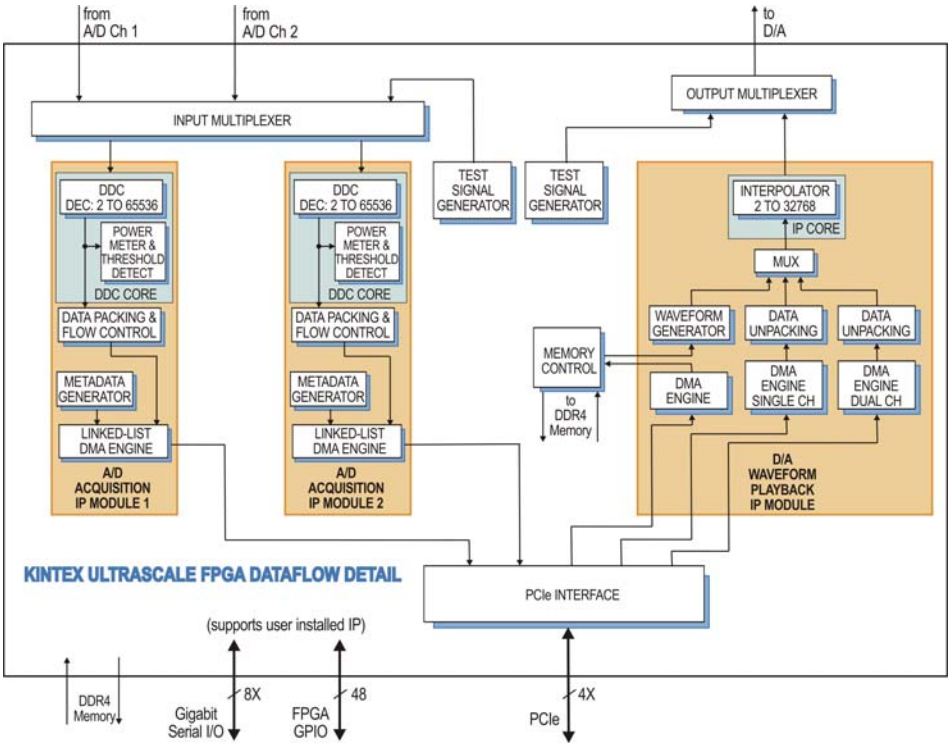
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014)

Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Model 52851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2 connector
-105	Gigabit serial FPGA I/O through VPX P1 connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ **Digital Downconverters**
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3U VPX board 3.937 in x 6.717 in (100.00 mm x 170.61 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

New!

Model 52861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Model 52861 COTS (left) and rugged version

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52861 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

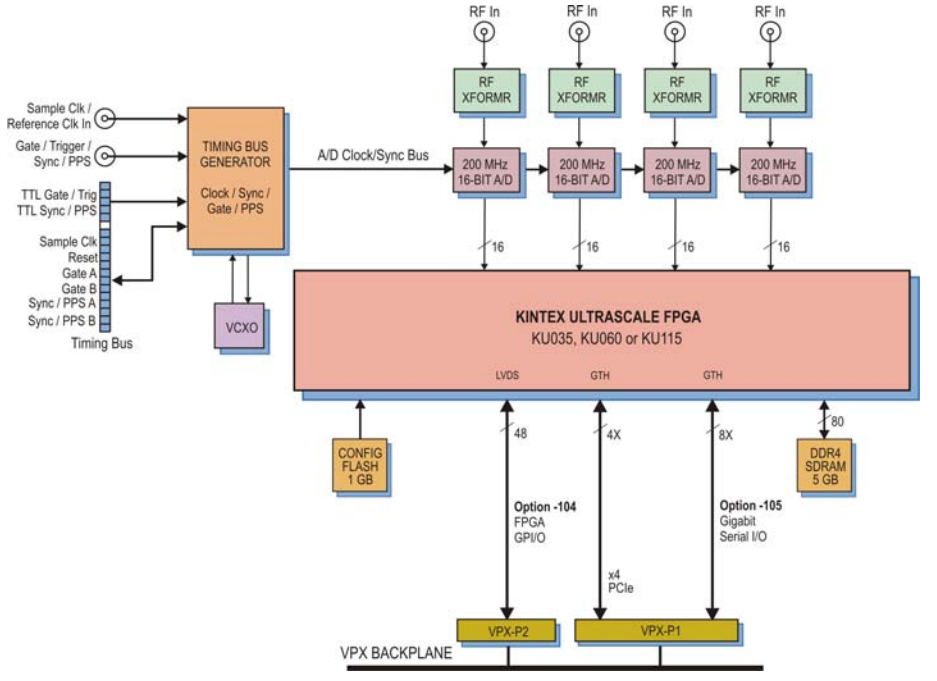
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 52861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

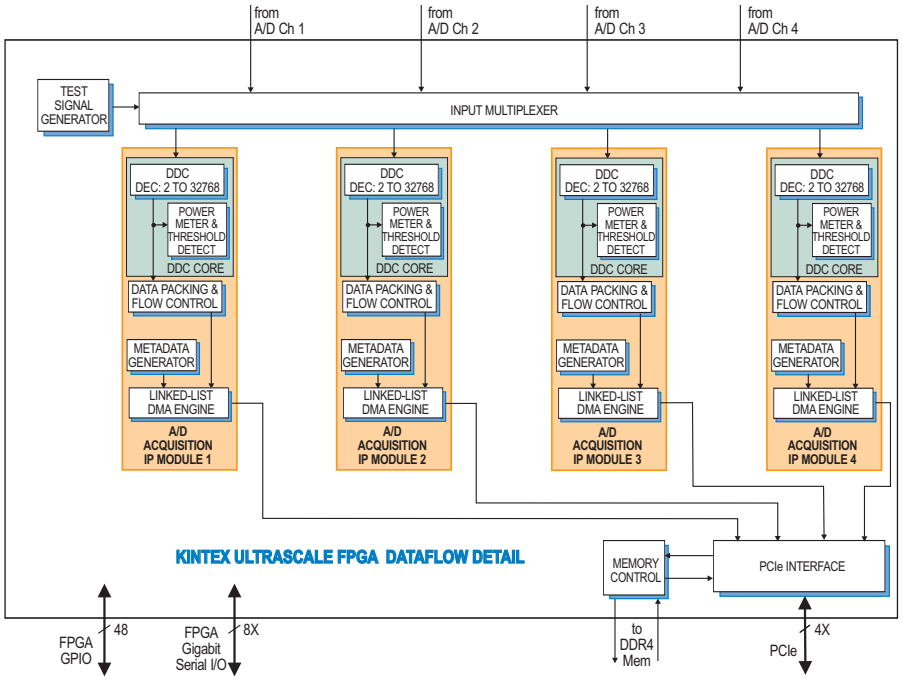
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 52861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 52861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

Model 52862 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52862 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

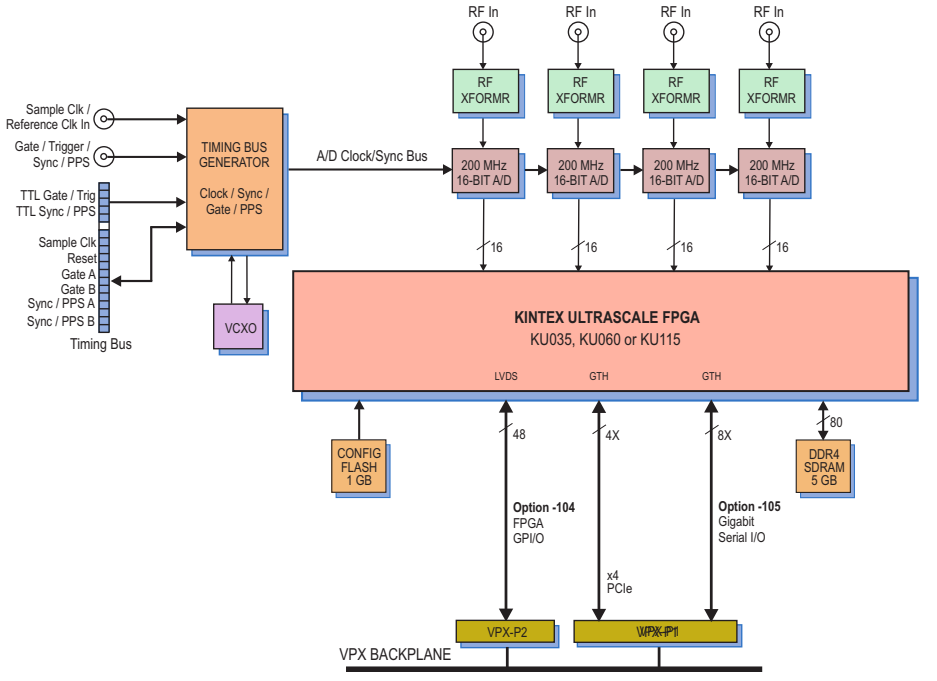
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 52862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

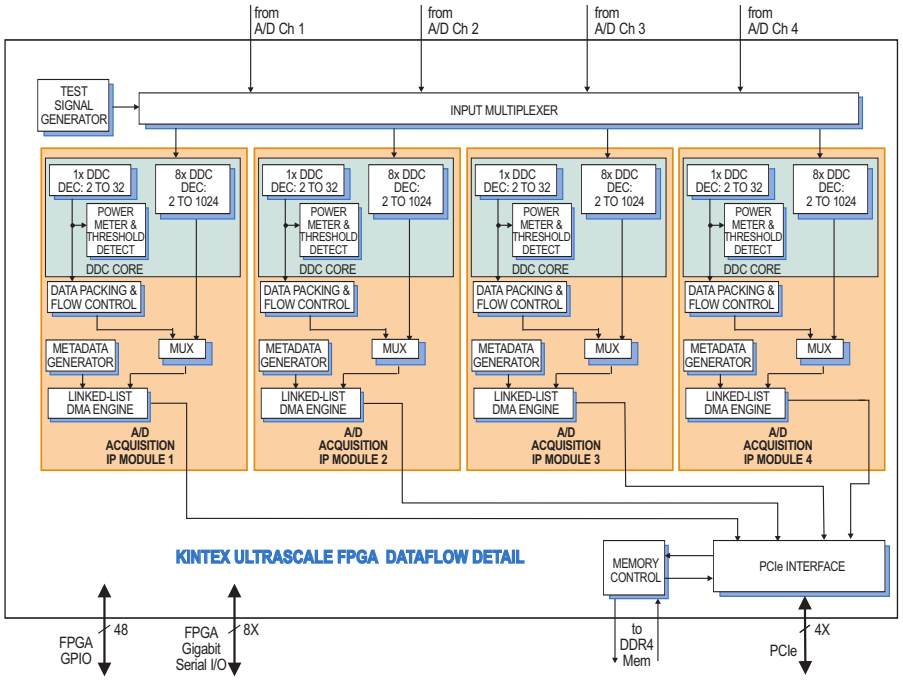
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 52862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

➤ PCI Express Interface

The Model 52862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Four channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Four banks, 8 channels per bank
Decimation Range: 2x to 1024x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity in all cases: 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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New!

Model 52800

Kintex UltraScale FPGA Coprocessor- 3U VPX

Model 5280 COTS (left) and rugged version

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Model 52800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 52800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

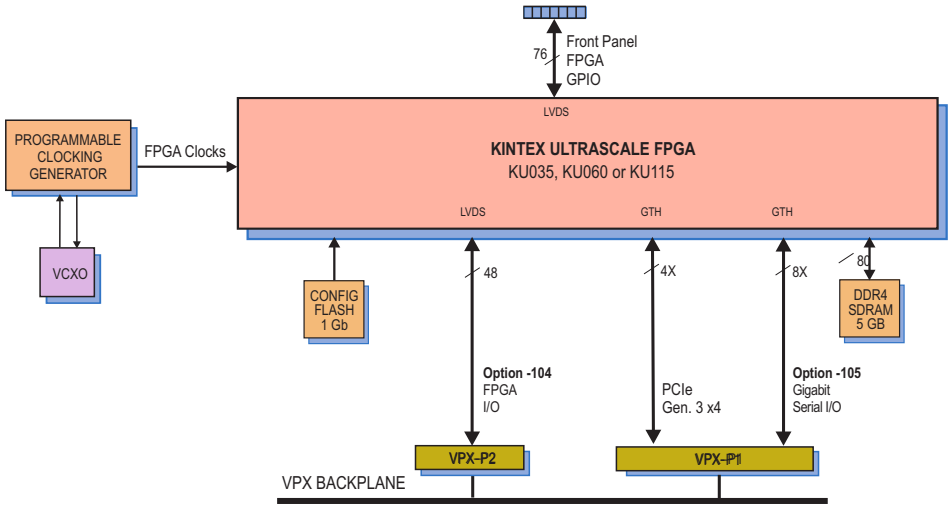
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Front Panel Digital I/O Interface

The 52800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 52800

Kintex UltraScale FPGA Coprocessor- 3U VPX

➤ PCI Express Interface

The Model 52800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. \

Memory Resources

The 52800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8264), or a 6U VPX chassis (Model 8267), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
52800	Kintex UltraScale FPGA Coprocessor - 3U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity in all options:** 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

VPX Families

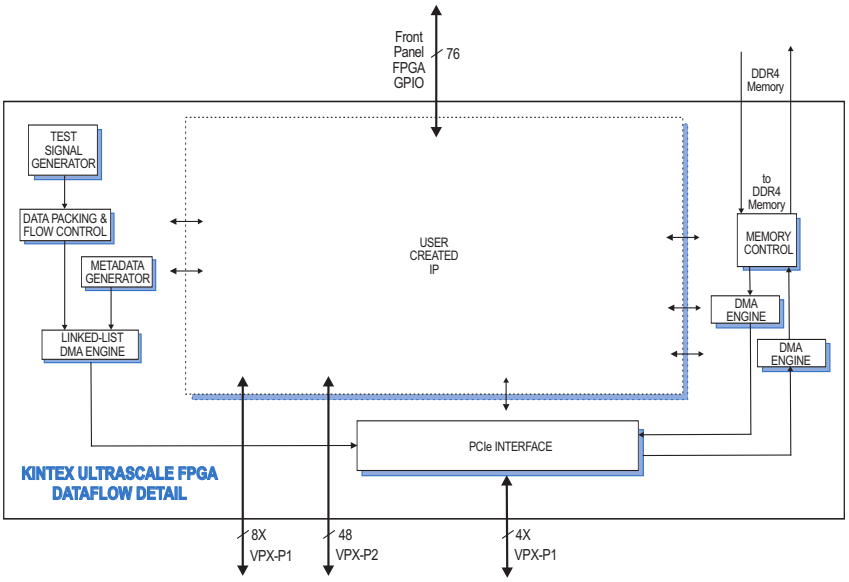
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 5220

Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

Model 5220 COTS (left) and rugged version

Bandit ReadyFlow Board Support Package

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

General Information

The Bandit® Model 5220 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded 3U VPX board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5220 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5220 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5220 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5220 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

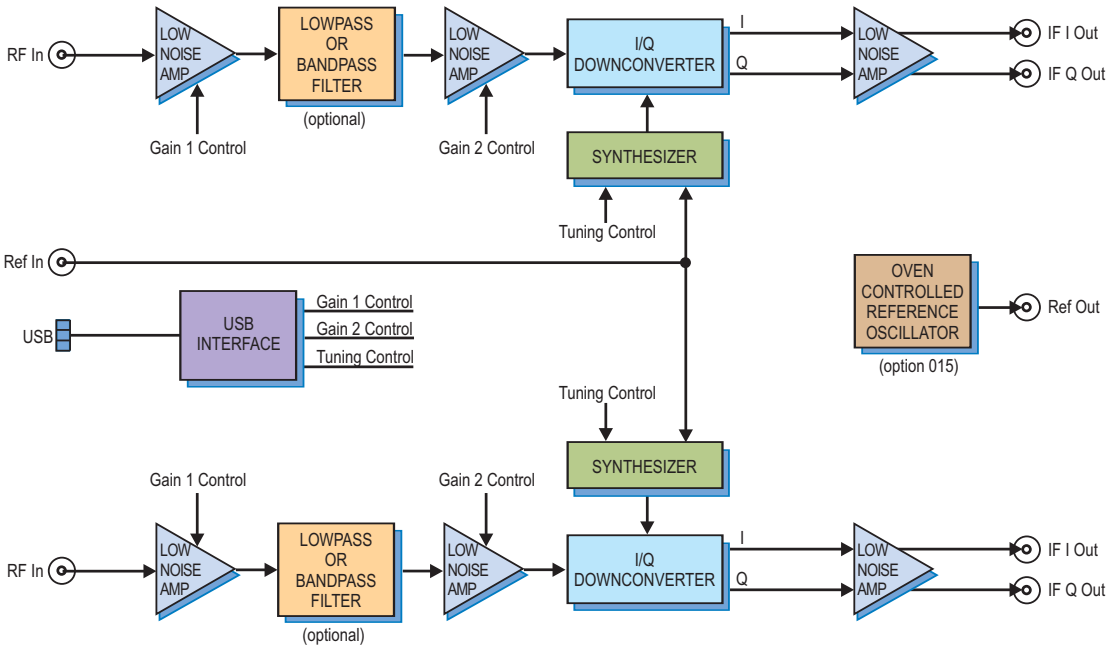
On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5220 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 5220

Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

➤ Specifications

RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** –60 dBm to –20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

Phase Noise
- **1 kHz:** –90 dBc/Hz
- **100 kHz:** –110 dBc/Hz
- **1 MHz:** –130 dBc/Hz

Noise Figure (referred to input)
- **60 dB gain:** 2.6 dB

Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedence:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

Reference Output Signal
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm
- **Aging**
  - **Daily:** ±10 ppb/day
  - **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm
- **Phase Noise**
  - **1 Hz Offset:** –67 dBc/Hz
  - **10 Hz Offset:** –100 dBc/Hz
  - **100 Hz Offset:** –130 dBc/Hz
  - **1 KHz Offset:** –148 dBc/Hz
  - **10 KHz Offset:** –154 dBc/Hz
  - **100 KHz Offset:** –155 dBc/Hz

IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

PCI Express Interface
- **PCIe Bus:** x4, power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5220	Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

Option	Description
-015	Oven Controlled Reference Oscillator
-145	1.45 GHz lowpass input filter
-280	2.80 GHz lowpass input filter

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New!

Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 9-slot, 4U 19-inch rackmount, 12-inch deep chassis which houses 3U VPX boards
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box ready-to-run examples

Ordering Information

Model	Description
8267	3U VPX Development System for Cobalt, Onyx and Flexor Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS
-101	Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

General Information

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies gurantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

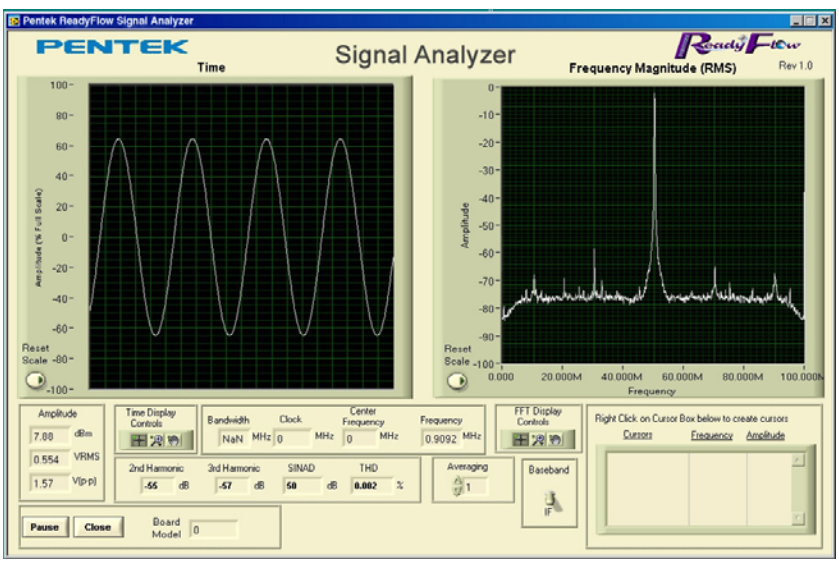
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and extended memory support.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19" W x 12" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



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RADAR & SDR I/O - 6U VPX

MODEL	DESCRIPTION
Cobalt 57620 & 58620	3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U VPX
Cobalt 57621 & 58621	3/6-Ch 200 MHz A/D, DDCs, DUC, 2/4-Ch. 800 MHz D/A, Virtex-6 FPGA - 6U VPX
Cobalt 57624 & 58624	2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - 6U VPX
Cobalt 57630 & 58630	1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U VPX
Cobalt 57640 & 58640	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 6U VPX
Cobalt 57641 & 58641	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 6U VPX
Cobalt 57650 & 58650	2/4 500 MHz A/Ds, 1/2 DUCs, 2/4 800 MHz D/As, Virtex-6 FPGA - 6U VPX
Cobalt 57651 & 58651	2/4-Ch 500 MHz A/D w. DDC, DUC w. 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U VPX
Cobalt 57660 & 58660	4/8-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 6U VPX
Cobalt 57661 & 58661	4/8-Ch 200 MHz A/D with DDCs, Beamformer and Virtex-6 FPGA - 6U VPX
Cobalt 57662 & 58662	4/8-Ch 200 MHz A/D with 32/64-Ch DDC and Virtex-6 FPGA - 6U VPX
Cobalt 57663 & 58663	1100/2200-Channel GSM Channelizer with Quad or Octal A/D - 6U VPX
Cobalt 57664 & 58664	4/8-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 6U VPX
Cobalt 57670 & 58670	4/8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U VPX
Cobalt 57671 & 58671	4/8-Ch 1.25 GHz D/A with DUC, Extend. Interpol. and Virtex-6 FPGA - 6U VPX
Cobalt 57690 & 58690	1/2-Ch L-Band RF Tuner, 2/4-Ch 200 MHz A/D, Virtex-6 FPGA - 6U VPX
Onyx 57720 & 58720	3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX
Onyx 57721 & 58721	3/6-Ch 200 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX
Onyx 57730 & 58730	1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-7 FPGA - 6U VPX
Onyx 57741 & 58741	1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz, 12-bit A/D, DDC,Virtex-7 FPGA - 6U VPX
Onyx 57751 & 58751	2/4-Ch 500 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX
Onyx 57760 & 58760	4/8-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U VPX
Onyx 57761 & 58761	4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 6U VPX
Onyx 57791 & 58791	L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 6U VPX
Jade 57131 & 58131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
Jade 57132 & 58132	8-Channel 250 MHz A/D with Multiband DDCs and Kintex FPGA - 6U VPX
Jade 57141 & 58141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex FPGA - 6U VPX
Jade 57821 & 58821	3-Channel 200 MHz A/D, DDC, DUC 2-Channel 800 MHz D/A, Kintex FPGA - 6U VPX
Jade 57841& 58841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex FPGA - 6U VPX
Jade 57851& 58851	2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex FPGA - 6U VPX
Jade 57861 & 58861	4-Channel 200 MHz A/D with DDcs and Kintex UltraScale FPGA - 6U VPX
Jade 57862 & 58862	4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - 6U VPX
Jade 57800 & 58800	Kintex UltraScale FPGA Coprocessor - 6U VPX
8264	Development System for 6U VPX Cobalt, Onyx, Jade, Flexor, and Jade boards

Customer Information

Click Here for the PRODUCT SELECTOR

RADAR & SDR I/O - PMC/XMC
RADAR & SDR I/O - CompactPCI
RADAR & SDR I/O - x8 PCI Express
RADAR & SDR I/O - 3U VPX - FORMAT 1
RADAR & SDR I/O - AMC
RADAR & SDR I/O - 3U VPX - FORMAT 2
RADAR & SDR I/O - FMC

Last updated: March 2018

New!

Models 57620 and 58620

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

Model 58620

General Information

Models 57620 and 58620 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71620 XMC modules mounted on a VPX carrier board.

Model 57620 is a 6U board with one Model 71620 module while the Model 58620 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

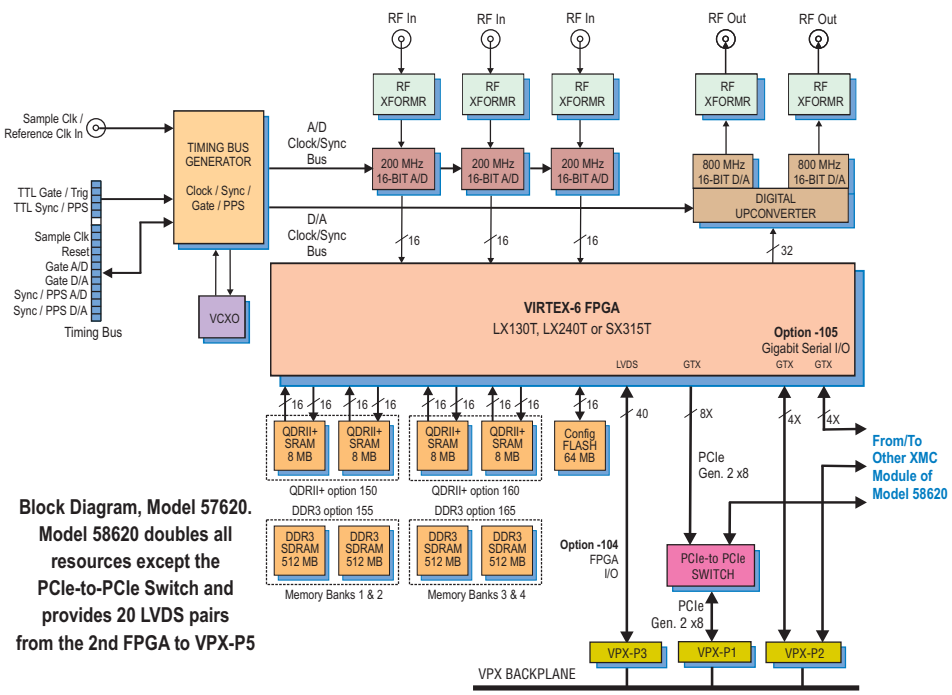
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57620; P3 and P5, Model 58620.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57620; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58620. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz 16-bit D/As
- 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57620. Model 58620 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57620 and 58620

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

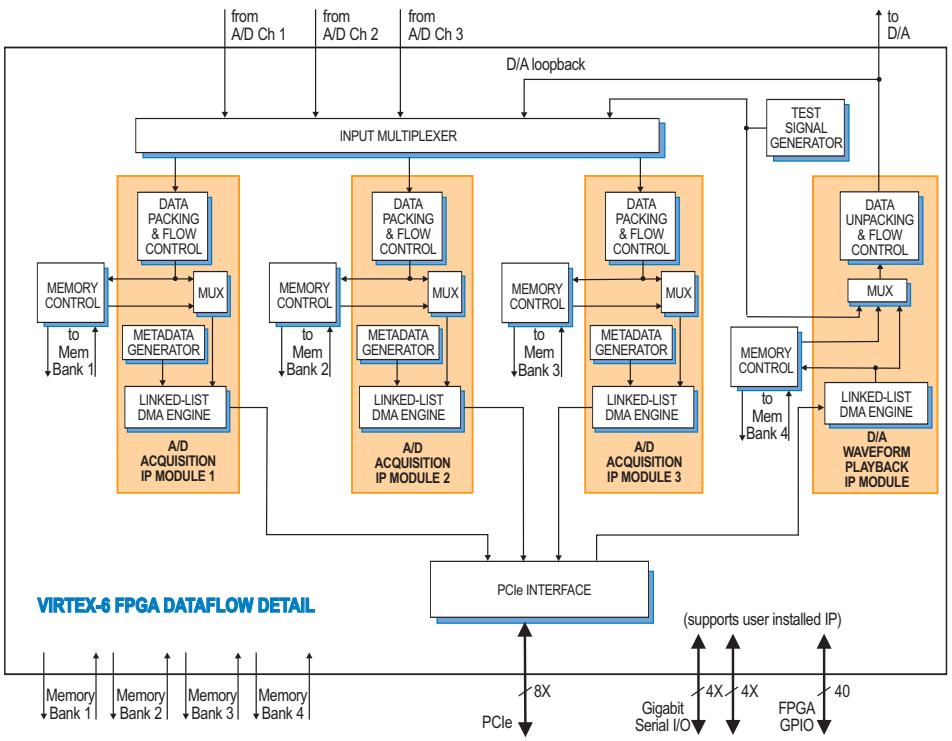
Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57620 and 58620

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57620	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 6U VPX
58620	6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A with two Virtex-6 FPGAs - 6U VPX

Options:

-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57620; P3 and P5 connectors, Model 58620
-105	Gigabit link between the FPGA and P2 connector, Model 57620; gigabit links from each FPGA to P2 connector, Model 78620
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57620: 3 A/Ds, 1 DUC, 2 D/As
Model 58620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57620; P3 and P5, Model 58620
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57620; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58620

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Models 57621 & 58621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

Model 58621

Cobalt
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (Digital Downconverters)
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz 16-bit D/As
- One or two multiboard programmable beamformers
- 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57621 and 58621 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71621 XMC modules mounted on a VPX carrier board.

Model 57621 is a 6U board with one Model 71621 module while the Model 58621 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, three or six multiband DDCs, one ot two DUCs, two or four D/As and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, one or two programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

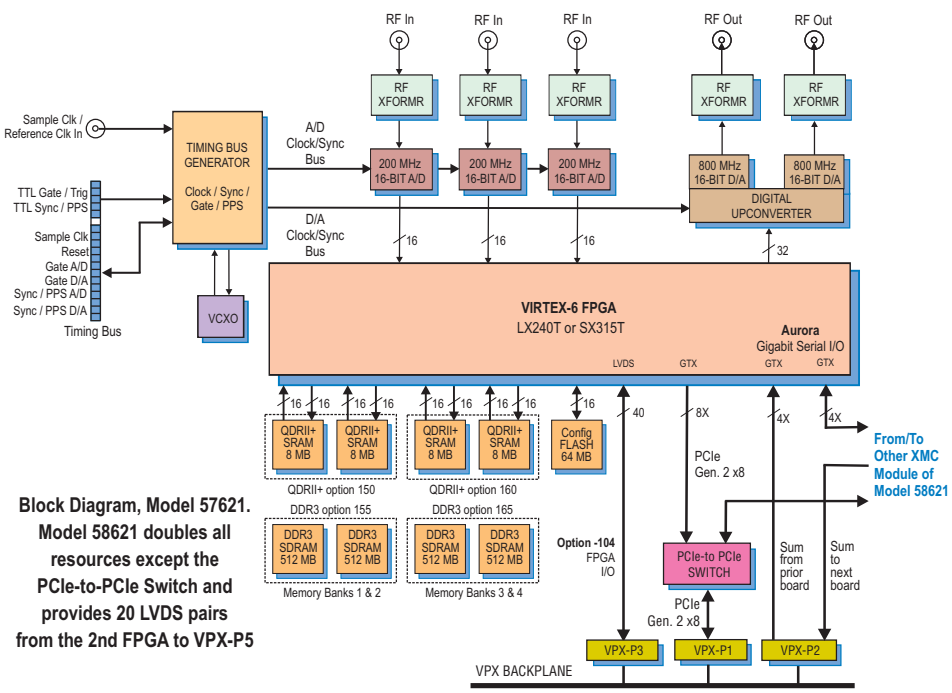
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57621; P3 and P5, Model 58621. ➤



Block Diagram, Model 57621. Model 58621 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57621 & 58621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

➤ A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

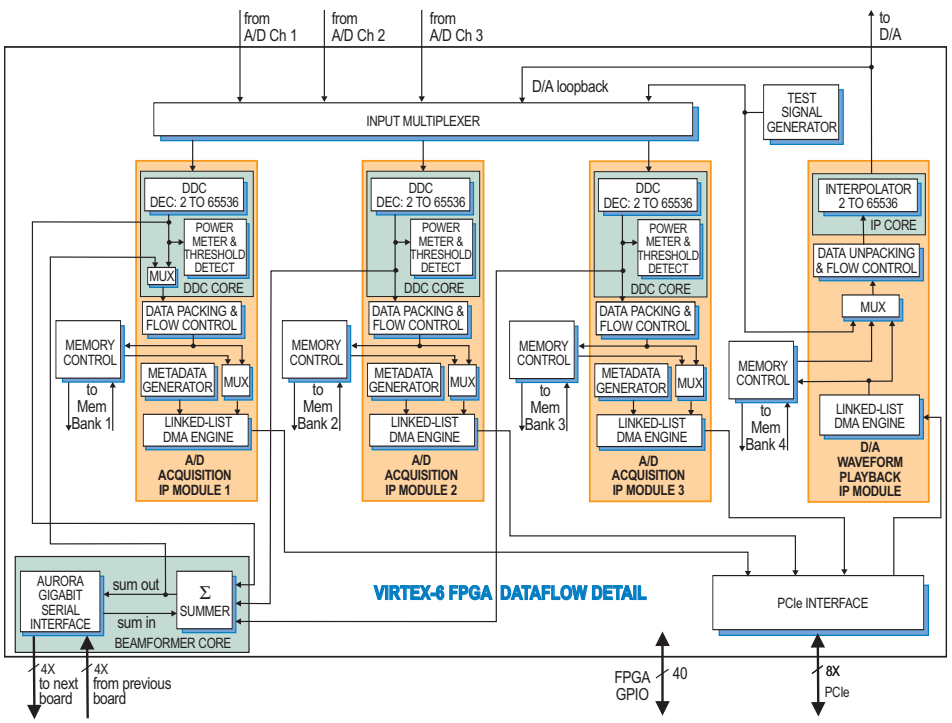
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via the built-in Xilinx Aurora gigabit serial interfaces through the VPX P2 connectors. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions include sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off- board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57621 & 58621

3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U VPX
58621	6-Channel 200 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U VPX
Options:	
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57621; P3 and P5 connectors, Model 58621
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57621: 3 A/Ds, 3 DDCs, 1 DUC, 2 D/As

Model 58621: 6 A/Ds, 6 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (3 or 6)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via VPX P2 connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57621; P3 and P5, Model 58621

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57800 & 58800

Kintex UltraScale FPGA Coprocessor- 6U VPX

Model 58800

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex Ultra-Scale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57800 and 58800 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a VPX carrier board. Model 57800 is a 6U board with one Model 71800 module while the Model 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57800 and Model 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

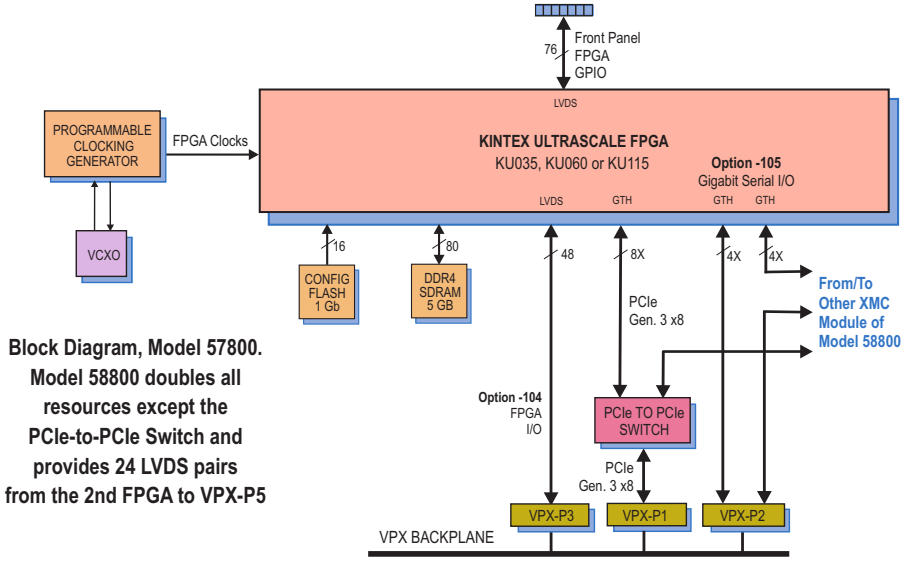
Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols. ➤



Block Diagram, Model 57800. Model 58800 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57800 & 58800

Kintex UltraScale FPGA Coprocessor- 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57800	Kintex UltraScale FPGA Coprocessor - 6U VPX
58800	Double Kintex UltraScale FPGA Coprocessors - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Front-Panel Digital I/O Interface

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Specifications

Front Panel Digital I/O (1 or 2)
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 or 76 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800
- **Option -105** provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

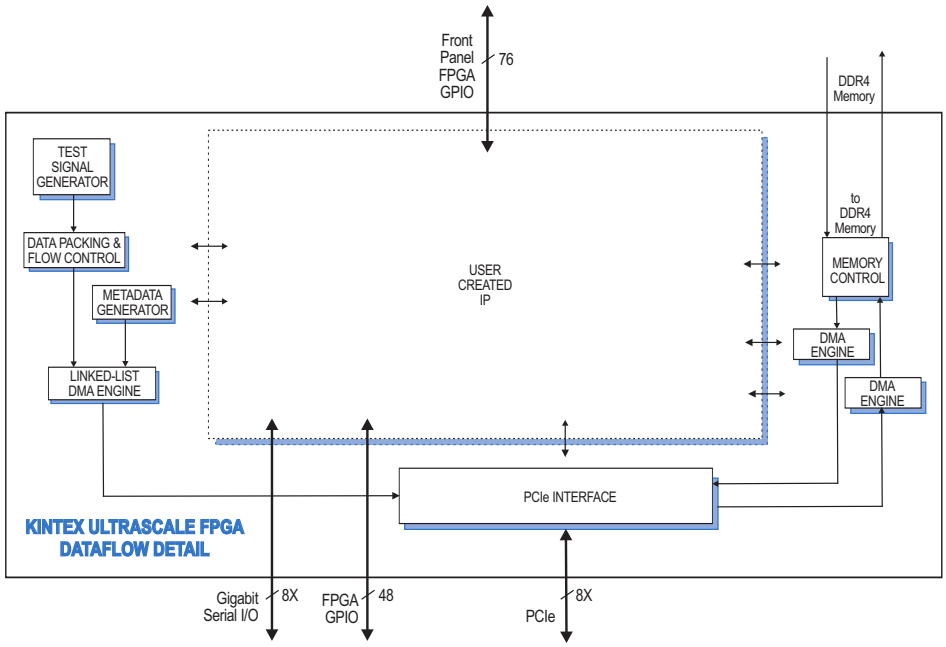
Option -702: L2 (air cooled)
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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New!

Models 57624 and 58624

2-or 4-Channel, 34- or 68-Signal Adaptive IF Relay - 6U VPX

Model 58624

Features

- Modifies 34 or 68 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two/four 200 MHz 16-bit A/Ds
- Two/four 800 MHz 16-bit D/As
- 34/68 DDCs and 34/68 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8,

General Information

Models 57624 and 58624 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71624 XMC modules mounted on a VPX carrier board. Model 57624 is a 6U board with one Model 71624 module while the Model 58624 is a 6U board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board

These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

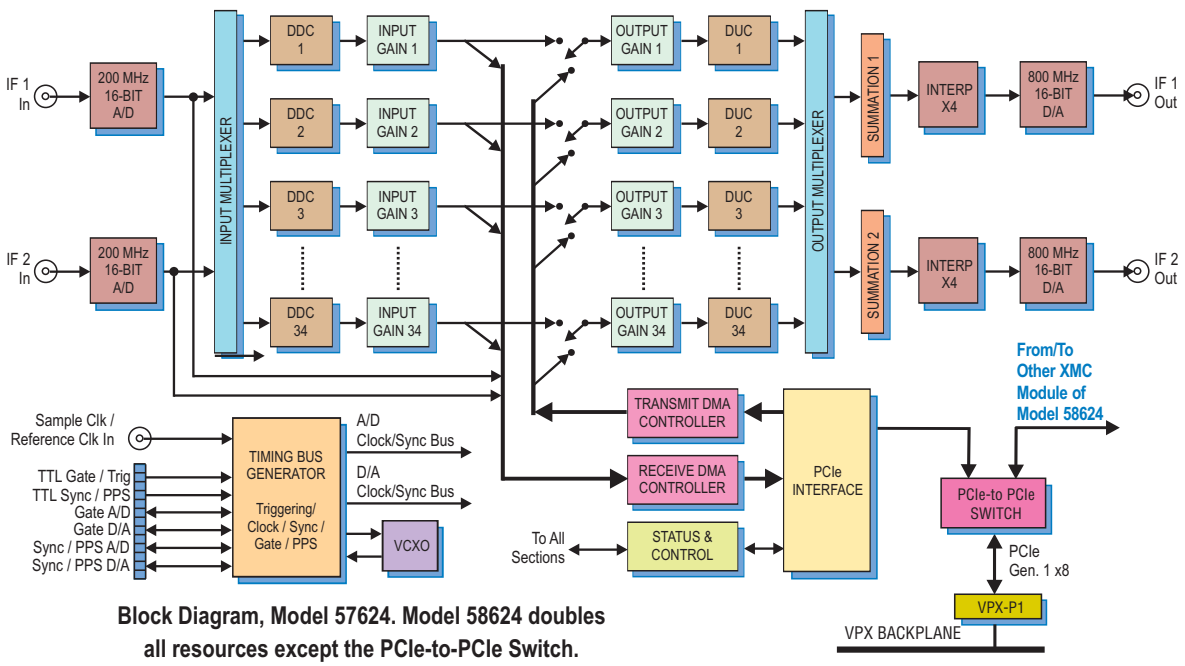
These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The output stage of these models consists of 34 or 68 DUCs (digital upconverters) and two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q ➤



Block Diagram, Model 57624. Model 58624 doubles all resources except the PCIe-to-PCIe Switch.

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➤ signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the adaptive relay of these models. Because of the complexity and proprietary nature of these functions, the FPGAs cannot be extended or modified by the user.

A/D Converters

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 or 68 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controllers

Two or four output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs of the first XMC module. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of Model 58624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begin filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controllers

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB. ➤

➤ Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts the summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

Clocking and Synchronization

Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from one or two on-board programmable VCXOs (voltage-controlled crystal oscillators). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

Models 57624 and 58624

2-or 4-Channel, 34- or 68-Signal Adaptive IF Relay - 6U VPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57624	Dual-Channel 34-Signal Adaptive IF Relay - 6U VPX
58624	Quad-Channel 68-Signal Adaptive IF Relay - 6U VPX
Options:	
-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As

Model 58624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2 or 4
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34 or 68
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/–48 dB

Digital Upconverters
- **Quantity:** 34 or 68
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2 or 4
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
- On-board clock synthesizers generate two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Required:** Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8;

Environmental
- **Standard:**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 702 L2 Extended Temp (air-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 712 L2 Extended Temp (conduction-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U VPX board, 233 x 160 mm (9.173 x 6.299 in.) ➤

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New!

Models 57630 & 58630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

Model 58630

General Information

Models 57630 and 58630 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a VPX carrier board.

Model 57630 is a 6U board with one Model 71630 module while the Model 58630 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

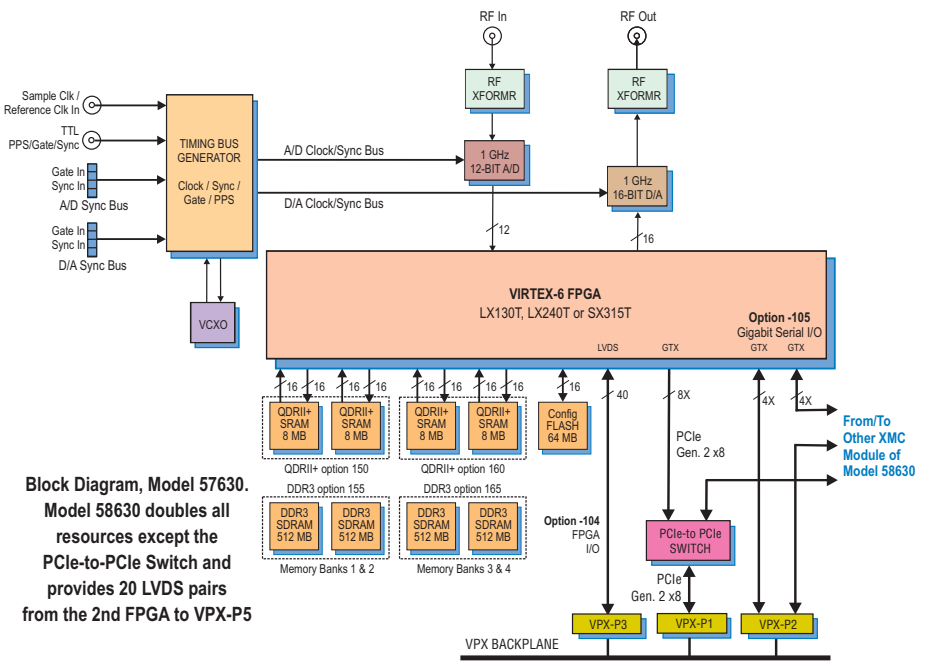
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57630. Model 58630 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57630 & 58630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to acept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

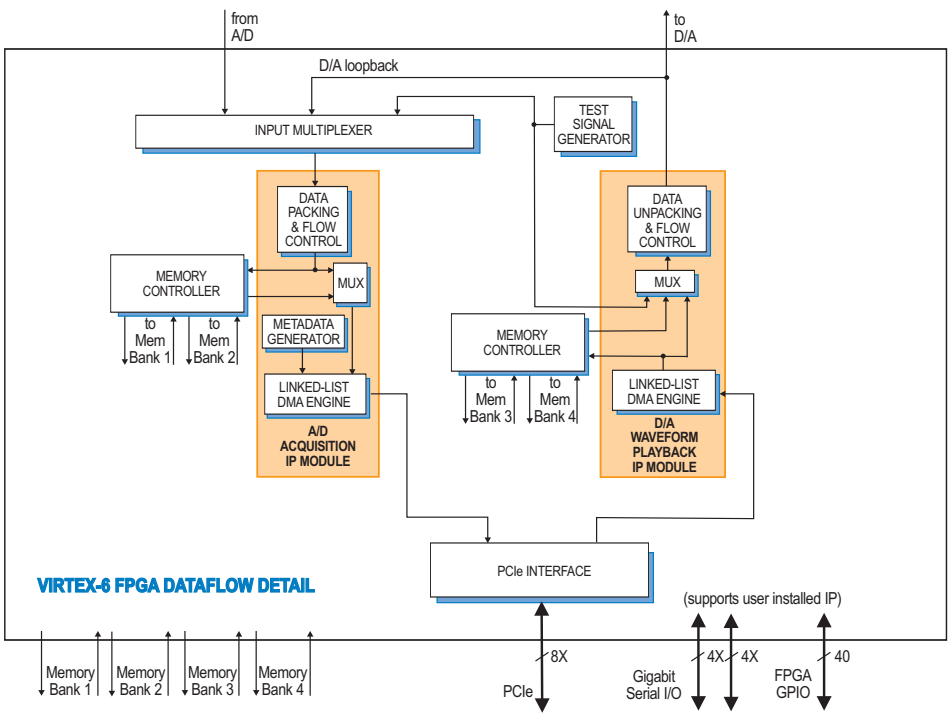
A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



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Models 57630 & 58630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57630	1 GHz A/D and D/A with Virtex-6 FPGA - 6U VPX
58630	Two 1 GHz A/D and D/A, with two Virtex-6 FPGAs - 6U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57630; P3 and P5 connectors, Model 58630
-105	Gigabit link between the FPGA and P2 connector, Model 57630; gigabit links from each FPGA to P2 connector, Model 78630
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57630: 1 A/D, 1 D/A
Model 58630: 2 A/Ds, 2 D/As
Front Panel Analog Signal Inputs (1 or 2)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converters (1 or 2)
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs (1 or 2)
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus (1 or 2): 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630
Memory Banks (1 or 2)
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57640 & 58640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX

Model 58640

General Information

Models 57640 and 58640 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a VPX carrier board.

Model 57640 is a 6U board with one Model 71640 module while the Model 58640 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

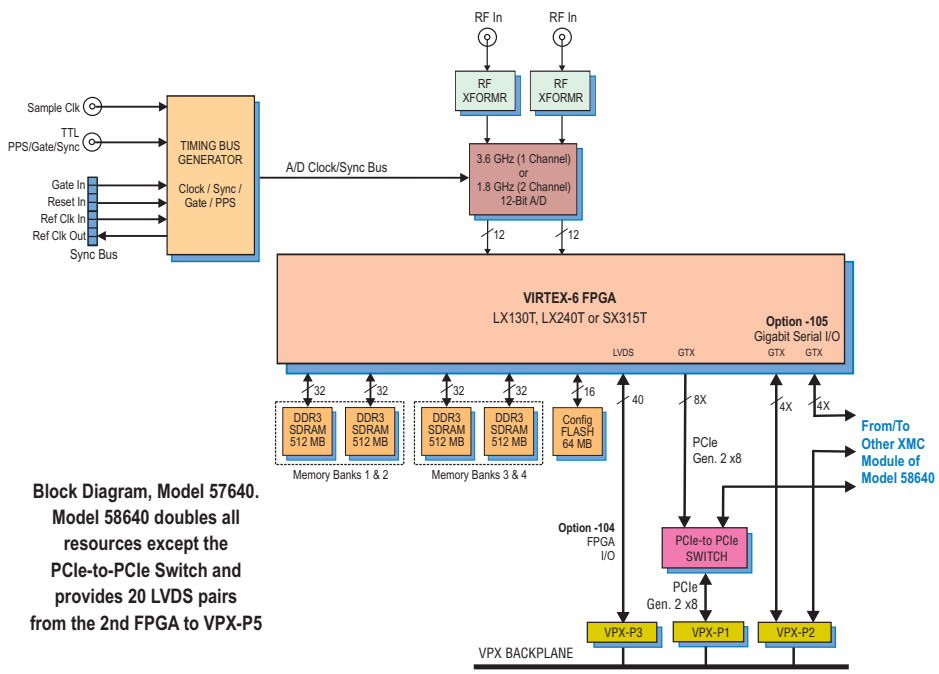
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57640; P3 and P5, Model 58640.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57640; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58640. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57640. Model 58640 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57640 & 58640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

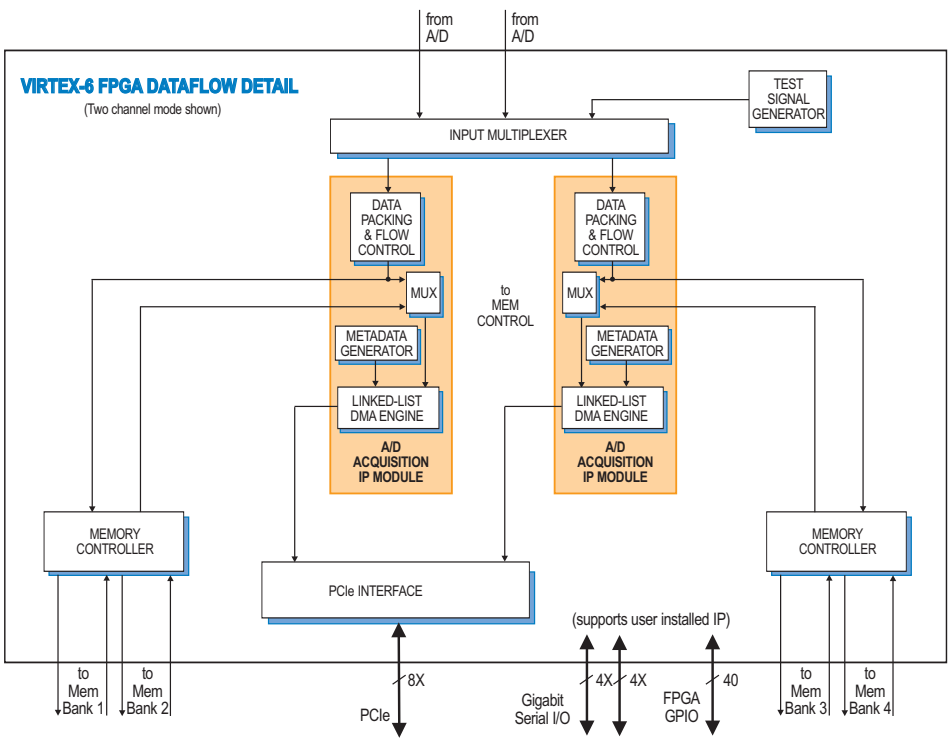
A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Models 57640 & 58640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U VPX
58640	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D with two Virtex-6 FPGAs - 6U VPX
Options:	
-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57640; P3 and P5 connectors, Model 58640
-105	Gigabit link between the FPGA and P2 connector, Model 57640; gigabit links from each FPGA to P2 connector, Model 78640
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57640: One A/D
Model 58640: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Sample Clock Sources (1 or 2)
Front panel SSMC connector
Sync Bus (1 or 2)
Multi-pin connectors, bus includes gate, reset and in and out ref clock
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57640; P3 and P5, Model 58640
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57640; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58640
Memory Banks (1 or 2)
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57641 & 58641

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX

Model 58641

General Information

Models 57641 and 58641 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71641 XMC modules mounted on a VPX carrier board.

Model 57641 is a 6U board with one Model 71641 module while the Model 58641 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, one- or two-channel programmable digital downconverters, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641.

A/D Converter Stage

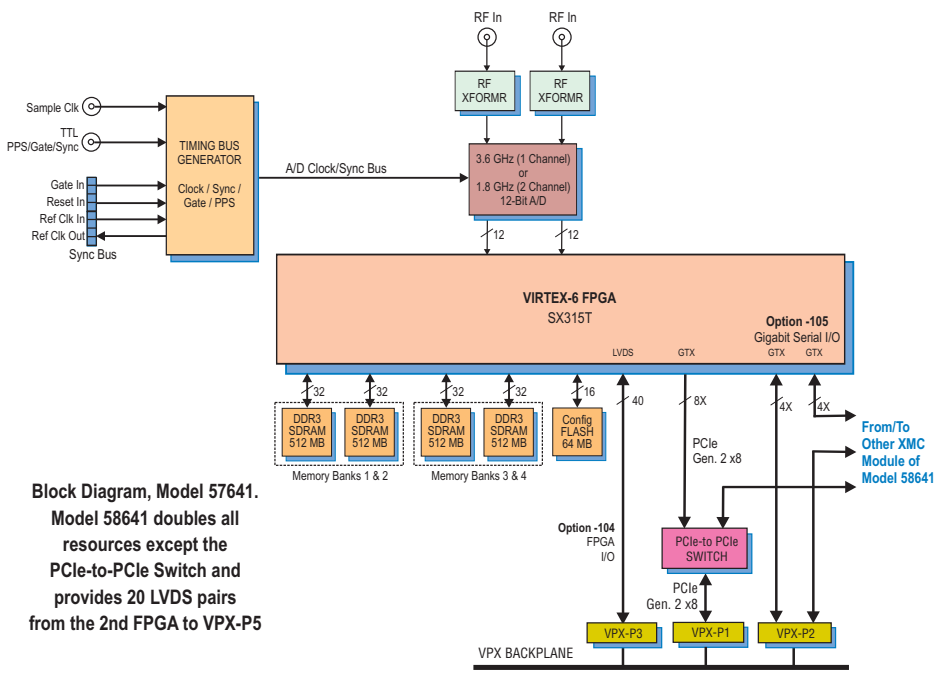
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources. ➤

Features

- Ideal radar and software radio interface solution
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57641. Model 58641 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57641 & 58641

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

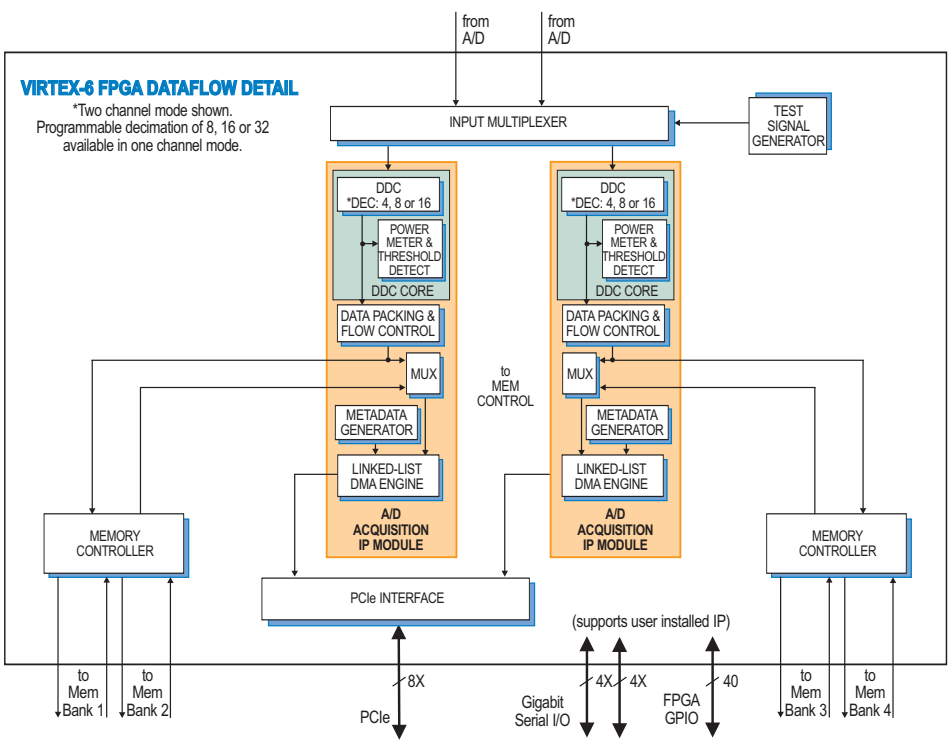
Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Models 57641 & 58641

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U VPX
58641	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
-105	Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57641: One A/D
Model 58641: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Sources (1 or 2)
Front panel SSMC connector
Sync Bus (1 or 2)
Multi-pin connectors, bus includes gate, reset and in and out ref clock
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641
Memory Banks (1 or 2)
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57650 & 58650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

Model 58650

Cobalt
ReadyFlow Board Support Package
GateFlow

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57650 and 58650 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71650 XMC modules mounted on a VPX carrier board.

Model 57650 is a 6U board with one Model 71650 module while the Model 58650 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these modles include two or four A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

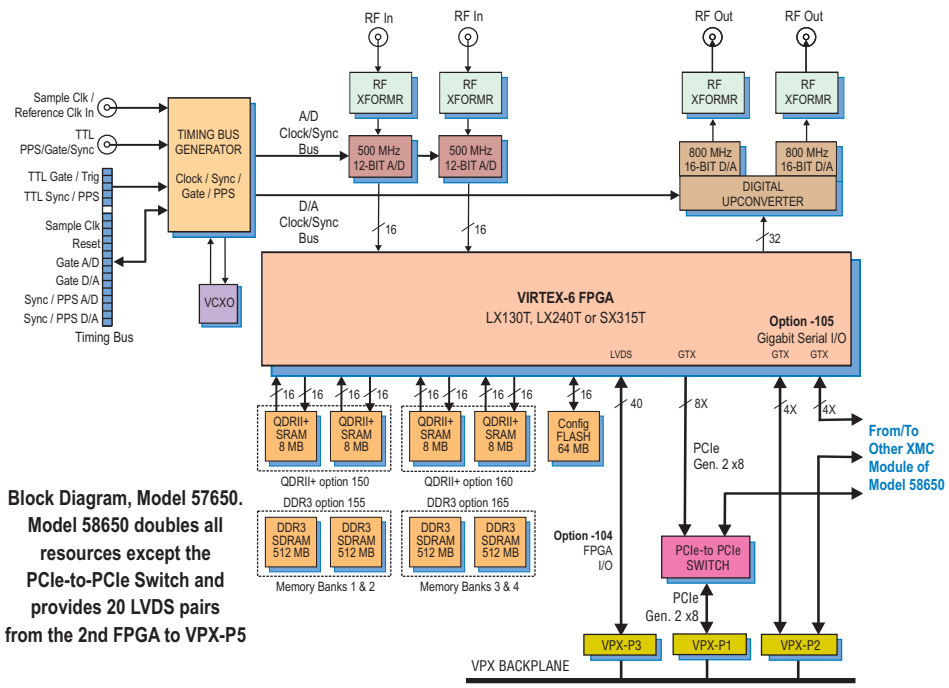
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57650; P3 and P5, Model 58650.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57650; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58650. ➤



Block Diagram, Model 57650. Model 58650 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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www.pentek.com

Models 57650 & 58650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back waveforms stored in either on-board memory or off- board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stages

The front end accepts two or four full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs and D/As accept baseband real or complex data streams from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

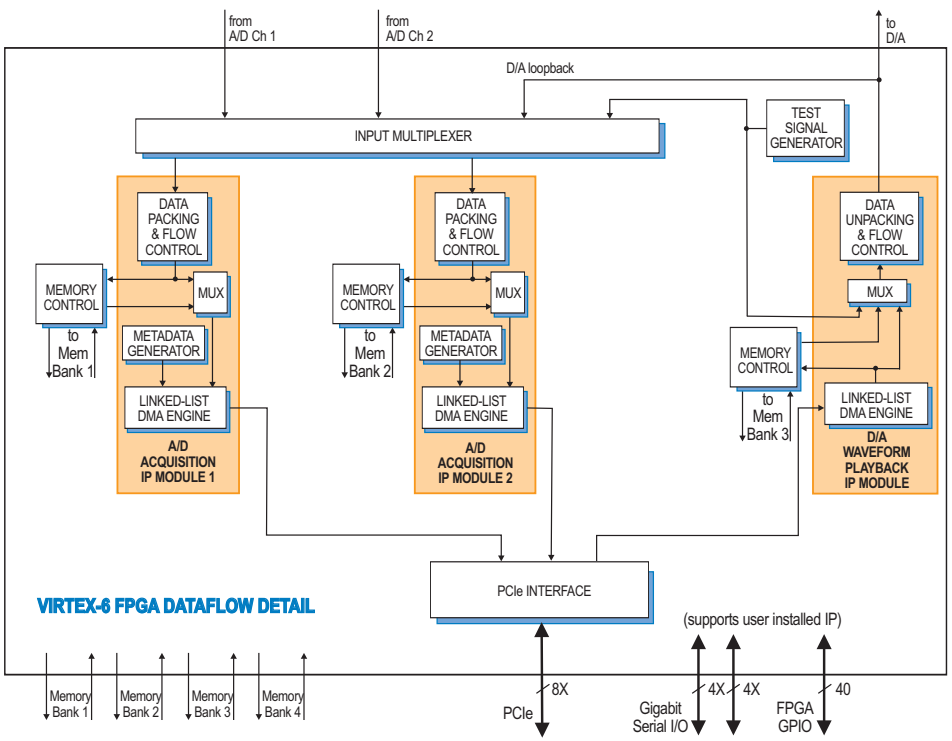
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



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Models 57650 & 58650

2- or 4-Channel 500 MHz A/D, DUC with 2-or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57650	Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 6U VPX
58650	Four 500 MHz A/Ds, Two DUCs, Four 800 MHz D/As with two Virtex-6 FPGAs - 6U VPX

Options:

-002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57650; P3 and P5 connectors, Model 58650
-105	Gigabit link between the FPGA and P2 connector, Model 57650; gigabit links from each FPGA to P2 connector, Model 78650
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57650: 2 A/Ds, 1 DUC, 2 D/As
Model 58650: 4 A/Ds, 2 DUCs, 4 D/As
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits
A/D Converters (option - 014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits
Front Panel Analog Signal Outputs (2 or 4)
Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57650; P3 and P5, Model 58650
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57650; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58650
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Model 57651 & 58651

2 or 4-Channel 500 MHz A/D with DDCs, DUCs with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

Model 58651

Cobalt

GateFlow

ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or 16 or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57651 and 58651 are members of the Cobalt® family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a VPX carrier board.

Model 57651 is a 6U board with one Model 71651 module while the Model 58651 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As, one or two beamformers and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beamforming IP cores, an Aurora and a PCIe interfaces complete the factory-installed functions and enable these models to operate without the need to develop any FPGA IP.

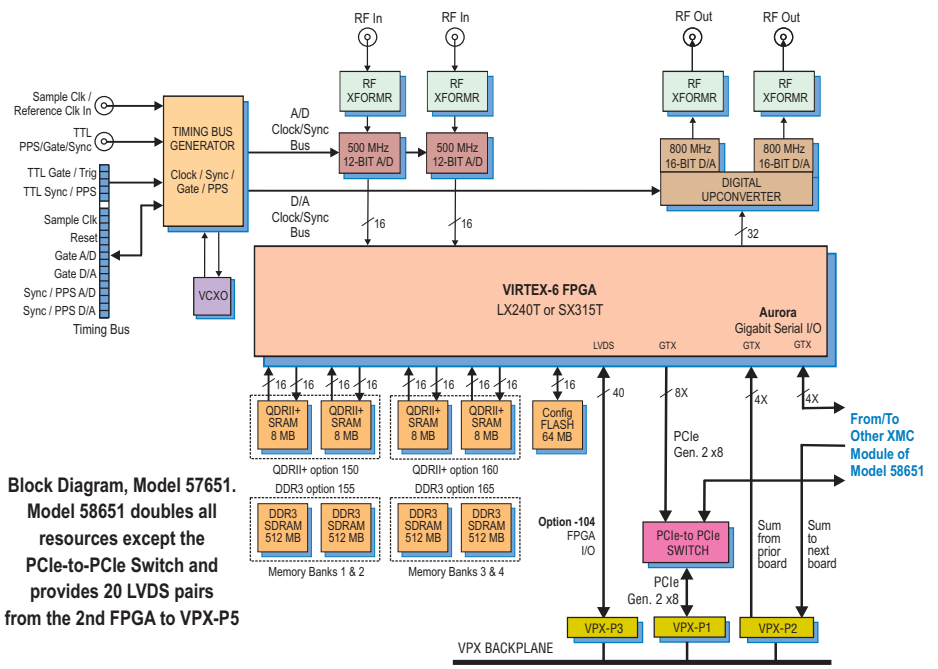
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57651; P3 and P5, Model 58651. ➤



Block Diagram, Model 57651. Model 58651 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Model 57651 & 58651

2 or 4-Channel 500 MHz A/D with DDCs, DUCs with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is program- mable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

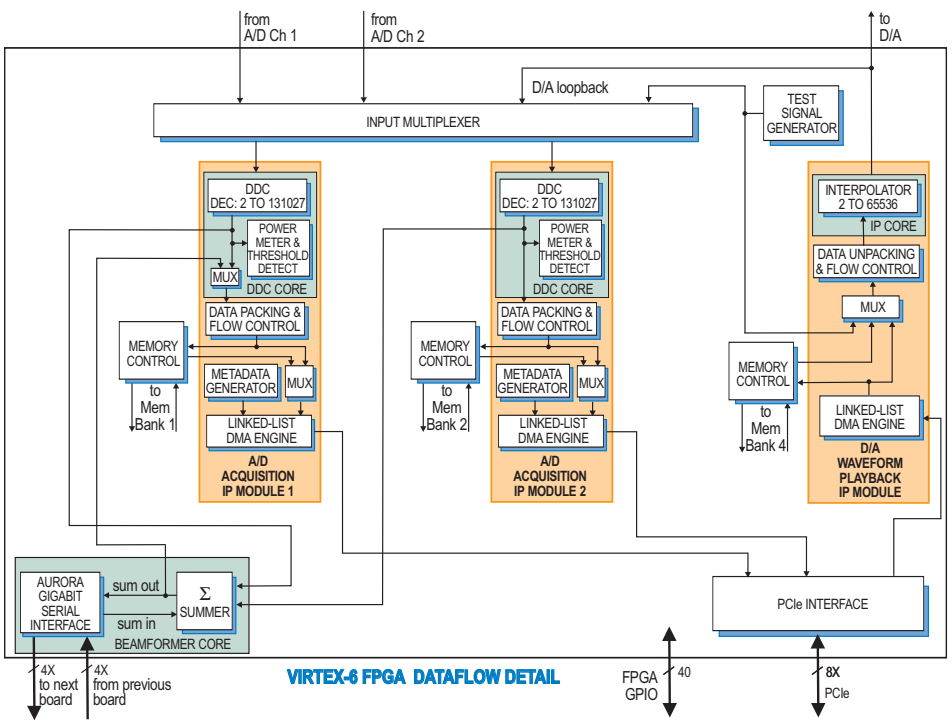
A programmable summation block provides summing of any of the DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple models can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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2 or 4-Channel 500 MHz A/D with DDCs, DUCs with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

➤ A/D Converter Stages

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to three or six independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Model 57651 & 58651

2 or 4-Channel 500 MHz A/D with DDCs, DUCs with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57651	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U VPX
58651	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U VPX

Options:

002*	-2 FPGA speed grade
-014	400 MHz, 14-bit A/Ds
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57651; P3 and P5 connectors, Model 58651
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57651: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

Model 58651: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (Option -014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters (2 or 4)
Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolators (1 or 2)
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via a dual 4X connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57651; P3 and P5, Model 58651

Memory (1 or 2)
Option -150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57660 & 58660

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U OpenVPX

Model 58660

General Information

Models 57660 and 58660 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a VPX carrier board.

Model 57660 is a 6U board with one Model 71660 module while the Model 58660 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

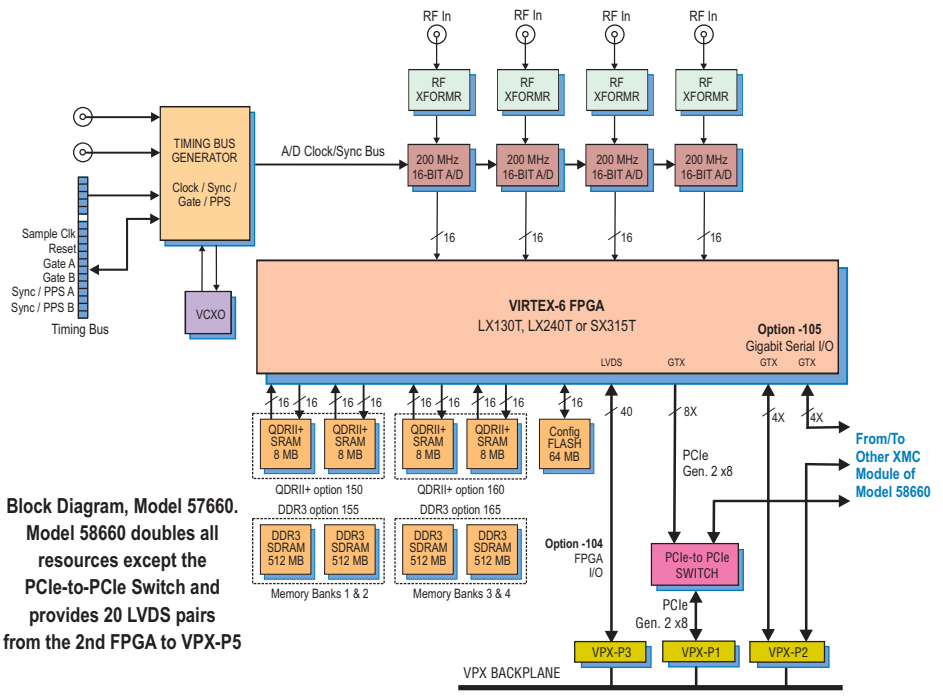
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57660. Model 58660 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U OpenVPX

A/D Converter Stages

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

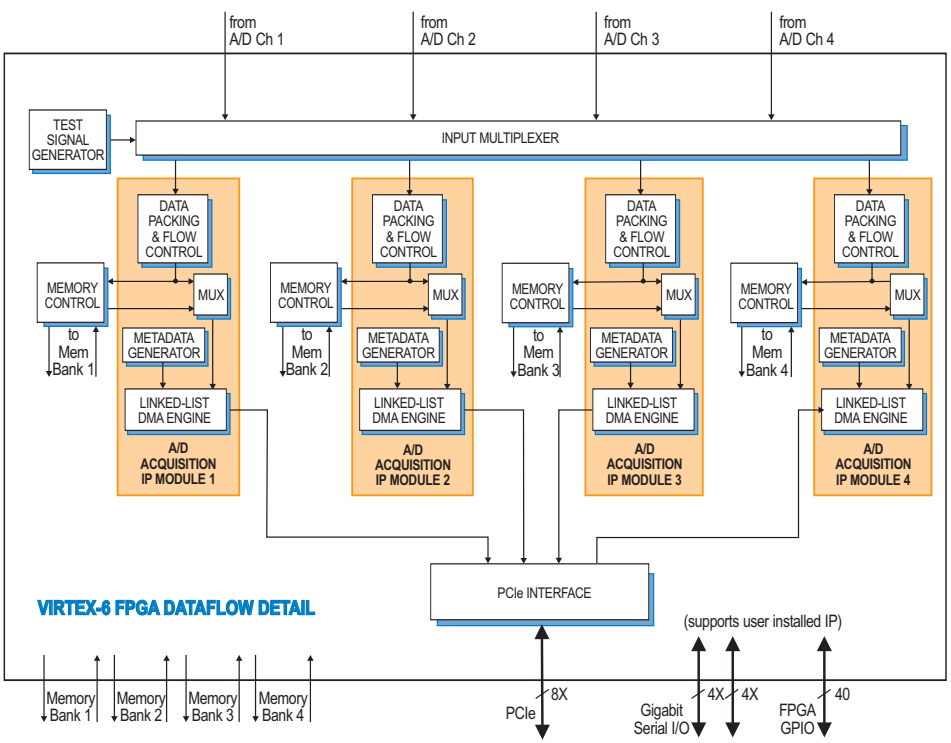
These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Models 57660 & 58660

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U VPX
58660	8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57660; P3 and P5 connectors, Model 58660
-105	Gigabit link between the FPGA and P2 connector, Model 57660; gigabit links from each FPGA to P2 connector, Model 58660
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57660: 4 A/Ds
Model 58660: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board clock synthesizers
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57661 & 58661

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U OpenVPX

Model 58661

General Information

Models 57661 and 58661 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71661 XMC modules mounted on a VPX carrier board.

Model 57661 is a 6U board with one Model 71661 module while the Model 58661 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, four or eight multiband DDCs, one or two programmable beamformers, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

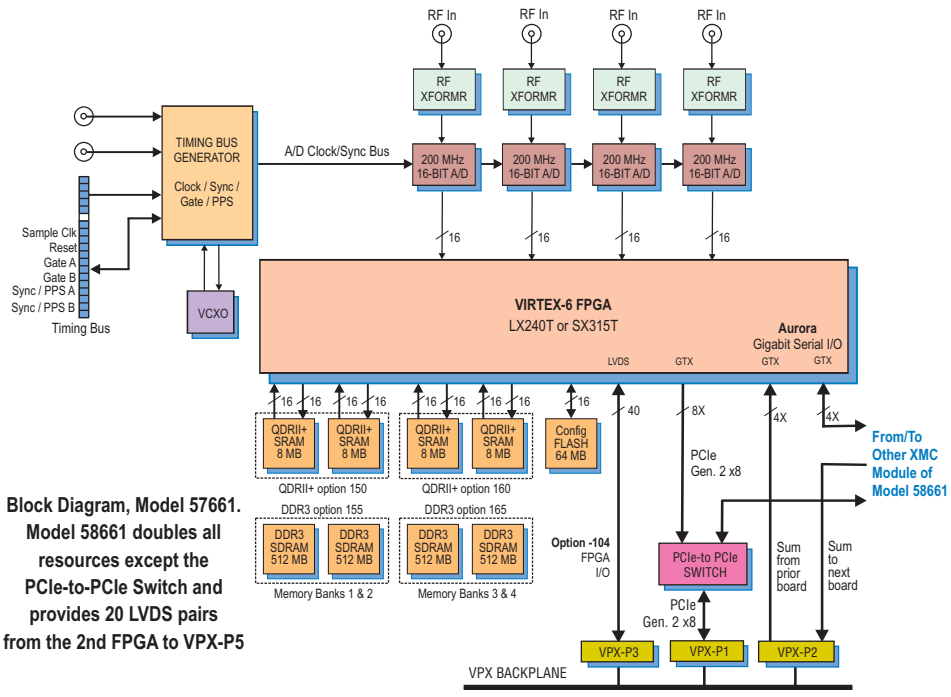
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57661; P3 and P5, Model 58661. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57661. Model 58661 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57661 & 58661

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

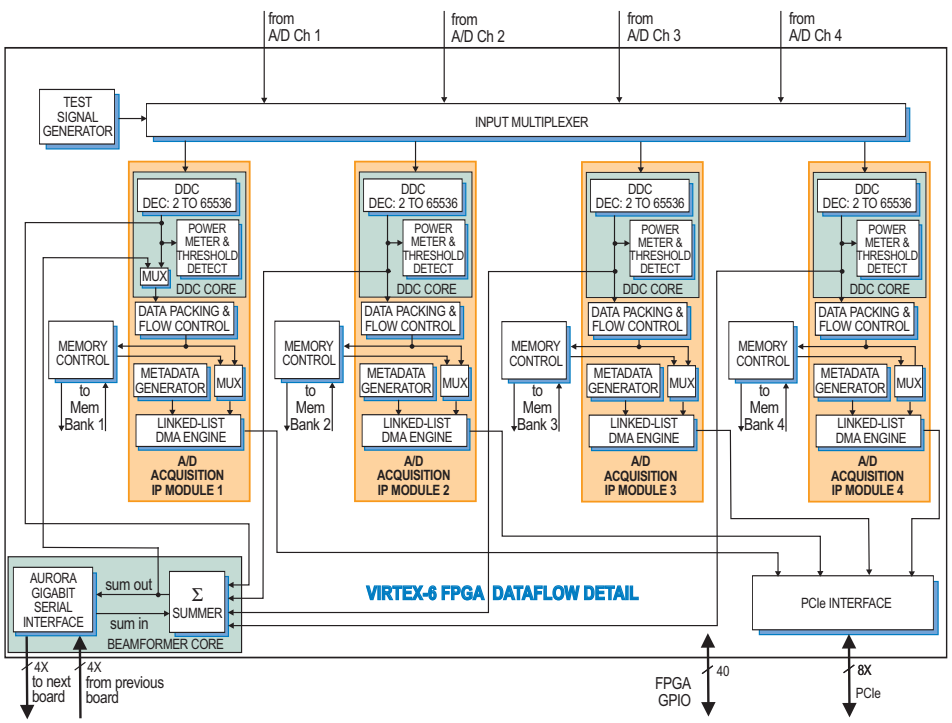
A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ➤



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Models 57661 & 58661

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U OpenVPX

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U VPX
58661	8-Channel 200 MHz A/D with DDCs and two Virtex-6 FPGAs - 6U VPX
Options:	
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57661; P3 and P5 connectors, Model 58661
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 57661: 4 A/Ds
Model 58660: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via VPX P2 connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources (1 or 2)
- On-board clock synthesizer

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57661; P3 and P5, Model 58661

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

Model 58662

General Information

Models 57662 and 58662 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a VPX carrier board.

Model 57662 is a 6U board with one Model 71662 module while the Model 58662 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, 32 or 64 multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, test signal generators, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

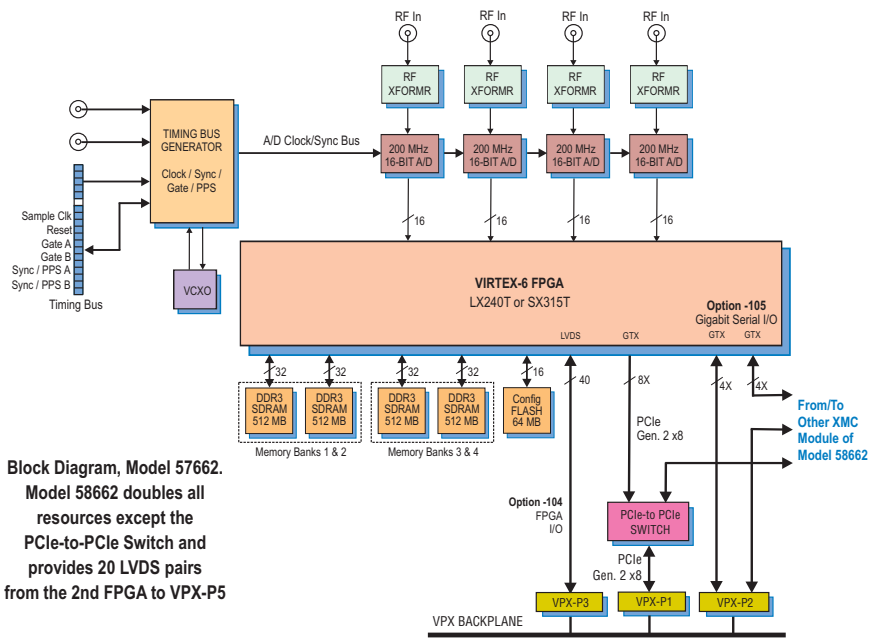
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- 32 or 64 channels of multiband DDCs (digital downconverters)
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57662. Model 58662 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

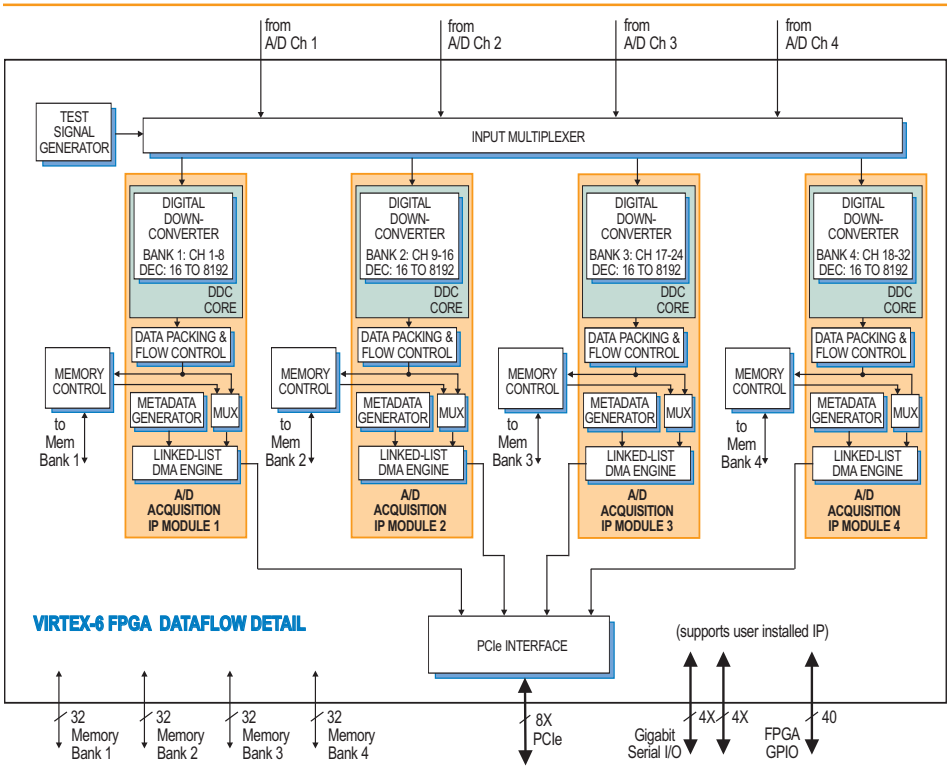
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with DDR3 SDRAM. ➤



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Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 6U VPX
58662	8-Ch 200 MHz A/D with 64-Ch DDC and two Virtex-6 FPGAs - 6U VPX
Options:	
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57662; P3 and P5 connectors, Model 58662
-105	Gigabit link between the FPGA and P2 connector, Model 57662; gigabit links from each FPGA to P2 connector, Model 58660
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57662: 4 A/Ds, 32 DDCs
Model 58660: 8 A/Ds, 64 DDCs
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (32 or 64)
Quantity: Four 8-channel banks, one per acquisition module
Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, >100 dB stopband attenuation
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662
MemoryBanks (1 or 2)
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57663 & 58663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - 6U OpenVPX

Model 58663

Features

- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- PCI Express (Gen. 1 & 2) interface up to x4
- LVPECL clock/sync bus for multiboard synchronization
- Ruggedized and conduction-cooled versions available

General Information

Models 57663 and 58663 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a VPX carrier board.

Model 57663 is a 6U board with one Model 71663 module while the Model 58663 is a 6U board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA develpment required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

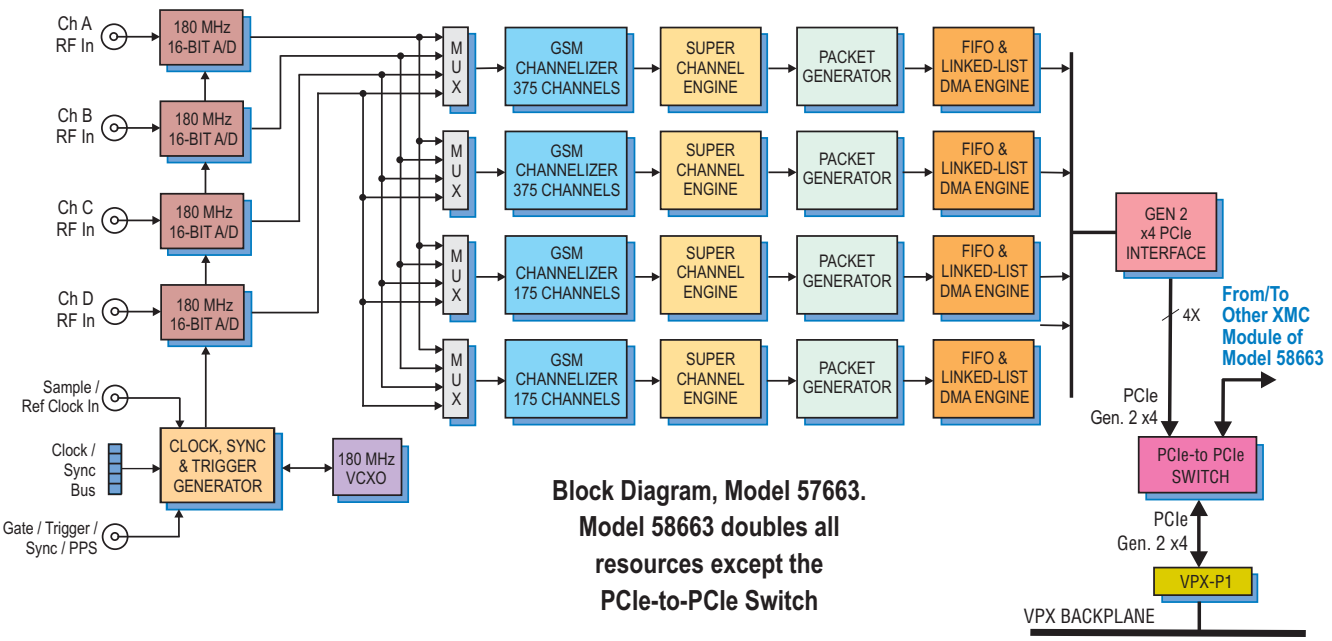
The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤



Block Diagram, Model 57663. Model 58663 doubles all resources except the PCIe-to-PCIe Switch

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - 6U OpenVPX

➤ GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digtitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single "superchannel". This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once compete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data "payload" samples can be identified and recovered by the host.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The PCIe interface is also used as the programming interface for all status and control between these models and host. ➤

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www.pentek.com

Models 57663 & 58663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Specifications

Model 57663: 4 A/Ds, 1100 Channels
Model 58663: 8 A/Ds, 2200 Channels
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
GSM Channel Banks (1 or 2)
DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz
DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 KHz
> 96 dB attenuation at > ±3 MHz
DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
DDC Data Output Format:
24 bits I + 24 bits Q
Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
Frequency Offsets for each DDC:
First: $-f_s/4$ (-270.8333 kHz)
Second: 0 Hz
Third: $+f_s/4$ (+270.8333 kHz)
Fourth: $+f_s/2$ (+541.666 kHz)
Superchannel Sample Rate: f_s
Superchannel Output Format:
26 bits I + 26 bits Q
Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94
Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
57663	1100-Channel GSM Channelizer with Quad A/D - 6U VPX
58663	2200-Channel GSM Channelizer with Octal A/D - 6U VPX

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

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New!

Models 57664 & 58664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U VPX

Model 58664

General Information

Models 57664 and 58664 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71664 XMC modules mounted on a VPX carrier board.

Model 57664 is a 6U board with one Model 71664 module while the Model 58664 is a 6U board with two XMC modules rather than one. Their PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

These models include four or eight A/Ds, four or eight multiband DDCs, one or two programmable beamformers, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

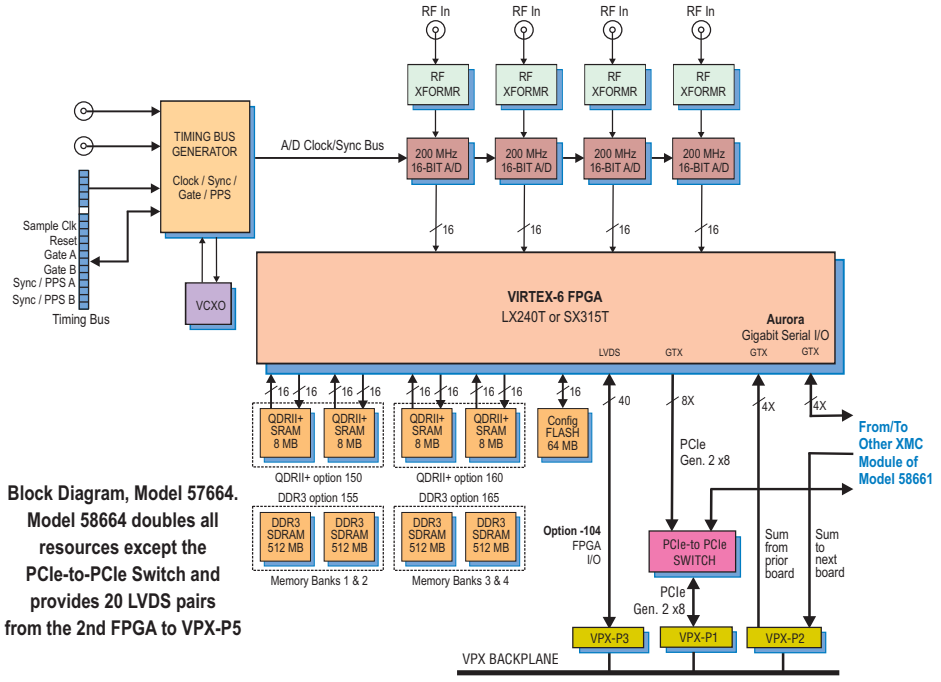
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57664; P3 and P5, Model 58664. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57664. Model 58664 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57664 & 58664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U VPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

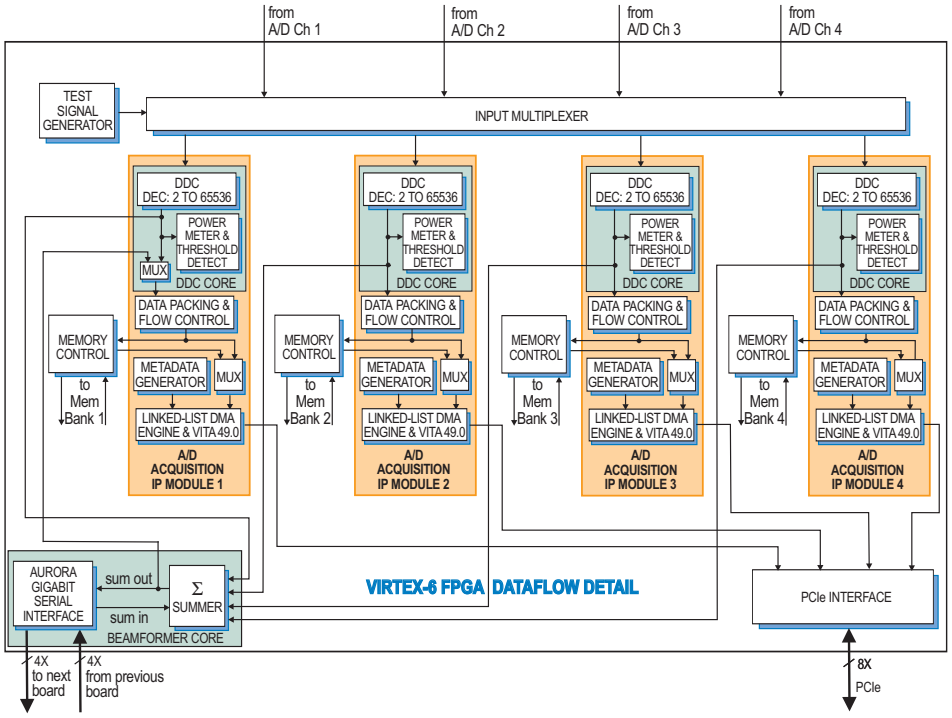
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

These models support fully the VITA 49.0 specification. ➤



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4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U VPX

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Models 57664 & 58664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U VPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57664	4-Channel 200 MHz A/D with DDCs, VITA 49.0, one Virtex-6 FPGA - 6U VPX
58664	8-Channel 200 MHz A/D with DDCs, VITA 49.0, two Virtex-6 FPGAs - 6U VPX
Options:	
-064	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57664; P3 and P5 connectors, Model 58664
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57664: 4 A/Ds
Model 58664: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (4 or 8)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Beamformers (1 or 2)
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via VPX P2 connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit
Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57664; P3 and P5, Model 58664
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57670 & 58670

4- or 8-Channel 1.25 GHz D/A with DUC and Virtex-6 FPGA - 6U OpenVPX

Model 58670

Cobalt
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57670 and 58670 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a VPX carrier board.

Model 57670 is a 6U board with one Model 71670 module while the Model 58670 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eightD/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

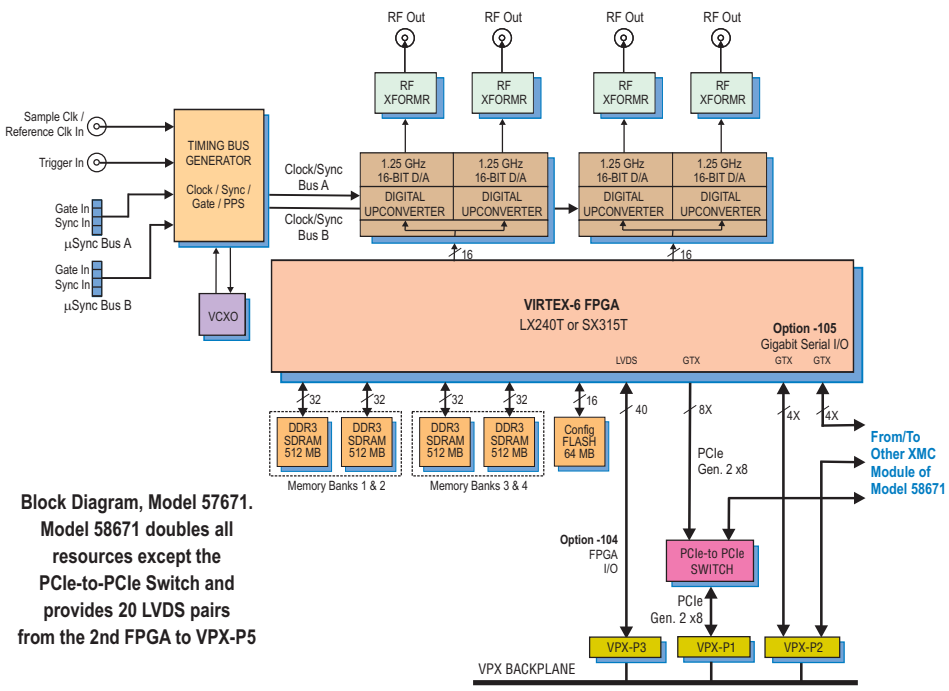
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57670; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58670. ➤



Block Diagram, Model 57671. Model 58671 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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4- or 8-Channel 1.25 GHz D/A with DUC and Virtex-6 FPGA - 6U OpenVPX

➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four or eight front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

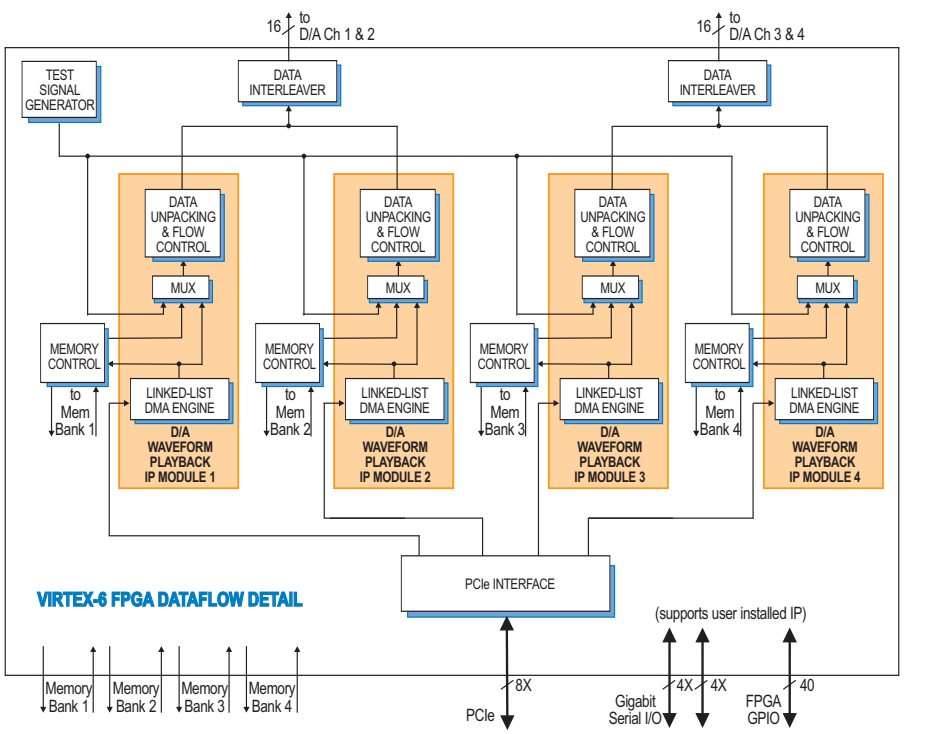
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 58670.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Models 57670 & 58670

4- or 8-Channel 1.25 GHz D/A with DUC and Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U VPX
58670	8-Channel 1.25 GHz D/A with two Virtex-6 FPGAs - 6U VPX

Options:

-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57670; P3 and P5 connectors, Model 58670
-105	Gigabit link between the FPGA and P2 connector, Model 57670; gigabit links from each FPGA to P2 connector, Model 58670
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57670: 4-Channel DUC, 4-channel D/A

Model 58670: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or8)
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (4 or 8)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57670; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58670

Memory Banks (1 or 2)
Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57671 & 58671

4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

Model 58671

General Information

Models 57671 and 58671 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71671 XMC modules mounted on a VPX carrier board.

Model 57671 is a 6U board with one Model 71671 module while the Model 58671 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

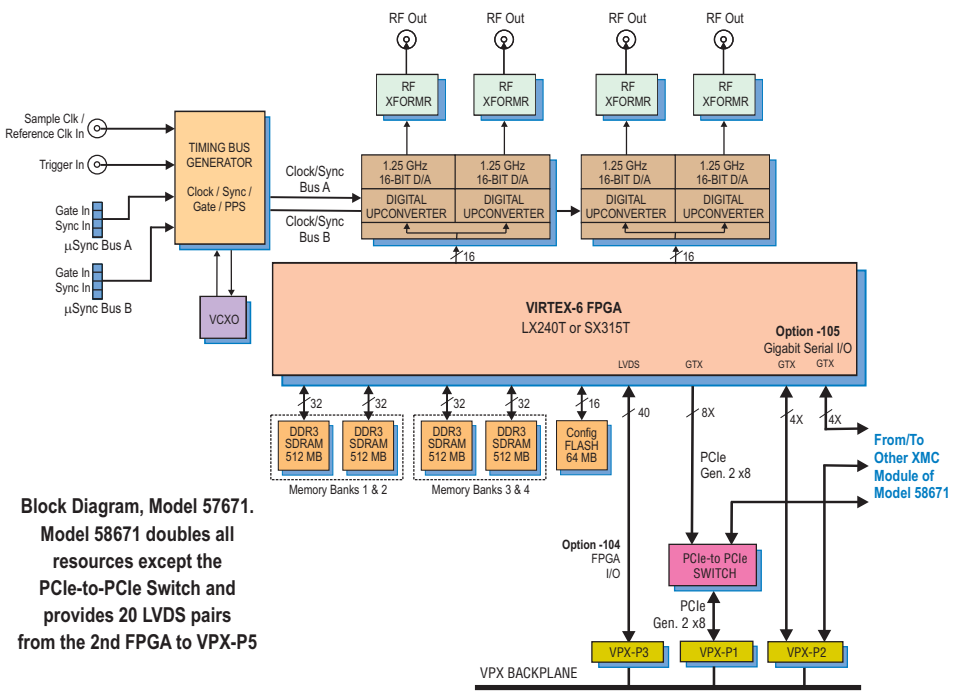
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57671. Model 58671 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUCs (digital upconverters) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGAs and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, these models feature an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog outputs are through front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤

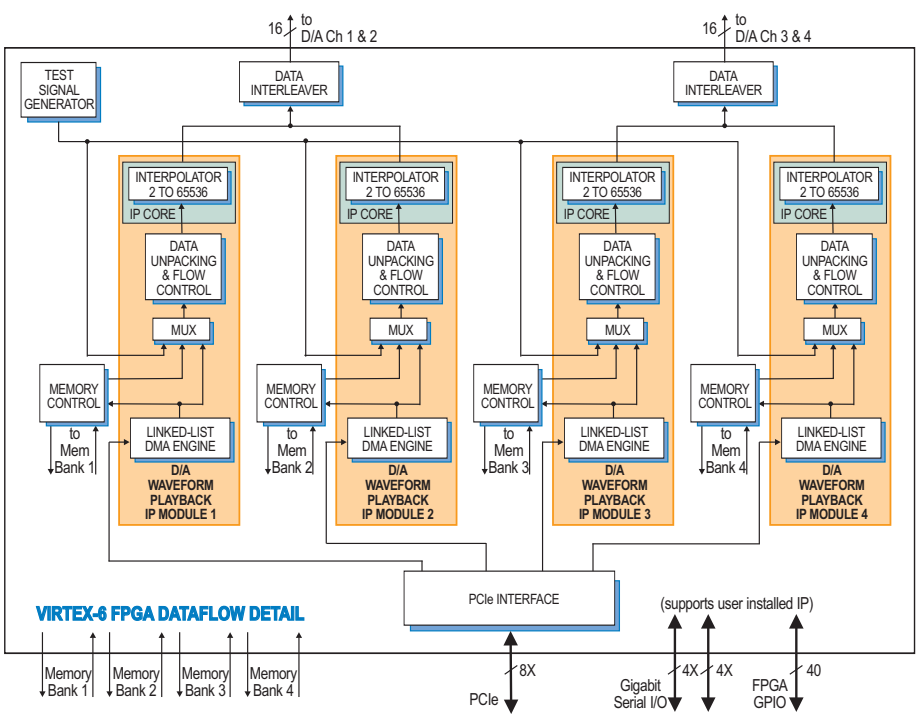
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked-list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 58671.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Models 57671 & 58671

4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U VPX
58671	8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and two Virtex-6 FPGAs - 6U VPX
Options:	
-002*	-2 FPGA speed grade
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57671; P3 and P5 connectors, Model 58671
-105	Gigabit link between the FPGA and P2 connector, Model 57671; gigabit links from each FPGA to P2 connector, Model 58671
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57671: 4-Channel DUC, 4-channel D/A

Model 58671: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or8)
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (4 or 8)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex- 6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671

Memory Banks (1 or 2)
Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

Model 58690

Cobalt
GateFlow
ReadyFlow Board Support Package

Features

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57690 and 58690 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a VPX carrier board.

Model 57690 is a 6U board with one Model 71690 module while the Model 58690 is a 6U board with two XMC modules rather than one.

These models include one ot two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

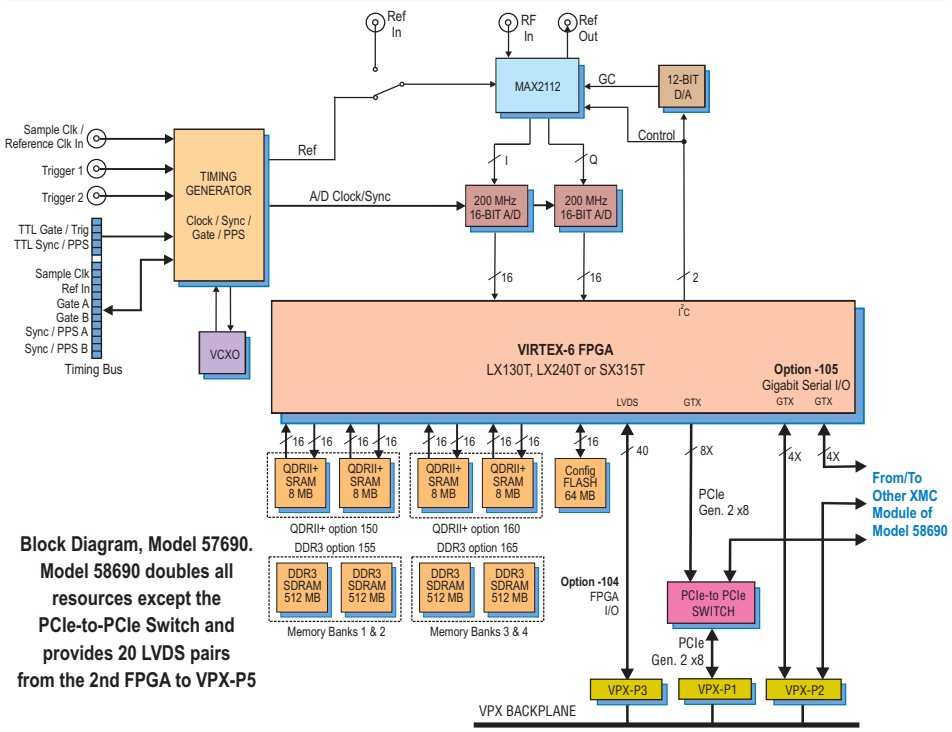
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690. ➤



Block Diagram, Model 57690. Model 58690 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

➤ RF Tuner Stages

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LNBs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNAs offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stages

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the bosrd. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave bosrds, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

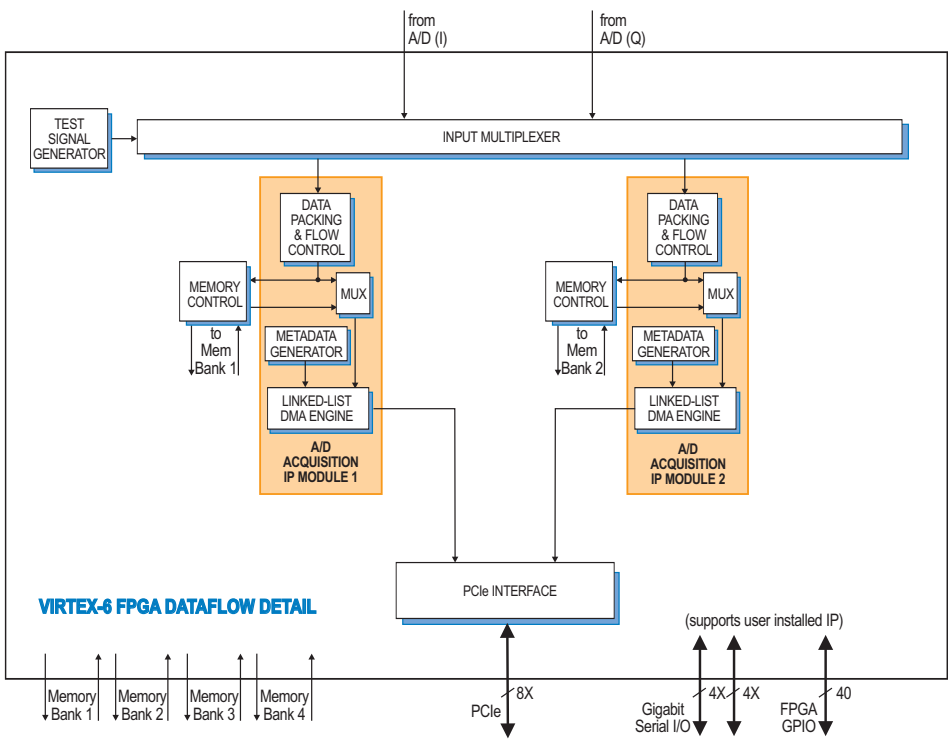
The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57690 & 58690

One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX
58690	Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57690; P3 and P5 connectors, Model 58690
-105	Gigabit link between the FPGA and P2 connector, Model 57690; gigabit links from each FPGA to P2 connector, Model 58690
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57690: One RF tuner, two A/Ds
Model 58690: Two RF tuners, four A/Ds
Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuners (1 or 2)
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters (2 or 4)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer
A/D Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Inputs (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (2 or 4)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57720 & 58720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U Open VPX

Model 58720

General Information

Models 57720and 58720 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71720 XMC modules mounted on a VPX carrier board.

Model 57720 is a 6U board with one Model 71720 module while the Model 58720 is a 6U board with two XMC modules rather than one.

These models include three or sixA/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

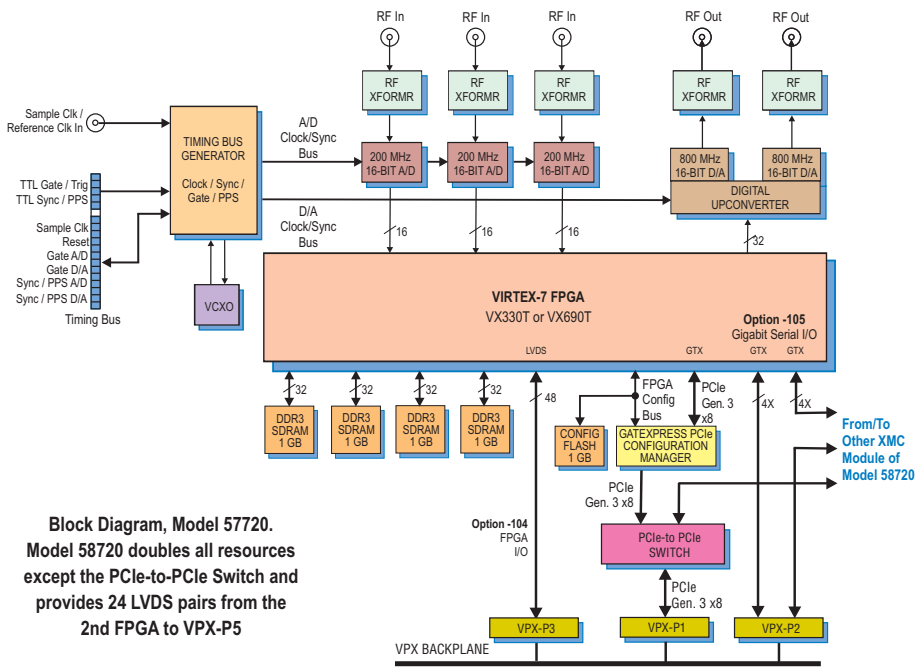
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz 16-bit D/As
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57720. Model 58720 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57720 & 58720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U Open VPX

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

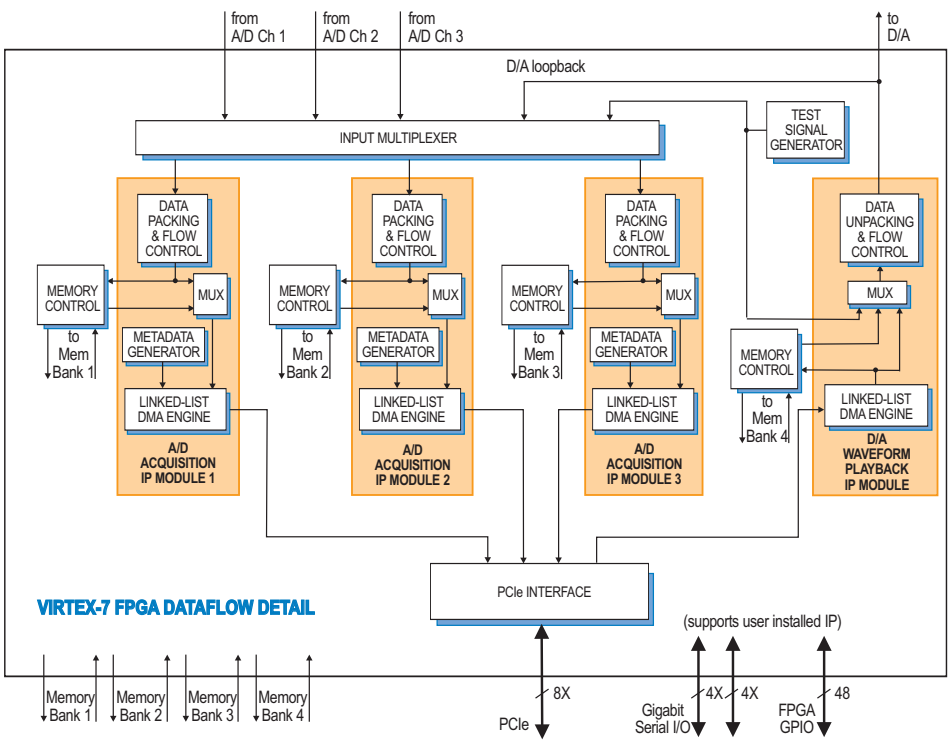
A/D Converter Stages

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages. ➤



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Models 57720 & 58720

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U Open VPX

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex7 FPGA - 6U VPX
58720	6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A with two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57720; P3 and P5 connectors, Model 58720
-105	Gigabit link between the FPGA and P2 connector, Model 57720; gigabit links from each FPGA to P2 connector, Model 78720

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Specifications

Model 57620: 3 A/Ds, 1 DUC, 2 D/As
Model 58620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (3 or 6)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720.

Memory Banks (4 or 8)
- **Type:** DDR3 SDRAM
- **Size:** 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Models 57721 & 58721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U OpenVPX

Model 58721

General Information

Models 57721 and 58721 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71721 XMC modules mounted on a VPX carrier board.

Model 57721 is a 6U board with one Model 71721 module while the Model 58721 is a 6U board with two XMC modules rather than one.

These models include three or sixA/Ds, programmable DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful programmable DDC IP core. The waveform playback IP module contains one or two intrepolation IP cores, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

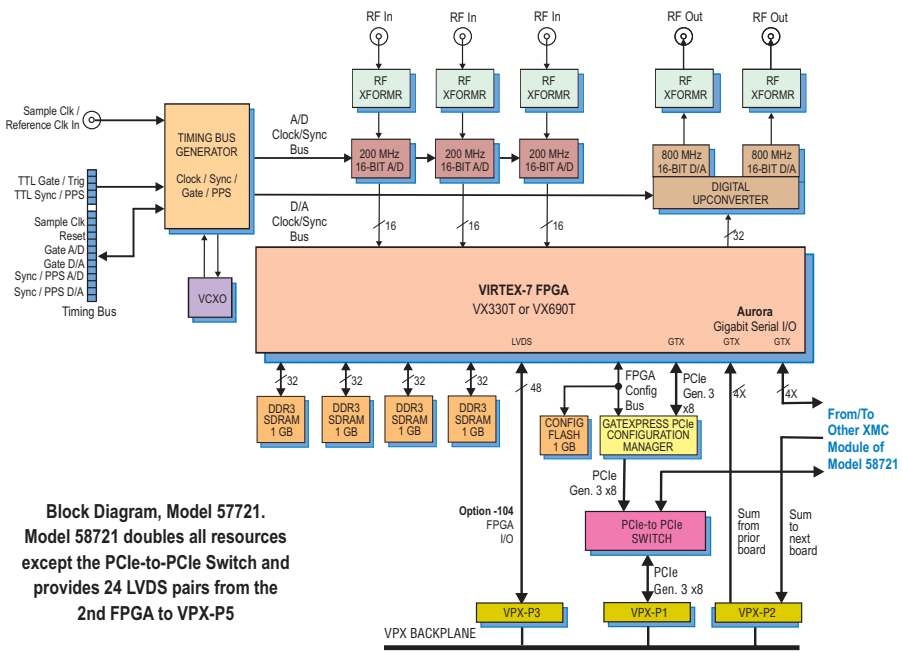
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57721; P3 and P5, Model 58721.➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs
- One or two DUCs
- Two or four 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57721. Model 58721 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57721 & 58721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U OpenVPX

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

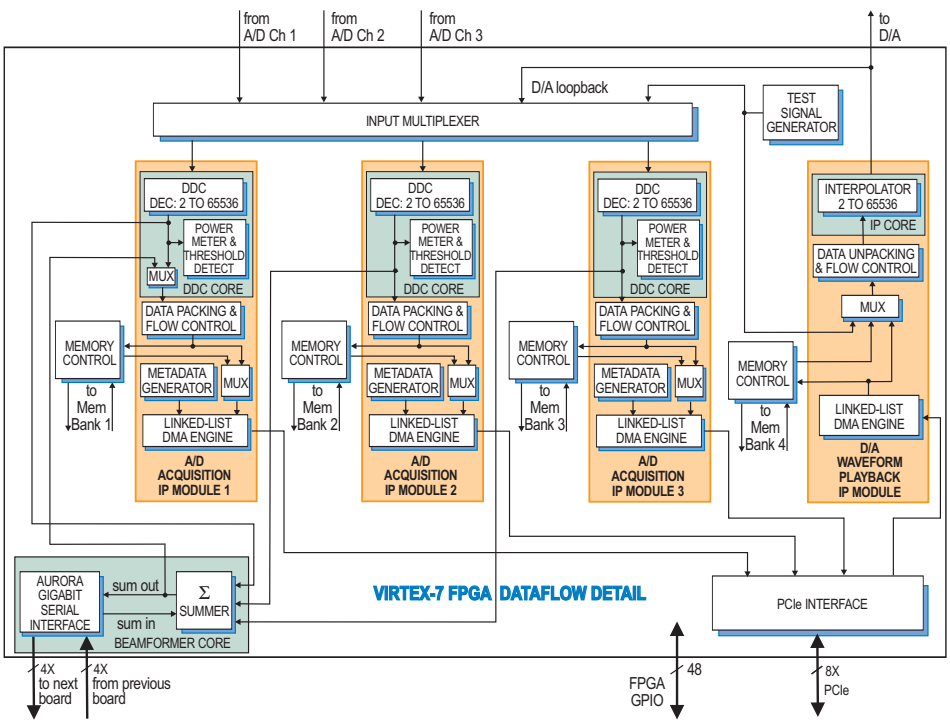
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

Thefactory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U OpenVPX

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUC (digital upconverters) and D/As accept baseband real or complex data stream from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57721 & 58721

3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57721	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U VPX
58721	6-Channel 200 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57721; P3 and P5 connectors, Model 58721

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 57721: 3 A/Ds, 1 DUC, 2 D/As
Model 58721: 6 A/Ds, 2 DUCs, 4 D/As
Front Panel Analog Signal Inputs (3 or 6)
Input: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (3 or 6)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits
Digital Interpolators (1 or 2)
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Beamformers (1 or 2)
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via VPX P2 connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit
Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57721; P3 and P5, connectors, Model 58721
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

➤

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New!

Models 57730 & 58730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

Model 58730

Onyx

GateXpress

GateFlow

ReadyFlow Board Support Package

General Information

Models 57730 and 58730 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a VPX carrier board.

Model 57730 is a 6U board with one Model 71730 module while the Model 58730 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

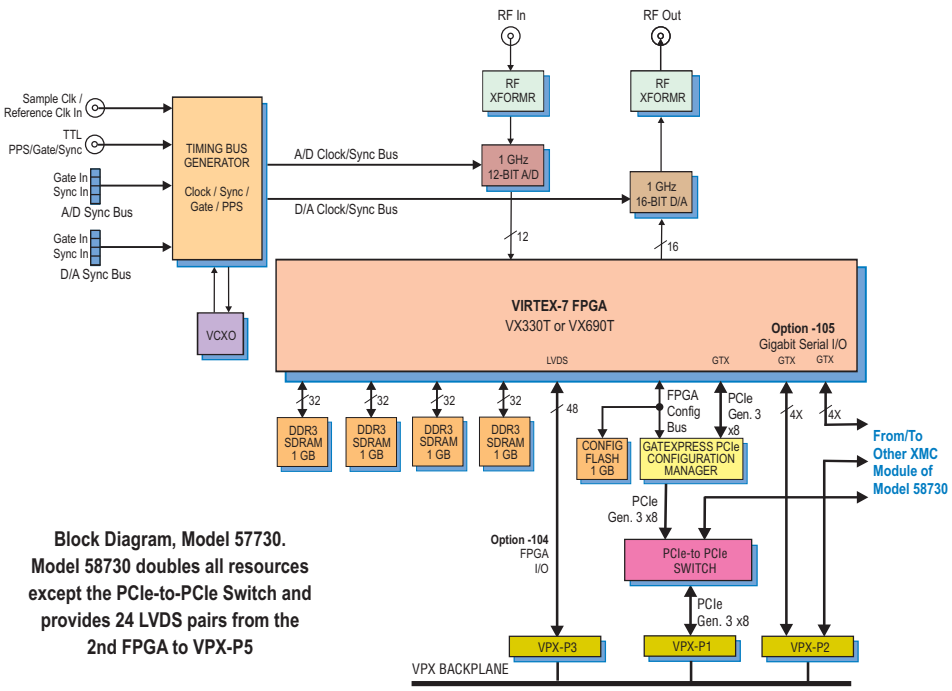
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57730. Model 58730 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57730 & 58730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

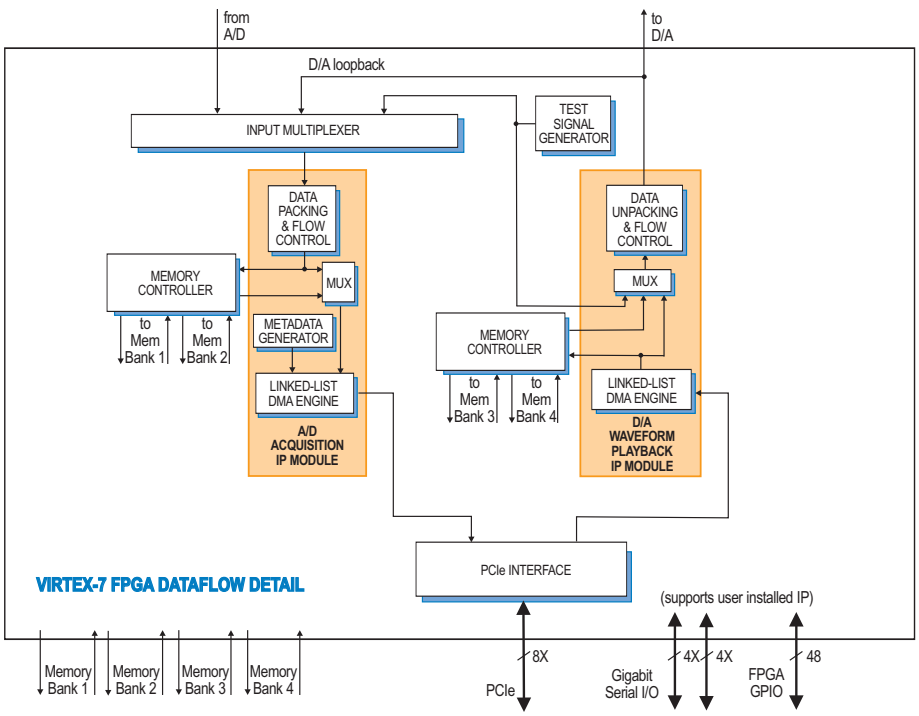
A/D Converter Stages

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.

D/A Converter Stages

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to acept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2- or 1/4-rate input data. Analog output is through front panel SSMC connectors. ➤



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Models 57730 & 58730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57730	1 GHz A/D and D/A with Virtex-7 FPGA - 6U VPX
58730	Two 1 GHz A/Ds and D/As, with two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57730; P3 and P5 connectors, Model 58730
-105	Gigabit link between the FPGA and P2 connector, Model 57730; gigabit links from each FPGA to P2 connector, Model 78730

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 9192 Cobalt or Onyx Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 57730: 1 A/D, 1 D/A
Model 58730: 2 A/Ds, 2 D/As
Front Panel Analog Signal Inputs (1 or 2)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converters (1 or 2)
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs (1 or 2)
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus (1 or 2): 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O (1 or 2)
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57741 & 58741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGAs - 6U OpenVPX

Model 58741

General Information

Models 57741and 58741 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a VPX carrier board.

Model 57741 is a 6U board with one Model 71741 module while the Model 58741 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

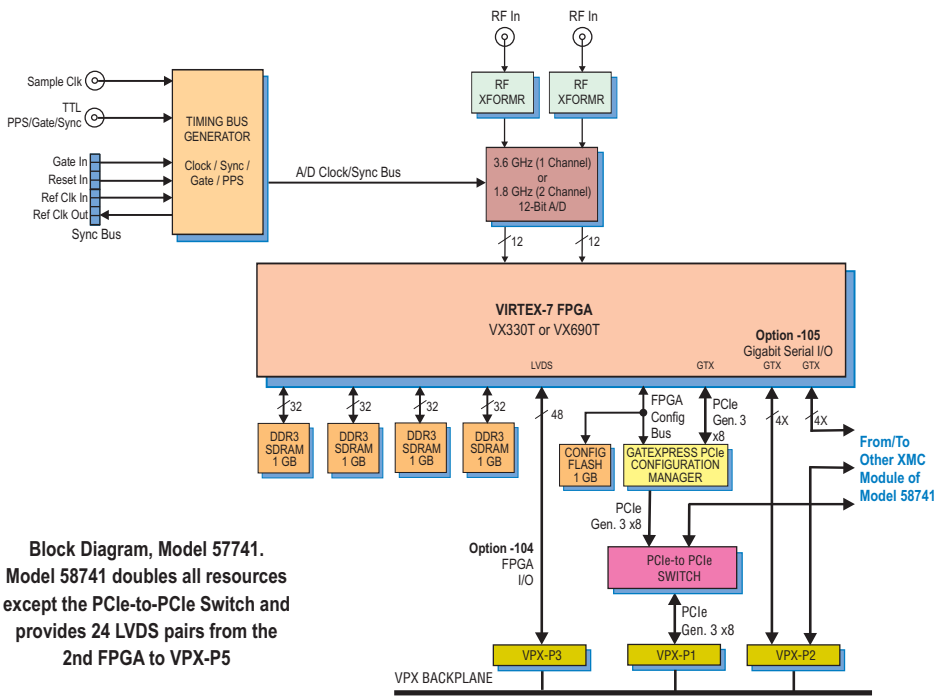
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57741. Model 58741 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57741 & 58741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGAs - 6U OpenVPX

A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, four banks are used to store the single-channel of input data. In dual-channel mode, two memory banks store data from input channel 1 and two memory banks store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Core

Within each FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

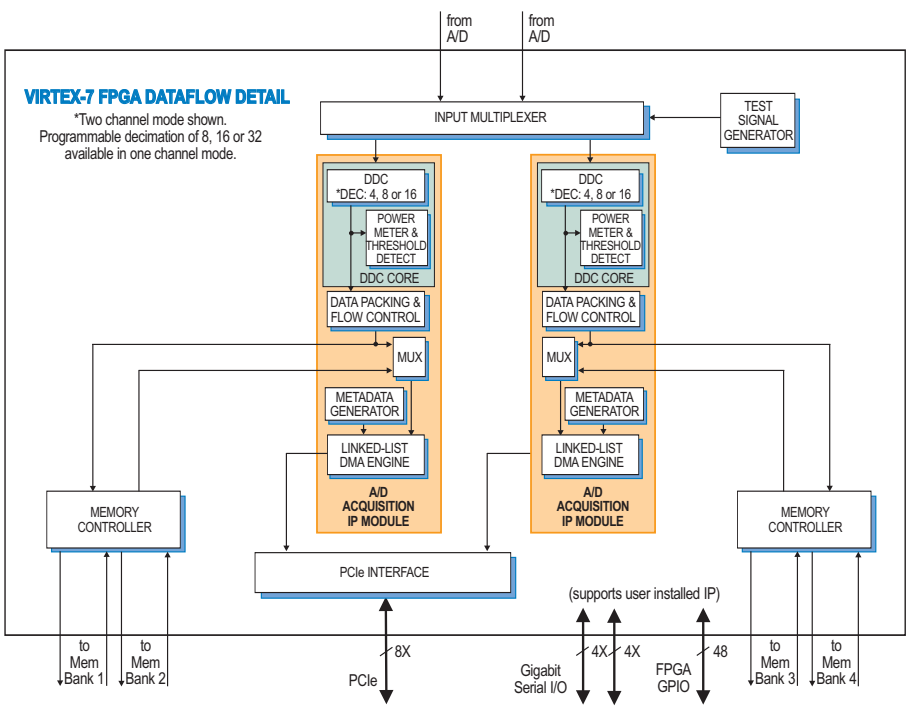
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57741 & 58741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGAs - 6U OpenVPX

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U VPX
58741	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57741; P3 and P5 connectors, Model 58741
-105	Gigabit link between the FPGA and P2 connector, Model 57741; gigabit links from each FPGA to P2 connector, Model 78741

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two boards can be synchronized with a simple cable. For larger systems, multiple boards can be synchronized using the Model 5292 high-speed sync board to drive the sync bus.

Specifications

Model 57741: One A/D
Model 58741: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Sources (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741.
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57751 & 58751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - 6U OpenVPX

Model 58751

Onyx7

GateXpress

GateFlow

ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Models 57751 and 58751 are members of the Onyx® family of high-performance 6 U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a VPX carrier board.

Model 57751 is a 6U board with one Model 71751 module while the Model 58751 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules.

IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

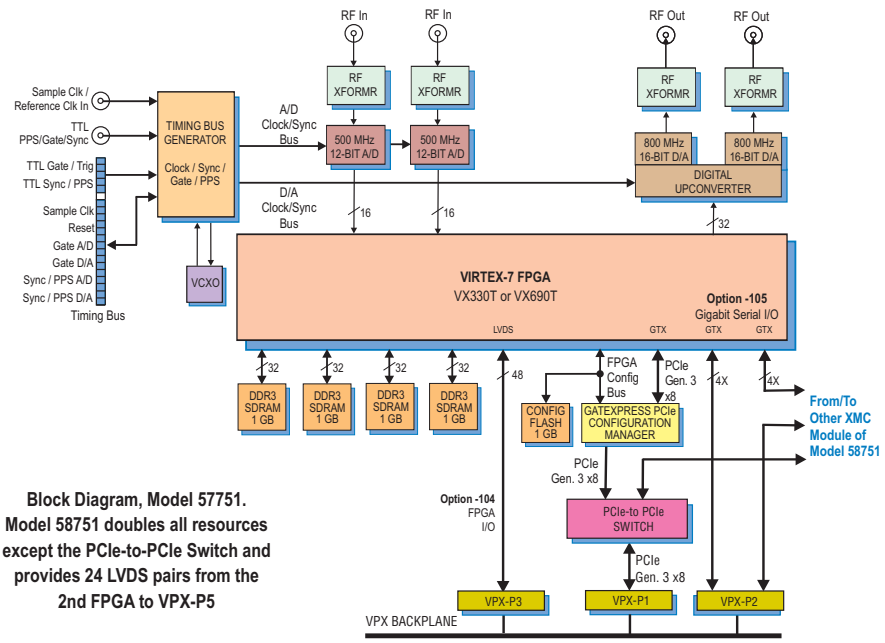
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57751; P3 and P5, Model 58751.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57751; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58751. ➤



Block Diagram, Model 57751. Model 58751 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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Models 57751 & 58751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP Module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

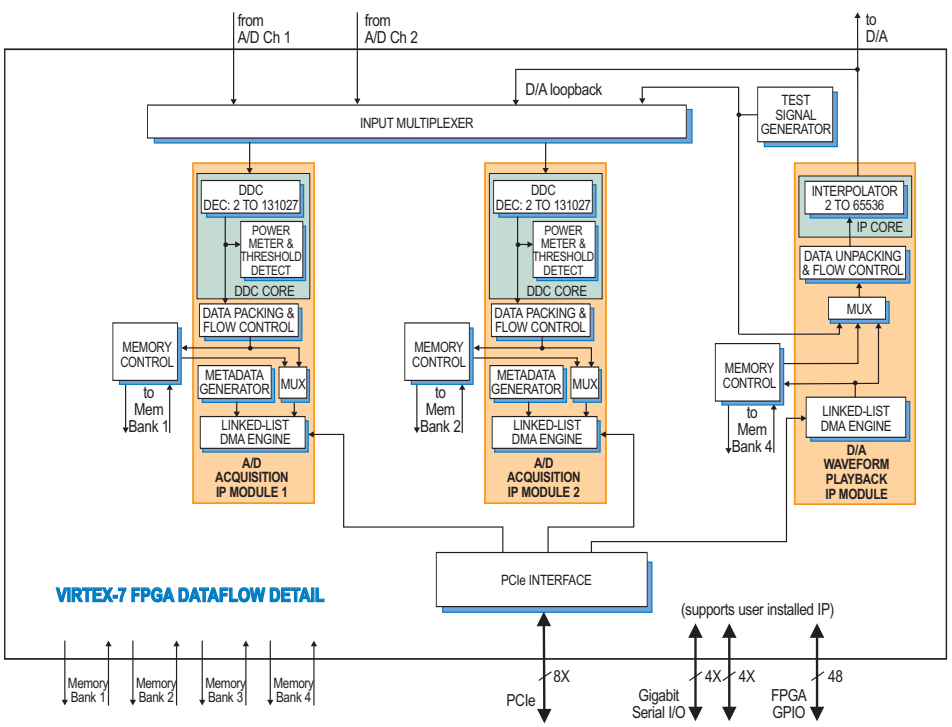
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. ➤



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➤ In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, Texas Instruments ADS5474 400 MHz, 14-bit A/Ds may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept the baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog outputs are through front-panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57751 & 58751

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2-or 4-Channel 800 MHz D/A with Virtex-7 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U VPX
58751	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs - 6U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57751; P3 and P5 connectors, Model 58751
-105	Gigabit link between the FPGA and P2 connector, Model 57751; gigabit links from each FPGA to P2 connector, Model 78751

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57751: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

Model 58751: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014) (2 or4)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters (2 or 4)
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2) 26-pin connector
- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57751; P3 and P5, Model 58751
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57751; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58751

Memory Banks (4 or 8)
- **Type:** DDR3 SDRAM
- **Size:** 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Models 57760 & 58760

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 6U OpenVPX

Model 58760

General Information

Models 57760 and 58760 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a VPX carrier board.

Model 57760 is a 6U board with one Model 71760 module while the Model 58760 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

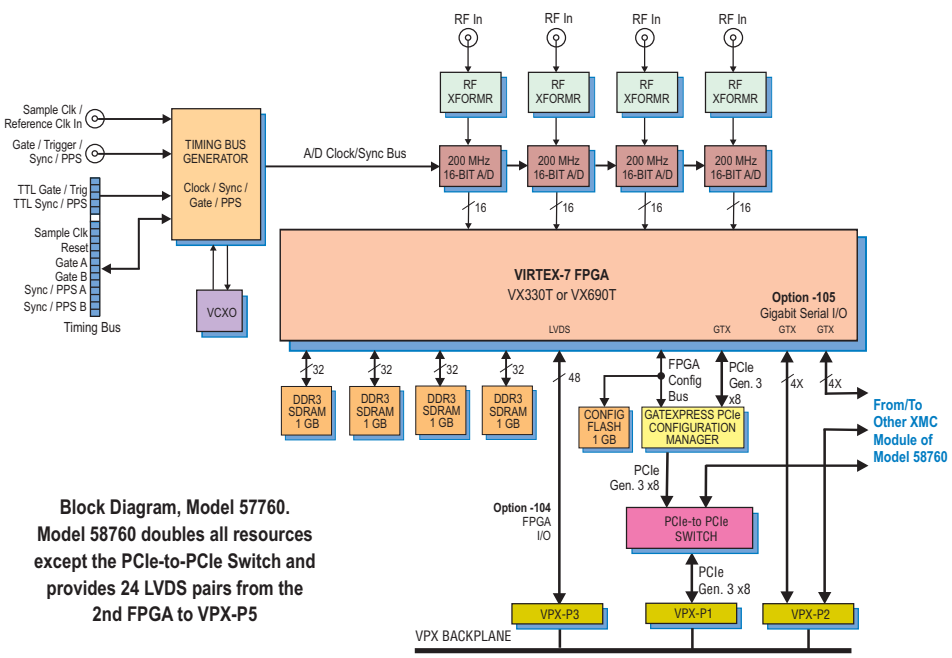
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57760. Model 58760 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 6U OpenVPX

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

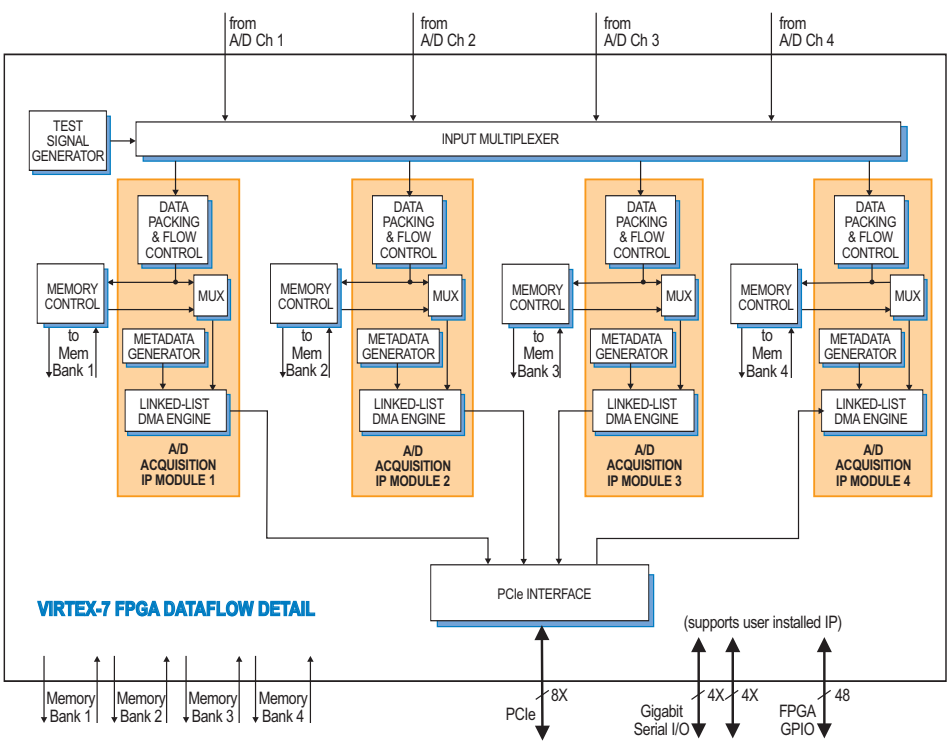
The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources. ➤

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



Models 57760 & 58760

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U VPX
58760	8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57760; P3 and P5 connectors, Model 58760
-105	Gigabit link between the FPGA and P2 connector, Model 57760; gigabit links from each FPGA to P2 connector, Model 78760

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57760: 4 A/Ds
Model 58760: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources: (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or 2)
26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760.
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Models 57761 & 58761

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

Model 58761

General Information

Models 57761 and 58761 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71761 XMC modules mounted on a VPX carrier board.

Model 57761 is a 6U board with one Model 71761 module while the Model 58761 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, programmable DDCs and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

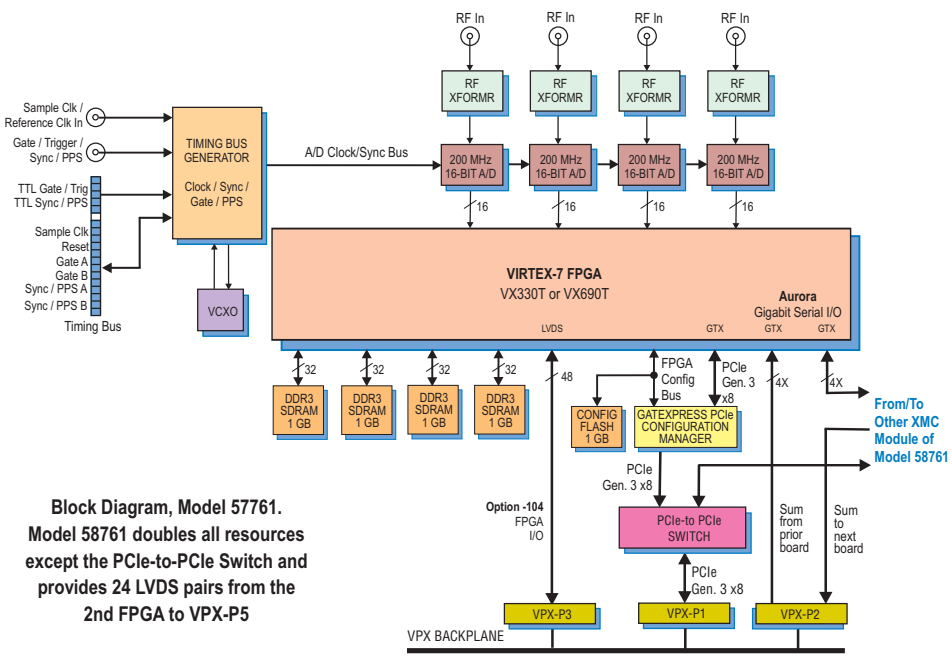
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57761; P3 and P5, Model 58761. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- Multiboard programmable beamformer
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57761. Model 58761 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57761 & 58761

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

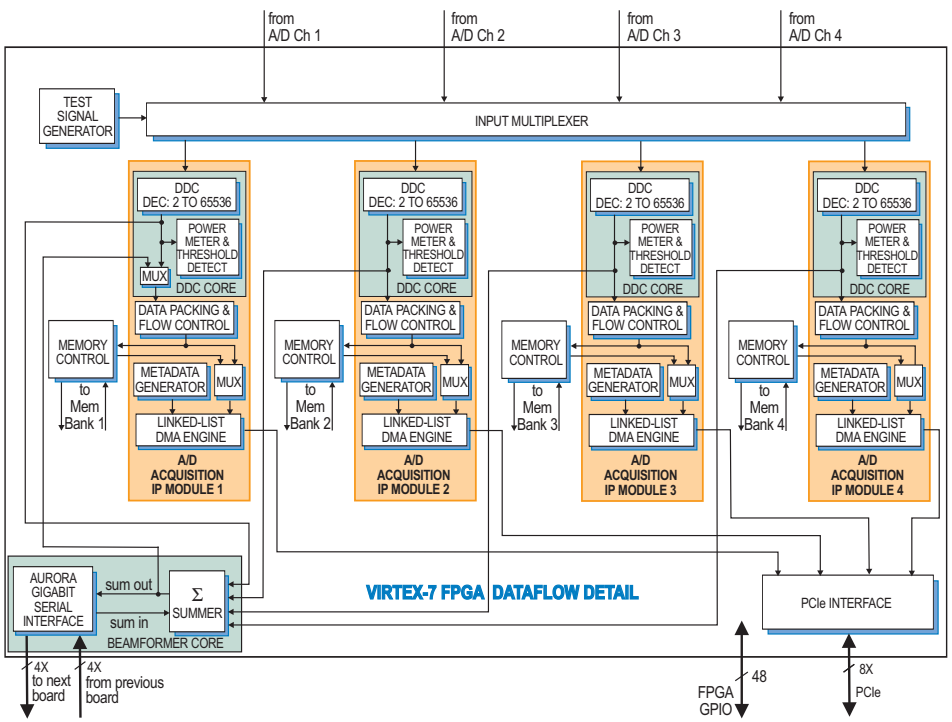
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57761 & 58761

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
57761	4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 6U VPX
58761	8-Channel 200 MHz A/D with DDCs, two Virtex-7 FPGAs - 6U VPX
Option:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57761; P3 and P5 connectors, Model 58761

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57761: 4 A/Ds,
Model 58761: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via VPX P2 connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources (1 or 2)
On-board clock synthesizer

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2) 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57761; P3 and P5, Model 58761

Memory Banks (4 or 8)
- **Type:** DDR3 SDRAM
- **Size:** 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Models 57791 & 58791

1 or 2 L-Band RF Tuners, 2-or 4-Channel 500 MHz A/D, Virtex-7 FPGAs - 6U VPX

Model 58791

Onyx

GateXpress

GateFlow

ReadyFlow Board Support Package

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs handle L-Band input signal levels from –50 dBm to +10 dBm
- Programmable analog down-converters provide IF or I+Q baseband signals at frequencies up to 123 MHz
- Two or four 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two or four FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Models 57751 and 58751 are members of the Onyx® family of high-performance 6U VPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a 6U VPX carrier board.

Model 57791 is a 6U board with one Model 71791 module while the Model 58751 is a 6U board with two XMC modules rather than one.

They include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features one or two Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The factory-installed functions include two or four A/D acquisition IP modules, four or eight DDR3 memory controllers, two or four DDCs (digital downconverters), RF tuner controllers, one or two clock and synchronization generators, one or two test signal generators, and a Gen 3 PCIe interface.

These models can operate as complete turnkey solutions with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

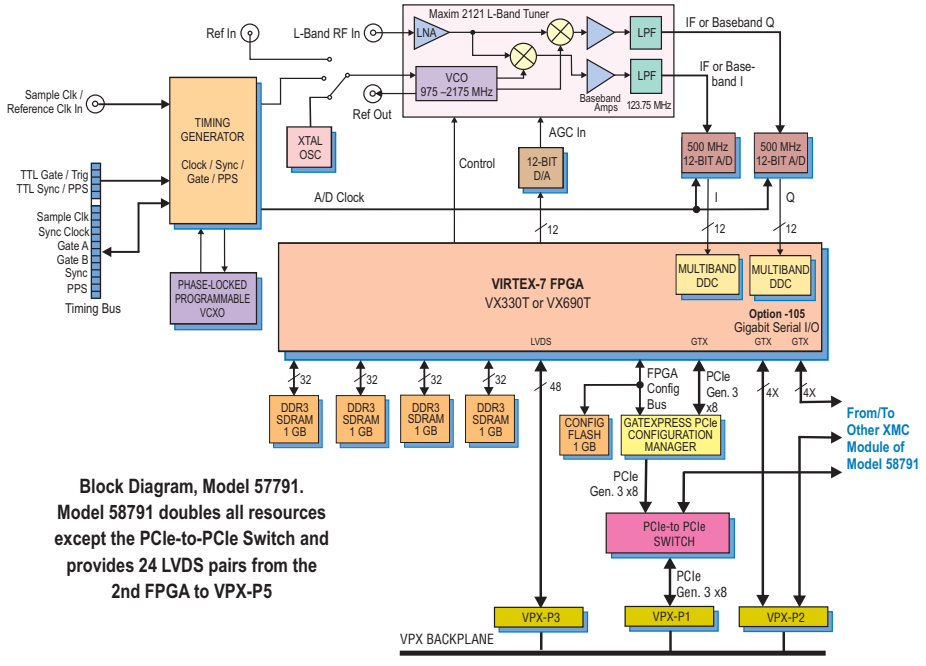
Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57791; P3 and P5, Model 58791.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57791; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58751. ➤



Block Diagram, Model 57791. Model 58791 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57791 & 58791

1 or 2 L-Band RF Tuners, 2-or 4-Channel 500 MHz A/D, Virtex-7 FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ RF Tuner Stage

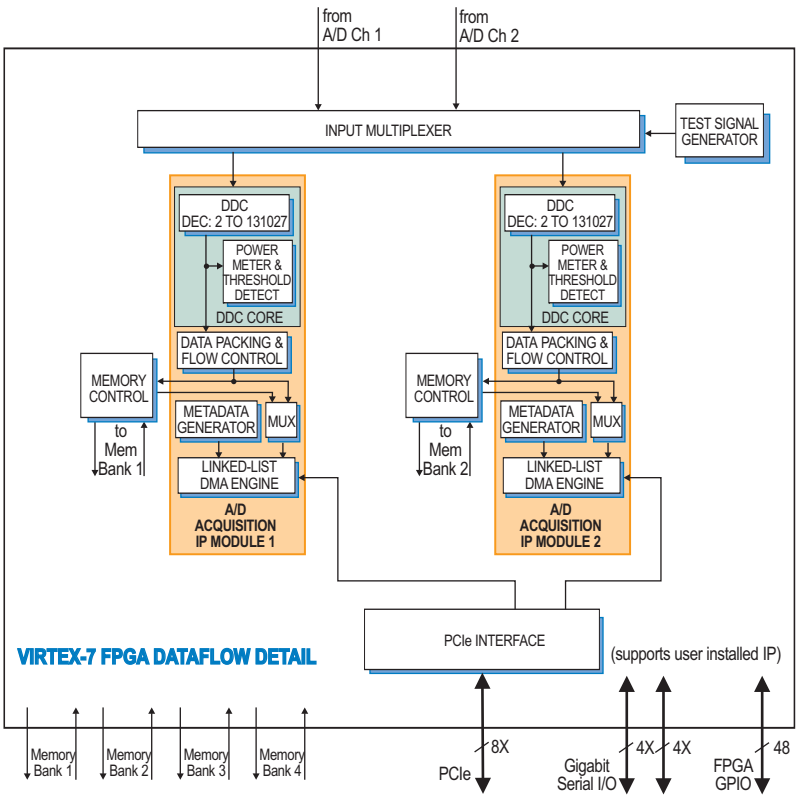
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The analog tuner outputs are digitized by two or four Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two or four independent A/D and DDC channels are now available for digitizing and downconverting signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

One or two internal timing generators provide all timing, gating, triggering and synchronization functions required by the A/D converters. They also serve as optional sources for the L-Band tuner references.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent 1 GB DDR3 SDRAMs for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be used to support custom user-installed IP within the FPGA .

PCI Express Interface

Models 57791 and 58791 include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57791 & 58791

1 or 2 L-Band RF Tuners, 2-or 4-Channel 500 MHz A/D, Virtex-7 FPGAs - 6U VPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
57791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 6U VPX
58791	Two L-Band RF Tuners with 4-Channel 500 MHz A/D with DDCs and two Virtex-7 FPGAs - 6U VPX
Options:	
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS I/O between the FPGA and P3 connector, Model 57791; P3 and P5 connectors, Model 58791
-105	Gigabit link between the FPGA and P2 connector, Model 57791; gigabit links from each FPGA to P2 connector, Model 78791

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8264	VPX Development System. See 8264 Datasheet for Options

➤ Specifications

Model 57791: 1 L-Band Tuner, 2 A/Ds, 2 DDCs, 1 FPGA
Model 58791: 2 L-Band Tuners, 4 A/Ds, 4 DDCs, 2 FPGAs
Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuner (1 or 2)
Type: Maxim MAX2121
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: $freq_{VCO} = (N.F.) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz
A/D Converters (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 10 MHz to 500 MHz
Resolution: 12 bits
Option -014: 400 MHz, 14-bit A/Ds
Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer
A/D Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Input (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus (1 or 2)
26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Input (2 or 4)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57791; P3 and P5, Model 58791
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57791; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58791
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3*: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

* Gen 3 requires a compatible backplane and SBC

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Models 57131 & 58131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

Model 58131

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports one or two Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 multiband DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57131 and 58131 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71131 XMC modules mounted on a VPX carrier board. Model 57131 is a 6U board with one Model 71131 module while the Model 58131 is a 6U board with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

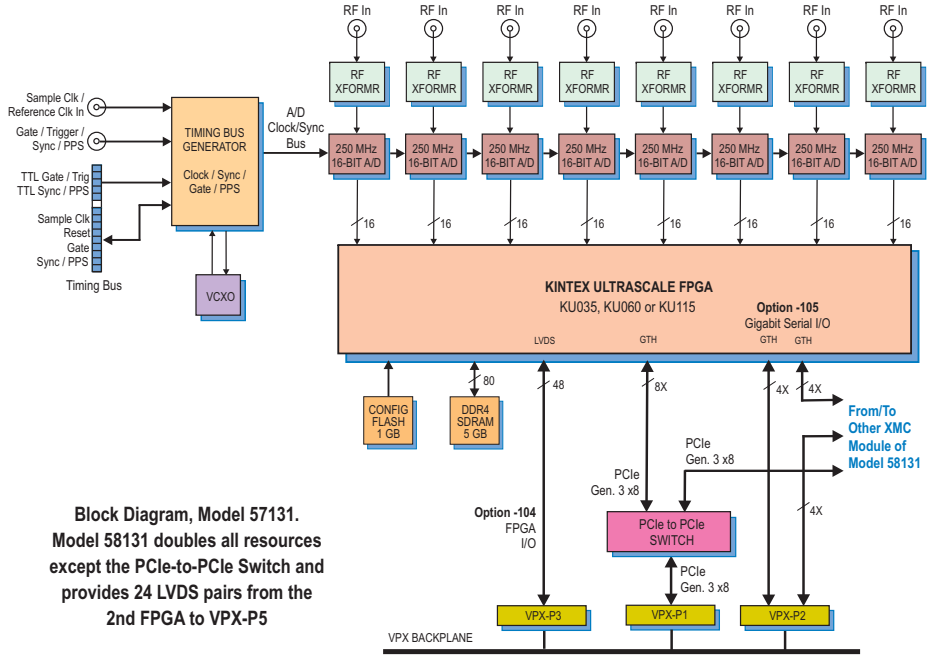
Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the ➤



Block Diagram, Model 57131. Model 58131 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57131 & 58131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients.

The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts eight or 16 analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

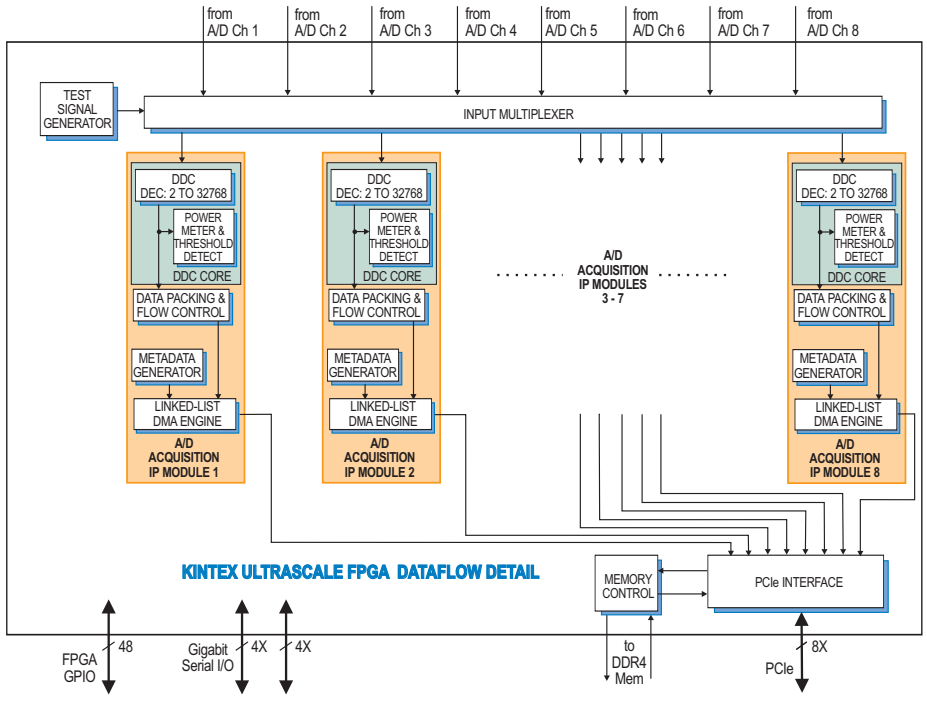
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight or four.

Memory Resources

The architecture supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 ➤



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Models 57131 & 58131

8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57131	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
58131	16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57131: 8 A/Ds;
Model 58131: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8 or 16)
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters (8 or 16)
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
On-board clock synthesizers

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57131; and P5 connector, Model 58131 for custom I/O
- **Option -105** provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB Model 57131; 10 GB Model 58131
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 9.187 in. x 6.717 in. (233.35 mm x 170.60 mm)

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New!

Models 57132 & 58132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U VPX

Model 58132

JADE

NAVIGATOR Design Suite

General Information

Models 57132 and 58132 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71132 XMC modules mounted on a VPX carrier board. Model 57132 is a 6U board with one Model 71132 module while the Model 58132 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

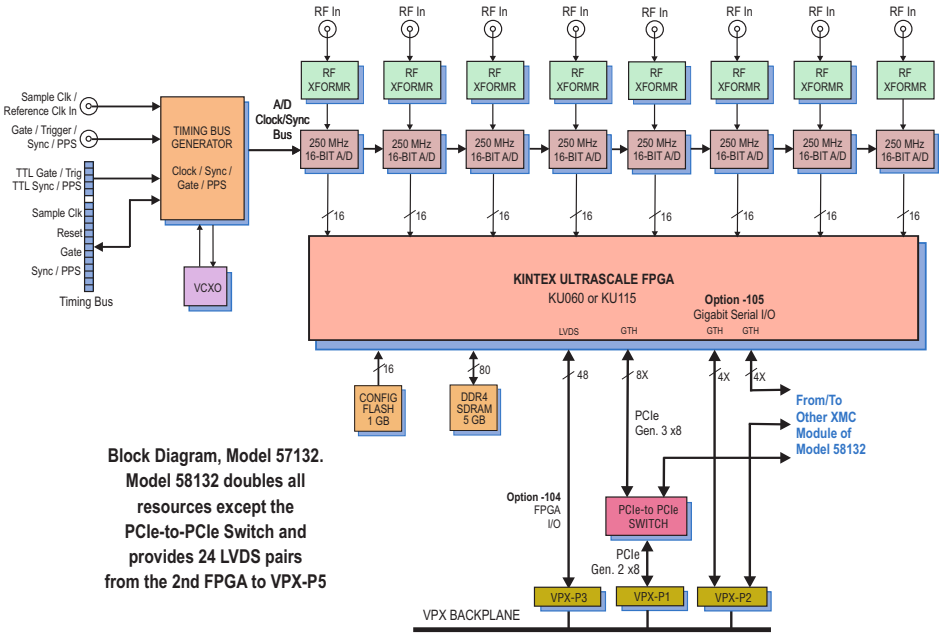
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 wideband DDCs
- 64 or 128 multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57132. Model 58132 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57132 & 58132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U VPX

A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filter for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57132; P3 and P5 connectors, Model 58132.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into eight or 16 TI ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

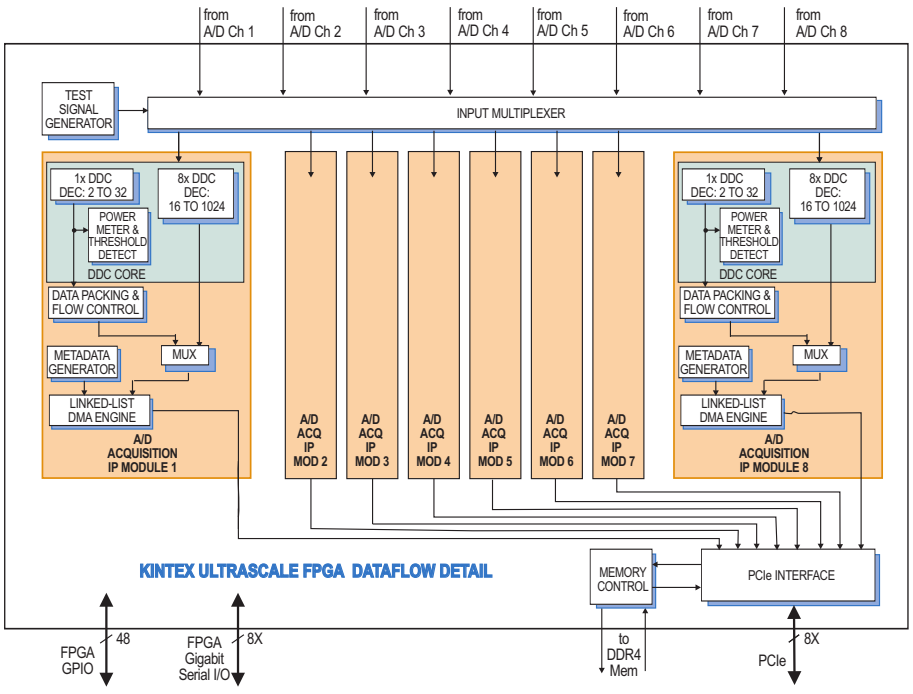
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied ➤



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Models 57132 & 58132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57132	8-Channel 250 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U VPX
58132	16-Channel 250 MHz A/D with multiband DDCs and two Kintex UltraScale FPGAs - 6U VPX

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P3, Model 57132; P3 and P5 Model 58132
-105	Gigabit serial FPGA I/O to VPX P2
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Specifications

Model 57132: 8 A/Ds; Model 58132: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8 or 16)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters (8 or 16)
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (64 or 128)
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57132; P3 and P5 connectors, Model 58132, for custom I/O
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2 banks)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB or 10 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: board 9.187 in x 6.717 in (233.35 mm x 170.60 mm)

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New

Models 57141 & 58141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

Model 58141

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One or two-channel mode with 6.4 GHz, 12-bit A/Ds
- Two-or four-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two or four-Channel 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57141 and 58141 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a VPX carrier board. Model 57141 is a 6U board with one Model 71141 module while the Model 58141 is a 6U board with two XMC modules rather than one.

They includet two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

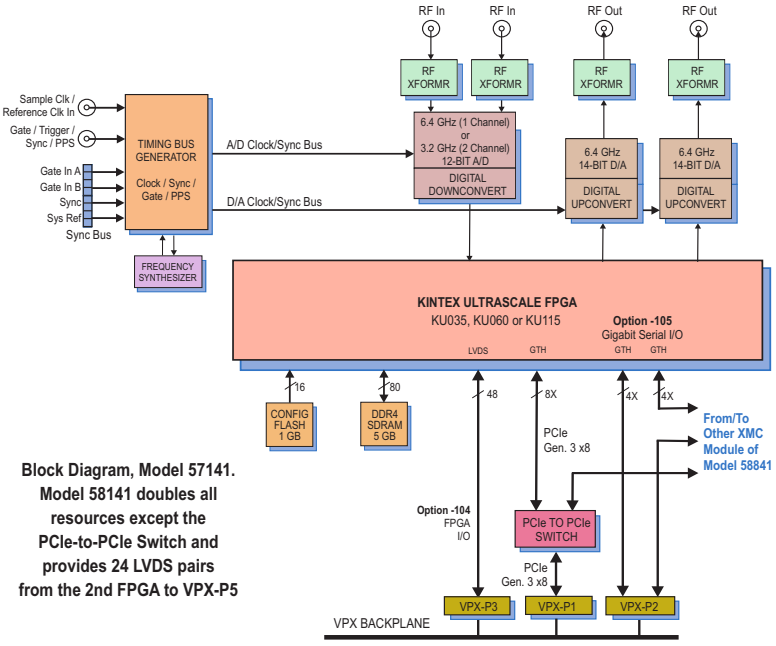
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include two or four A/D acquisition and two or four D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



Block Diagram, Model 57141. Model 58141 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57141 & 58141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory- installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

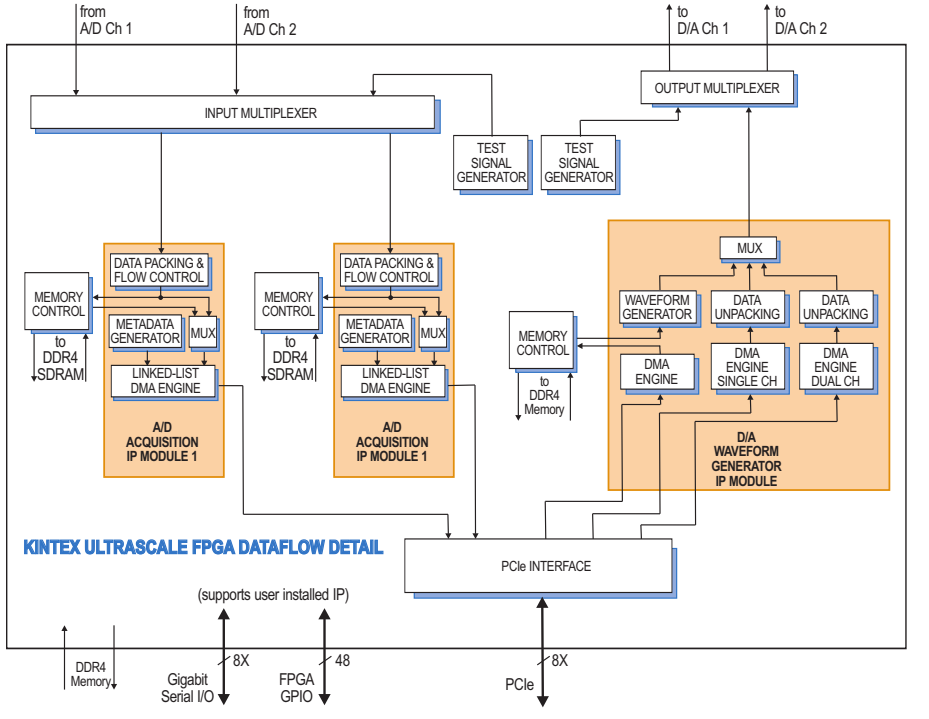
PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

These models accept a sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57141 & 58141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

➤ for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5792 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Specifications

Model 57141 One A/D
Model 58141 Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters (2 or 4)
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.
Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.
Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 or 10 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Ordering Information

Model	Description
57141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 6U VPX
58141	2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, 4-Ch. 6.4 GHz D/A, 2 ea. Ultra-Scale FPGAs - 6U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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New!

Models 57821 & 58821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

Model 58821

JADE

NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57821 and 58821 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71821 XMC modules mounted on a VPX carrier board. Model 57821 is a 6U board with one Model 71821 module while the Model 58821 is a 6U board with two XMC modules rather than one.

They include three or six A/Ds, complete multiboard clock and sync sections, large DDR4 memory, three or six DDCs, one or two DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

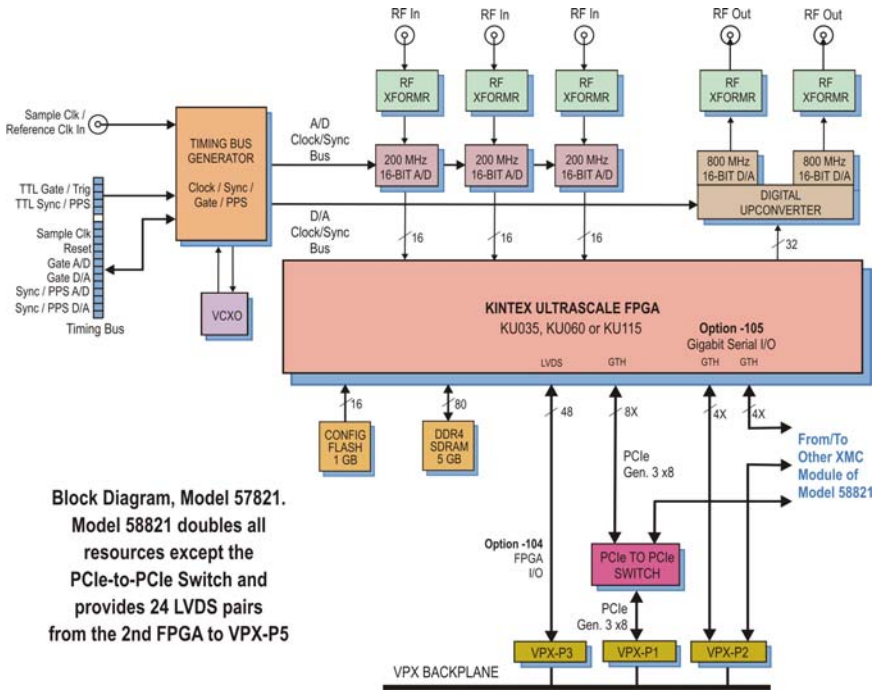
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The factory-installed functions for these models include three or six A/D acquisition and one or two waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three or six powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; programmable interpolators, and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



Block Diagram, Model 57821. Model 58821 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 57821 & 58821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from three A/Ds, or the test signal generators.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board memory or off- board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition rate etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

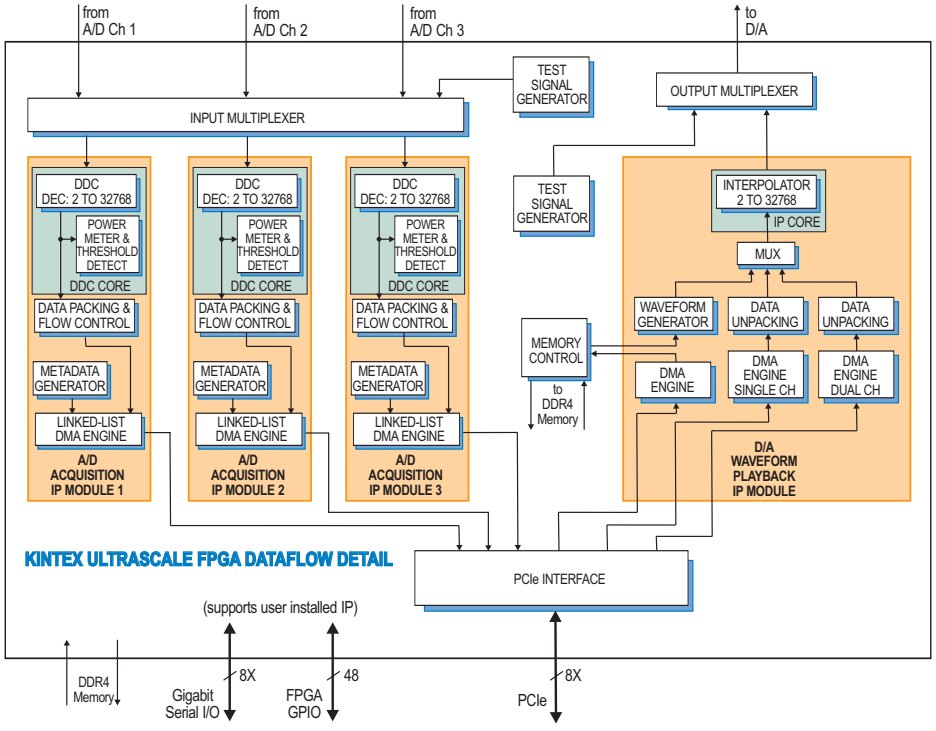
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57821; P3 and P5 connectors, Model 58821.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57821 & 58821

3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX
58821	6-Channel 200 MHz A/D with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGAs - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Specifications

Model 57821: 3 A/Ds
Model 58821: 6 A/Ds
Front Panel Analog Signal Inputs (3 or 6)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (3 or 6)
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
D/A Converters (1 or 2)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits
Digital Interpolator Core (1 or 2)
Interpolation Range: 2x to 32,768x in three stages of 2x to 32x
Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x
Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57821; P3 and P5 connectors, Model 58821
Option -105 provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols
Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

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New!

Models 57841 & 58841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz, 12-bit A/Ds, with Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX

Model 58841

JADE NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57841 and 58841 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

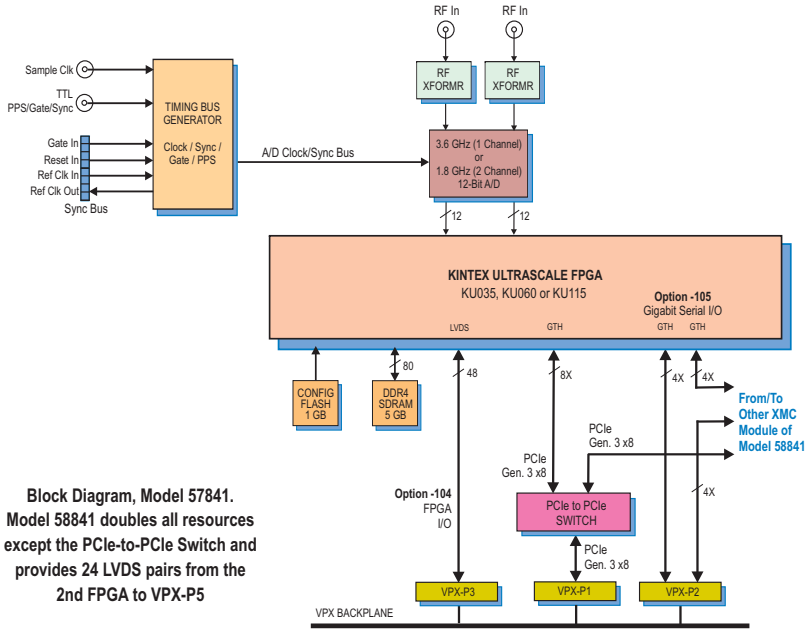
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, ➤



Block Diagram, Model 57841. Model 58841 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57841 & 58841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz, 12-bit A/Ds, with Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

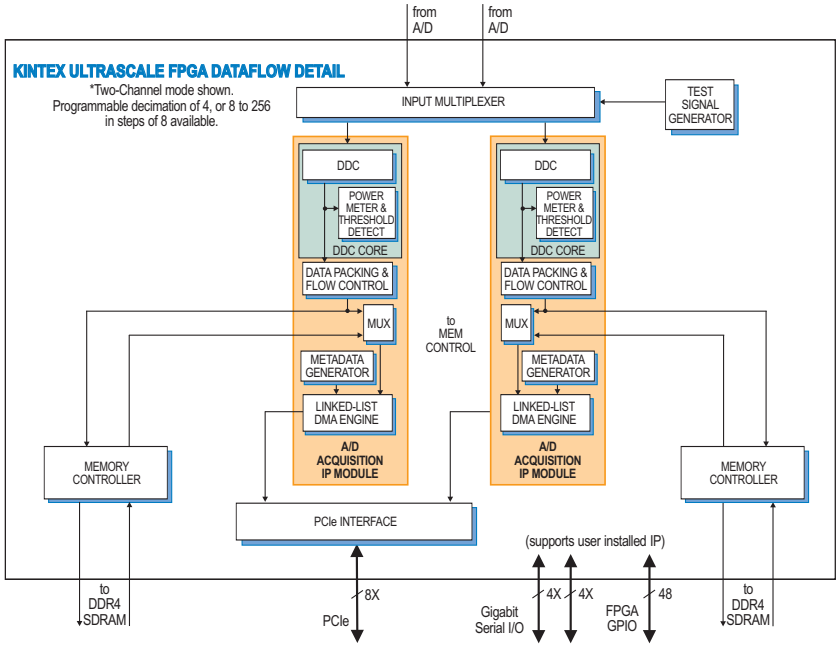
The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high- speed sync module to drive the sync bus. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57841 & 58841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz, 12-bit A/Ds, with Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX
58841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2, Model 57861; P2 and P5 Model 58861
-105	Gigabit serial FPGA I/O to VPX P1
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Memory Resources

The architecture supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Specifications

Model 57861: One A/D
Model 58861: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer
Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: (1 or 2)
Front panel SSMC connectors
Timing Bus: (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57861; and P5 connector, Model 58861 for custom I/O
Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory
Type: DDR4 SDRAM
Size: 5 GB Model 57841; 10 GB Model 58841
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Models 57851 & 58851

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - 6U VPX

Model 58851

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUC (digital upconverter)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

General Information

Models 57851 and 58851 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71851 XMC modules mounted on a VPX carrier board. Model 57851 is a 6U board with one Model 71851 module while the Model 58851 is a 6U board with two XMC modules rather than one.

They include two or four A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

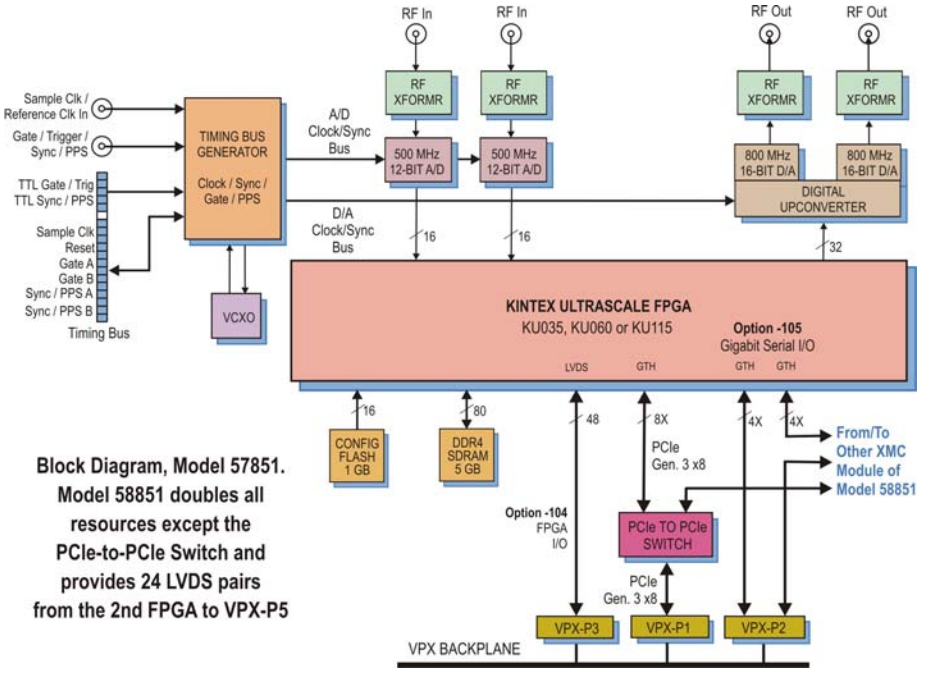
The factory-installed functions of these models include two or four A/D acquisition and two or four waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: two or four powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for data clocking and synchronization functions; test signal generators; programmable interpolators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions thereby saving the time of IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



Block Diagram, Model 57851. Model 58851 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57851 & 58851

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/As waveforms stored in either on-board memory or off-board host memory.

➤ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57851; P3 and P5 connectors, Model 58851.

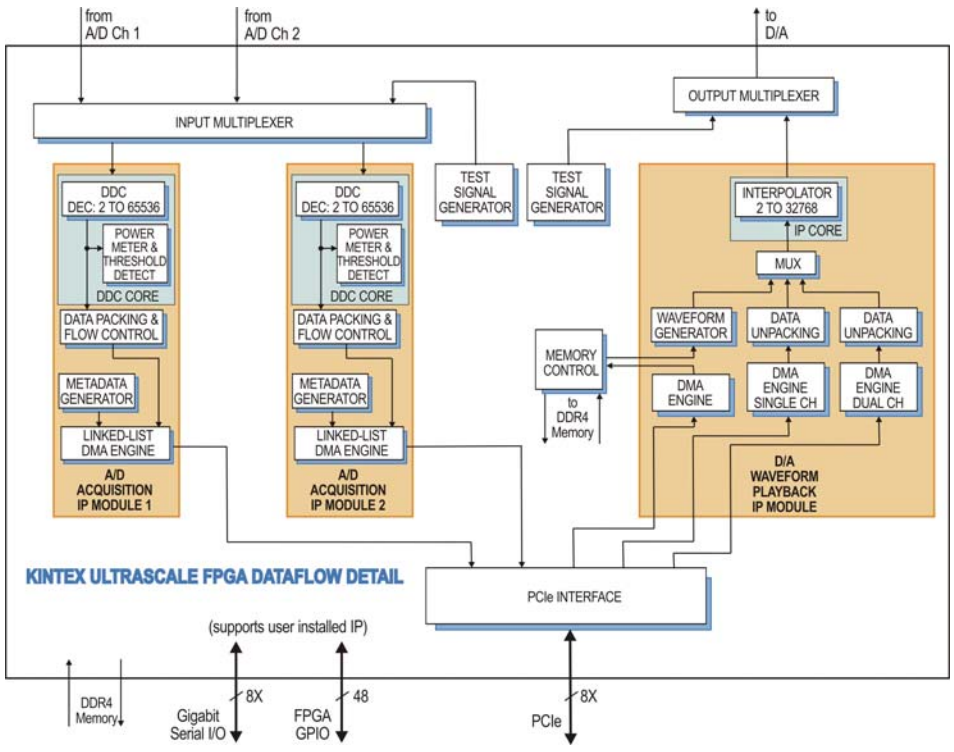
Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

Models 57851 & 58851

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX
58851	4-Channel 500 MHz A/D with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX

Options:

-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Specifications

Model 57851: 2 A/Ds
Model 58851: 4 A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits
A/D Converters (option -014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits
Digital Downconverters (2 or 4)
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits
Digital Interpolator Core (1 or 2)
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x
Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57851; P3 and P5 connectors, Model 58851; for custom I/O
Option -105: provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols
Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U Board 9.187 in x 6.717 in (233.35 mm x 170.61 mm)

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New!

Models 57861 & 58861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

Model 58861

JADE

NAVIGATOR Design Suite

General Information

Models 57861 and 58861 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

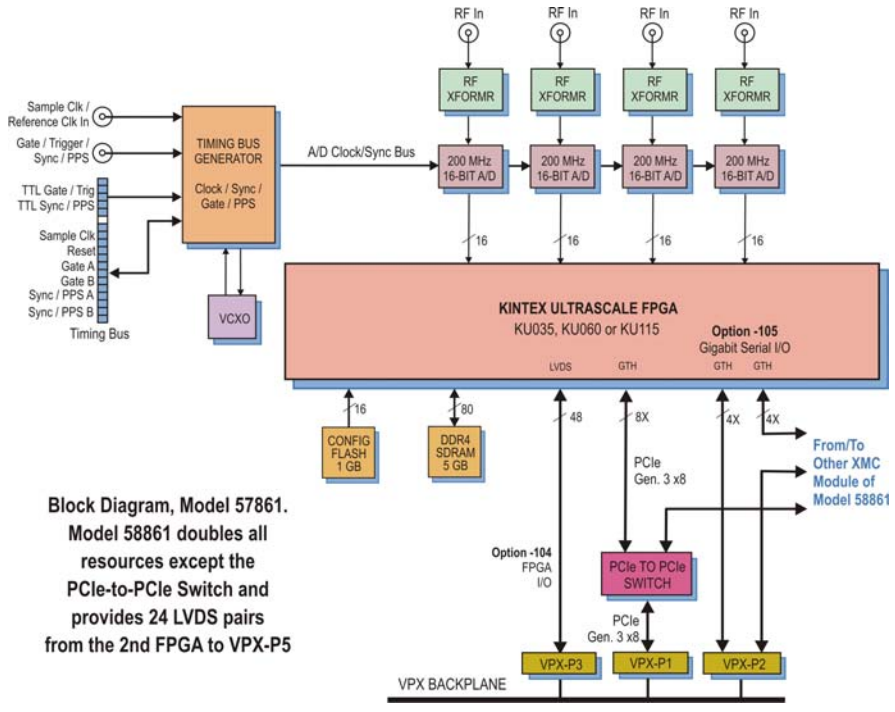
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57861. Model 58861 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57861 & 58861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57861; P3 and P5 connectors, Model 58861.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

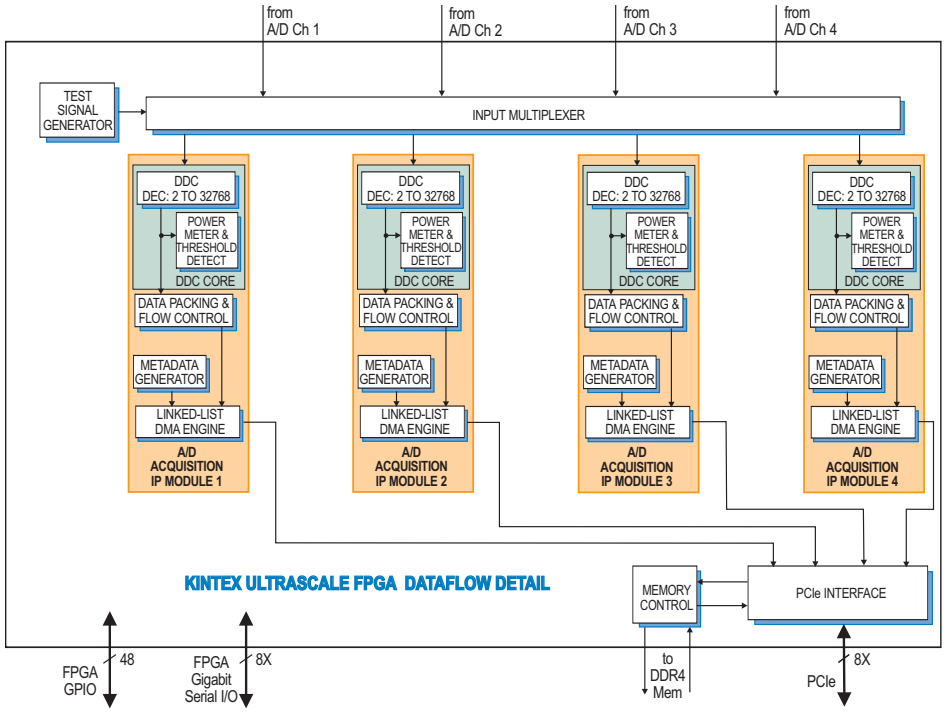
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. ➤



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www.pentek.com

Models 57861 & 58861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264) , they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57861	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
58861	8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P3, Model 57861; P3 and P5 Model 58861
-105	Gigabit serial FPGA I/O to VPX P2
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Specifications

Model 57861: 4 A/Ds
Model 58861: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (4 or 8)
Quantity: Four channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Sources: (1 or 2)
On-board clock synthesizer
Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus (1 or2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57861; P3 and P5 connectors, Model 58861, for custom I/O
Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols
Memory (1 or 2 banks)
Type: DDR4 SDRAM
Size: 5 GB or 10 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: Board 9.187 in x 6.717 in (233.35 mm x 170.60 mm)

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New!

Models 57862 & 58862

4 or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - 6U VPX

Model 58862

JADE

NAVIGATOR Design Suite

General Information

Models 57862 and 58862 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71862 XMC modules mounted on a VPX carrier board. Model 57862 is a 6U board with one Model 71862 module while the Model 58862 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

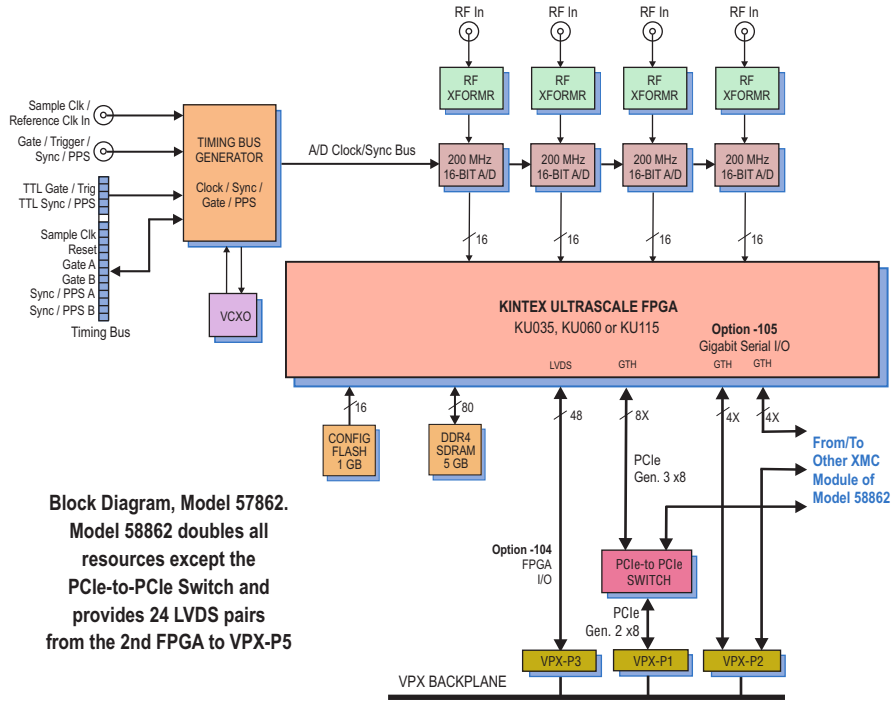
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57862. Model 58862 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57862 & 58862

4 or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - 6U VPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDC s accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57862; P3 and P5 connectors, Model 58862.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

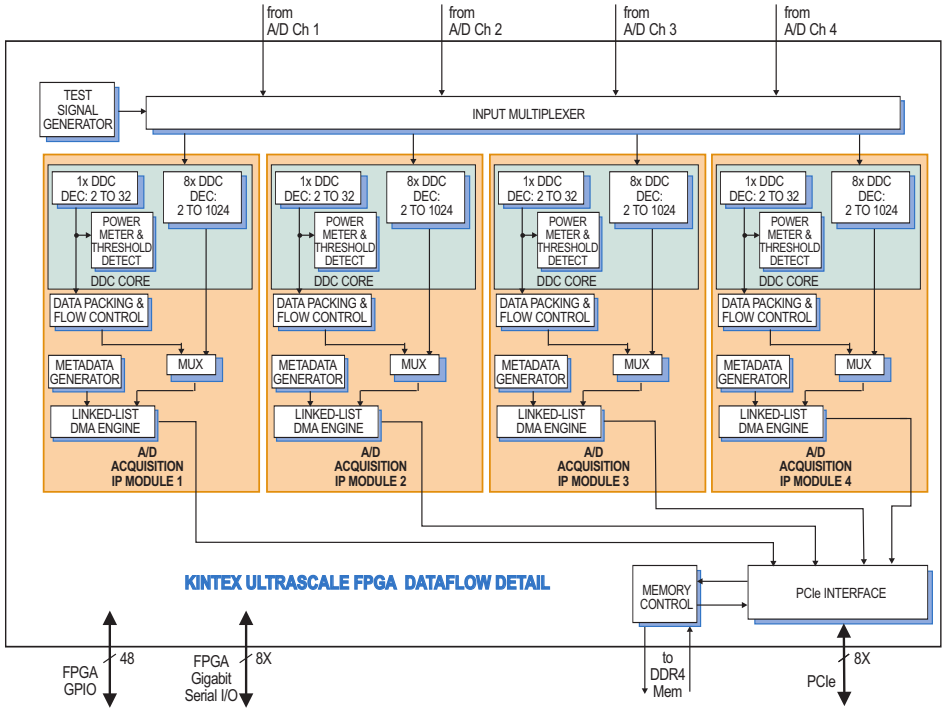
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Models 57862 & 58862

4 or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57862	4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U VPX
58862	8-Channel 200 MHz A/D with multiband DDCs and 2 Kintex UltraScale FPGAs - 6U VPX

Options:

- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P3, Model 57862; P3 and P5 Model 58862
-105	Gigabit serial FPGA I/O to VPX P2
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Specifications

Model 57862: 4 A/Ds; Model 58862: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (4 or 8)
- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57862; P3 and P5 connectors, Model 58862, for custom I/O
- **Option -105** provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2 banks)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB or 10 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Board 9.187 in x 6.717 in (233.35 mm x 170.60 mm)

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New!

Models 57800 & 58800

Kintex UltraScale FPGA Coprocessor- 6U VPX

Model 58800

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex Ultra-Scale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57800 and 58800 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a VPX carrier board. Model 57800 is a 6U board with one Model 71800 module while the Model 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57800 and Model 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

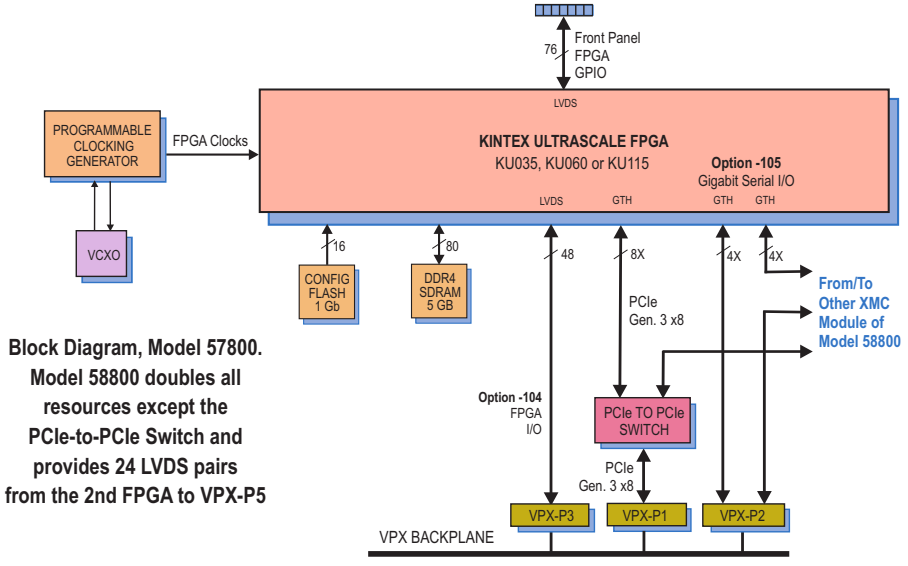
Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols. ➤



Block Diagram, Model 57800. Model 58800 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57800 & 58800

Kintex UltraScale FPGA Coprocessor- 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57800	Kintex UltraScale FPGA Coprocessor - 6U VPX
58800	Double Kintex UltraScale FPGA Coprocessors - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Front-Panel Digital I/O Interface

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Specifications

Front Panel Digital I/O (1 or 2)
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 or 76 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800
- **Option -105** provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

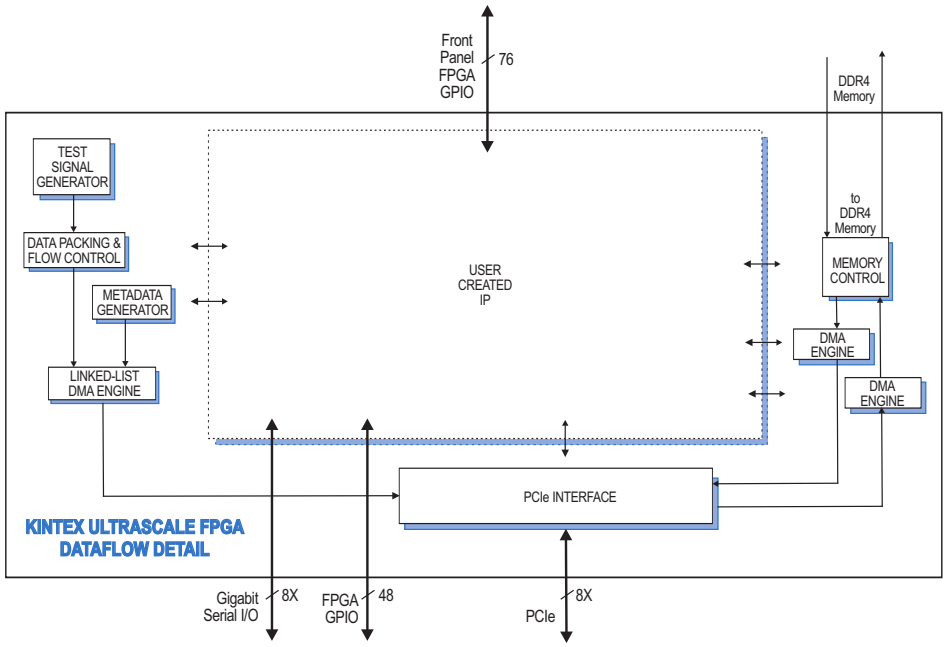
Option -702: L2 (air cooled)
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 8264

6U OpenVPX Development System for Cobalt and Onyx Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 9U 19-inch rackmount, 9-slot, 16-inch deep chassis which houses 6U VPX boards
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box ready-to-run examples

Ordering Information

Model	Description
8264	6U VPX Development System for Cobalt and Onyx Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

General Information

The Model 8264 is a fully-integrated, 6U VPX development system for Pentek Cobalt® and Onyx® software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 9U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19" 9U rackmount chassis that is 16" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies gurantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

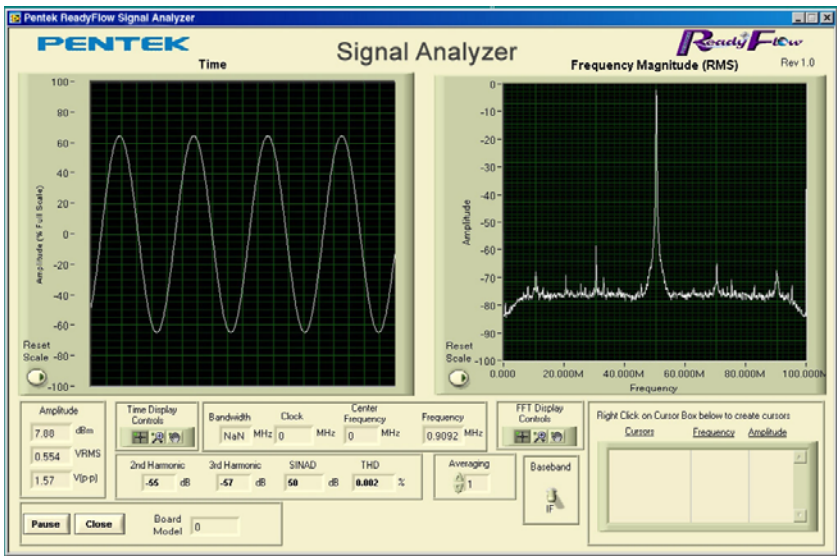
All 8264 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8264 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB
Dimensions: 6U Chassis, 19" W x 16" D x 10.5" H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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RADAR & SDR I/O - FMC

MODEL	DESCRIPTION
5973	Virtex-7 Processor and FMC Carrier - 3U VPX
5983	Kintex UltraScale Processor and FMC Carrier - 3U VPX
7070	Virtex-7 Processor and FMC Carrier - x8 PCIe
3312	4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - FMC
5973-312	FlexorSet: 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
5983-313	FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
7070-312	FlexorSet: 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCIe
3313	4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A w. DDC - FMC
5973-313	FlexorSet: 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
5983-313	FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
7070-313	FlexorSet: 4-Channel 250 MHz 16-bit A/D with DDCs, 2-Channel 800 MHz 16-bit D/A - x8 PCIe
3316	8-Channel 250 MHz, 16-bit A/D - FMC
5973-316	FlexorSet: 8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX
5983-317	FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
7070-316	FlexorSet: 8-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCI
5973-317	FlexorSet: 8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX
7070-317	FlexorSet: 8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe
3320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC
5973-320	FlexorSet: 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - 3U VPX
5983-320	FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
7070-320	FlexorSet: 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - x8 PCIe
3324	4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - FMC
5973-324	FlexorSet: 4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - 3U VPX
5983-324	FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
7070-324	FlexorSet: 4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - x8 PCIe
8266	PC Development System for PCIe Cobalt, Onyx and Flexor Boards
8267	3U VPX Development System for Cobalt, Onyx and Flexor Boards
3324-990	Reference Design for the Xilinx VC707 Evaluation Kit
	Customer Information

RADAR & SDR I/O - PMC/XMC
RADAR & SDR I/O - CompactPCI
RADAR & SDR I/O - x8 PCI Express
RADAR & SDR I/O - 3U VPX - FORMAT 1
RADAR & SDR I/O - AMC
RADAR & SDR I/O - 3U VPX - FORMAT 2
RADAR & SDR I/O - 6U VPX

Click Here for the PRODUCT SELECTOR

Last updated: April 2018

New!

Model 5973

3U OpenVPX Virtex-7 Processor and FMC Carrier

FlexOr
GateXpress
GateFlow
ReadyFlow
Board Support Package

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions That Include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

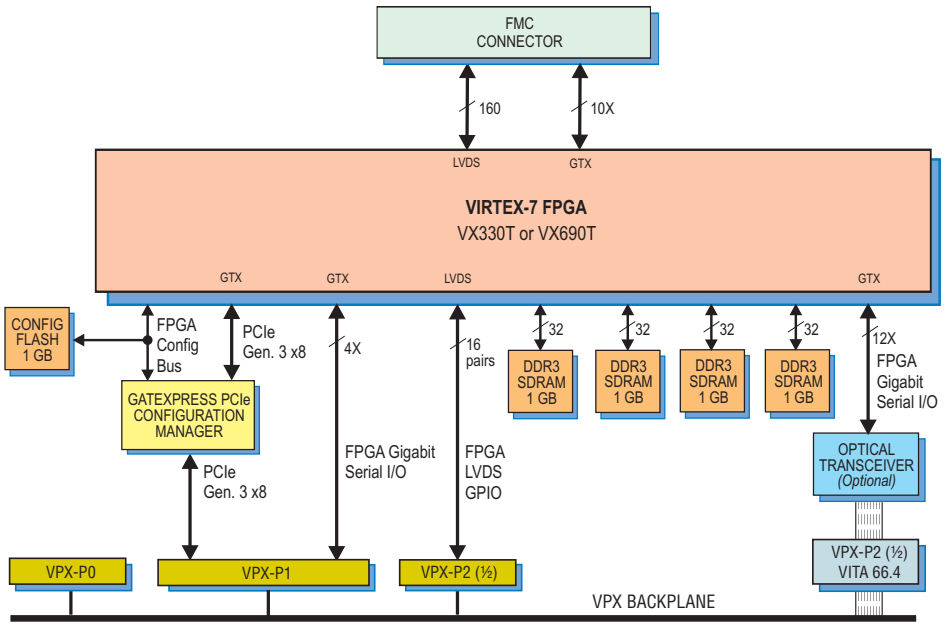
When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked- list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 5973

3U OpenVPX Virtex-7 Processor and FMC Carrier

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

FMC Product Combinations

If you wish to purchase this FMC Carrier in combination with an A/D FMC module, please see:

- FlexorSet Model 5973-312
- FlexorSet Model 5973-313
- FlexorSet Model 5973-316
- FlexorSet Model 5973-317
- FlexorSet Model 5973-320
- FlexorSet Model 5973-324

Ordering Information

Model	Description
5973	3U OpenVPX Virtex-7 Processor and FMC Carrier
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

Xilinx Virtex-7 FPGA

The 5973 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5973 supports the emerging VITA-66.4 standard, that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The 5973 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Specifications

I/O Module Interface: VITA-57.1, High Pin Count FMC site

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 5983

3U OpenVPX Kintex UltraScale Processor and FMC Carrier

JADEFX

FLEXOR

NAVIGATOR Design Suite

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGAs
- 9 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Kintex UltraScale FPGA for custom I/O
- Optional optical Interface for backplane gigabit serial interboard communication
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

The JadeFX™ Model 5983 is a high-performance 3U OpenVPX board based on the Xilinx Kintex UltraScale FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5983 includes a VITA-57.4 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface Flexor® FMCs to create a FlexorSet, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Jade family of Kintex UltraScale products, the JadeFX 5983 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

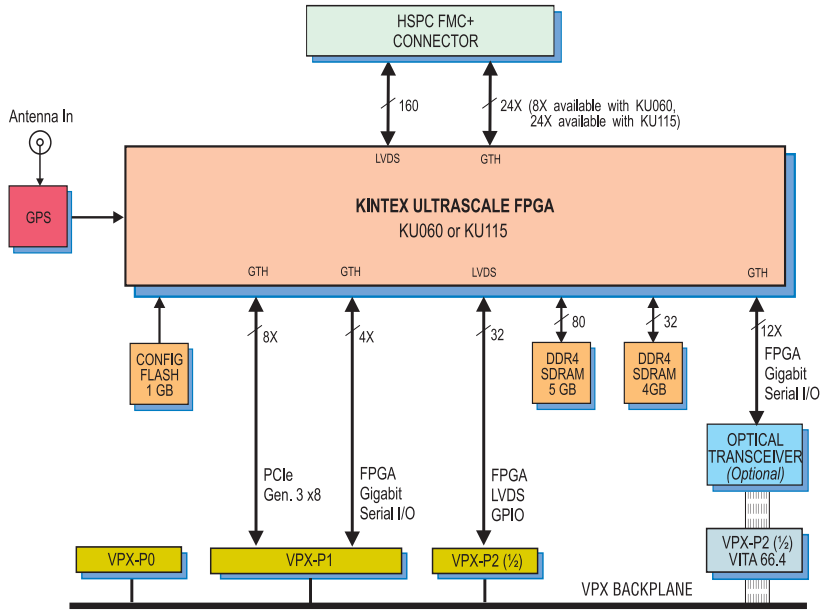
When integrated with a Pentek FMC, the 5983 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform generation engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked- list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel timing and sample-count information.

IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 5983

3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx, OnyxFx and JadeFX 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

FlexorSet Product Combinations

If you wish to purchase this FMC Carrier in combination with an FMC module, please see:

- FlexorSet Model 5983-313
- FlexorSet Model 5983-317
- FlexorSet Model 5983-320
- FlexorSet Model 5983-324

Ordering Information

Model	Description
5983	3U OpenVPX Kintex UltraScale Processor and FMC Carrier
Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5983 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

I/O Module Interface: VITA-57.4, High Serial Pin-Count FMC site

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU060-2
- **Optional:** Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- **Serial :** 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR4 SDRAM
- **Size:** Two banks, one 4 GB and one 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

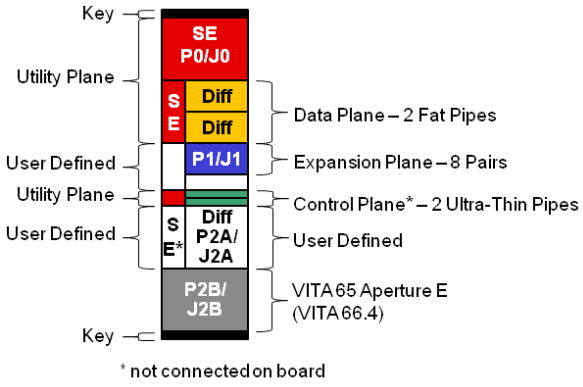
PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983 is compatibile with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1



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New!

Model 7070

PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

Model 7070 shown with Model 3312 multichannel A/D & D/A FMC module

FlexOr

GateXpress

GateFlow

ReadyFlow Board Support Package

General Information

The Flexor® Model 7070 is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 retains all of the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC module, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample-count information.

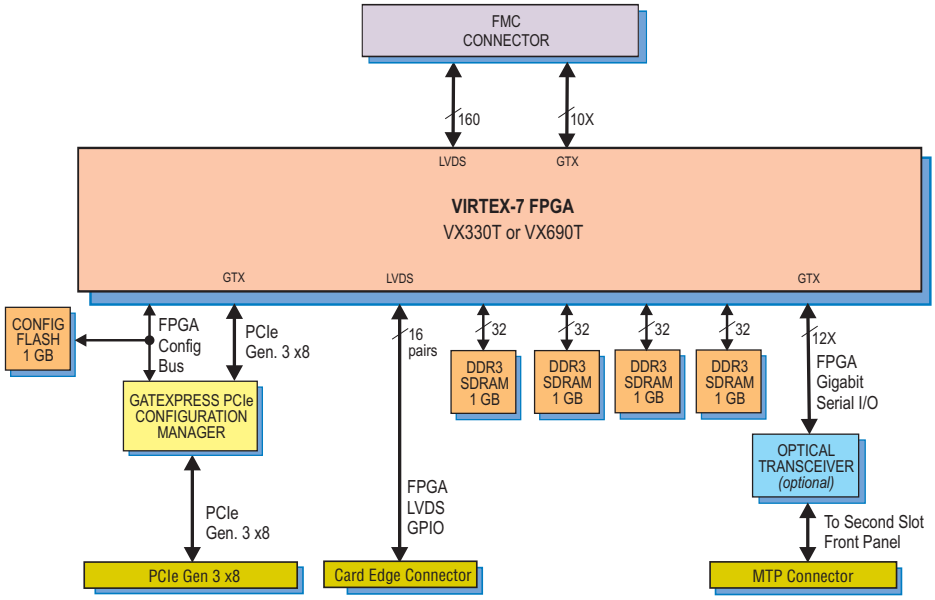
IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070 and installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- Optional user-configurable 12X optical gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Commercial and extended-temperature versions available



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

Model 7070

PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

FMC Product Combinations

If you wish to purchase this FMC Carrier in combination with an A/D FMC module, please see:

- FlexorSet Model 7070-312
- FlexorSet Model 7070-313
- FlexorSet Model 7070-316
- FlexorSet Model 7070-317
- FlexorSet Model 7070-320
- FlexorSet Model 7070-324

Ordering Information

Model	Description
7070	PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	16 pairs LVDS FPGA I/O
-110	12x gigabit serial optical I/O

Contact Pentek for availability of extended-temperature versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

Xilinx Virtex-7 FPGA

The 7070 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and a card edge connector for custom I/O. For applications requiring custom gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on a PCIe slot panel that can be installed in an empty, adjacent PCIe slot.

When configured with a VX330T FPGA, four duplex lanes are available.

GateXpress for FPGA Configuration

The 7070 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Specifications

I/O Module Interface: VITA-57.1, High Pin Count FMC site

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel, Option -104: 16 pairs of LVDS connections between the FPGA and a card-edge connector.

Optical (Option -110): User-configurable 12X (VX690T) or 4X (VX 330T) optical gigabit serial interface, MTP connector installed in an empty adjacent slot

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air cooled,

Size: Half-length PCIe card

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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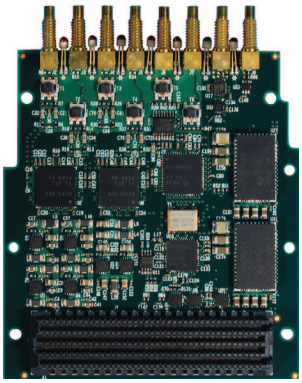
New!

Model 3312

4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A - FMC



FlexorSet

ReadyFlow Board Support Package

GateFlow

NAVIGATOR Design Suite

Features

- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3312 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform generator IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate- driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

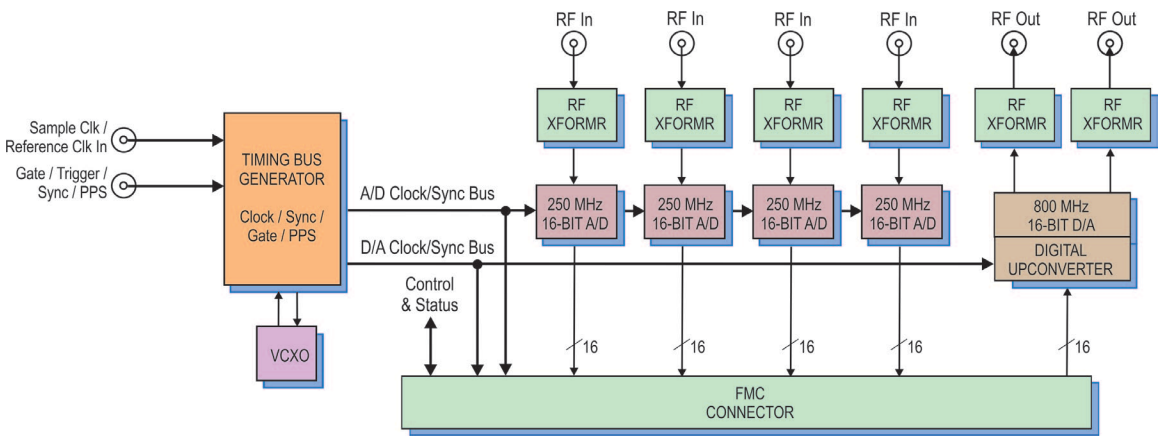
For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's task of identifying and executing on the data.

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3312's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

D/A Waveform Generator IP Module

With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easilyrecord to the D/As wave-forms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. ➤



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FMC Interface

The Model 3312 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

SPARK Development Systems

SPARK systems are fully-integrated saving engineers and system integrators the time and expense associated with building and testing a development system. SPARK systems ensure the optimum performance of Pentek boards and are available in 3U VPX **(Model 8267)** and in a PC environment **(Model 8266)**.

SPARK Development Systems

Ordering Information

Model	Description
3312	4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A FMC module
Options:	
3312-990	Reference design for 3312 installed on Xilinx VC707 Evaluation Kit
3U FlexorSet Description	
5973-312	4-Channel 250 MHz A/D with Virtex-7 FPGA
5973-313	4-Channel 250 MHz A/D, Virtex-7 FPGA with 4 multiband DDCs and interpolator
5983-313	4-Channel 250 MHz A/D, Kintex UltraScale FPGA with 4 multiband DDCs and interpolator
PCIe FlexorSet Description	
7070-312	4-Channel 250 MHz A/D with Virtex-7 FPGA -x8
7070-313	4 Channel 250 MHz A/D, Virtex-7 FPGA with 4 DDCs and interpolator -x8

Contact Pentek for availability of rugged and conduction-cooled versions and other support options

➤Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

Board Support Packages

Pentek's BSPs provide control of the 3312's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a powerful, quick-start platform to create custom applications. BSPs are compatible with Windows and Linux operating systems. ReadyFlow BSP is used with OnyxFX Virtex-7 FPGA carriers and Navigator BSP is used for all new development going forward including the JadeFX Kintex Ultrascale carriers.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the development kit to completely replace the Pentek IP with their own.

GateFlow is used with OnyxFX Virtex-7 FPGA carriers and Navigator FDK is used for all new FPGA development going forward including the JadeFX Kintex UltraScale carriers.

Model 3312 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
- **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin- Count FMC

➤

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Pentek FlexorSet Models

Form Factor	FPGA Type Development Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				5973-313	As above with 4 multiband DDCs & interpolation filters
			3316	5973-316	8 Ch 250 MHz 16-bit A/D
				5973-317	As above with 8 multiband DDCs
			3320	5973-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5973-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
	Kintex UltraScale Navigator BSP Navigator FDK Vivado	5983	3312	5983-313	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317	8 Ch 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5983-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
PCIe	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				7070-313	As above with 4 multiband DDCs & interpolation filters
			3316	7070-316	8 Ch 250 MHz 16-bit A/D
				7070-317	As above with 8 multiband DDCs
			3320	7070-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	7070-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A

New!

FlexorSet Model 5973-312

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A with DUC - 3U VPX

Model 5973-312

OnyxFX
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Includes Xilinx Virtex-7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973 is a member of the OnyxFX© family of high-performance 3U VPX baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5973-312 FlexorSet™ combines the Model 5973 and the Model 3312 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz 16-bit A/Ds, one digital upconverter, two 800 MHz 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-312 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP for DDR3 SDRAM memories.

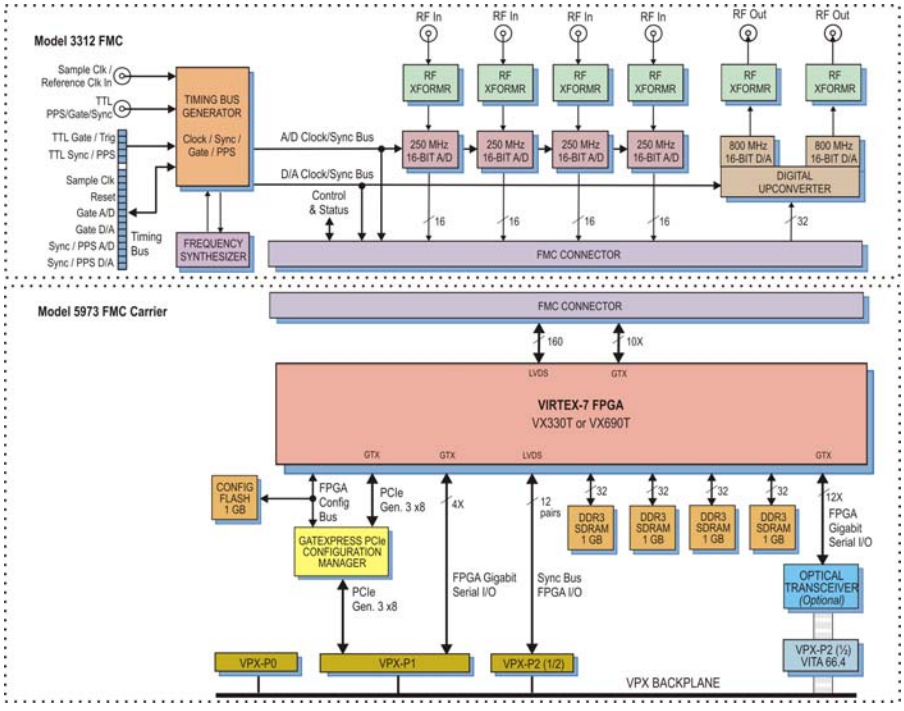
The 5973-312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤



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4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A with DUC - 3U VPX

A/D Acquisition IP Modules

The 5973-312 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5973-312 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Virtex-7 FPGA

The 5973-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols. Sixteen pairs of LVDS connections between the FPGA and the VPX P2 connector for synchronization and custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

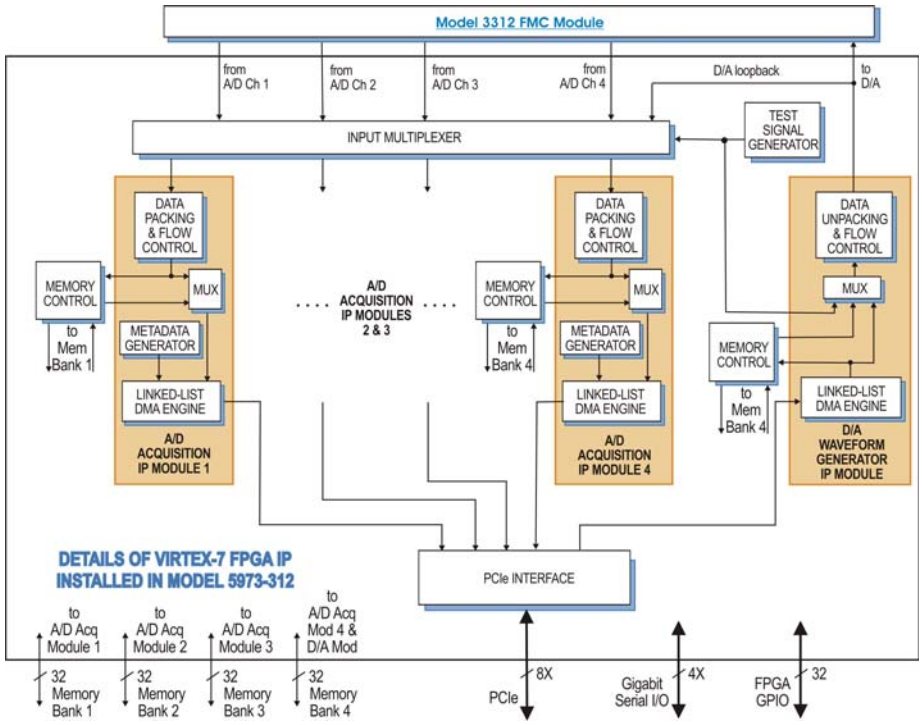
The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. ➤



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FlexorSet Model 5973-312

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A with DUC - 3U VPX

PCI Express Interface

The Model 5973-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5973-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
5973-312	4-Channel 250 MHz A/D, 2-Channel 800 MHz 16-bit D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

➤ In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for synchronization custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

FlexorSet Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

Model 5983-313

FlexOr

JADEFX

NAVIGATOR Design Suite

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-313 FlexorSet™ combines the Model 5983 and the Model 3313 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-313 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a powerful DDC core.

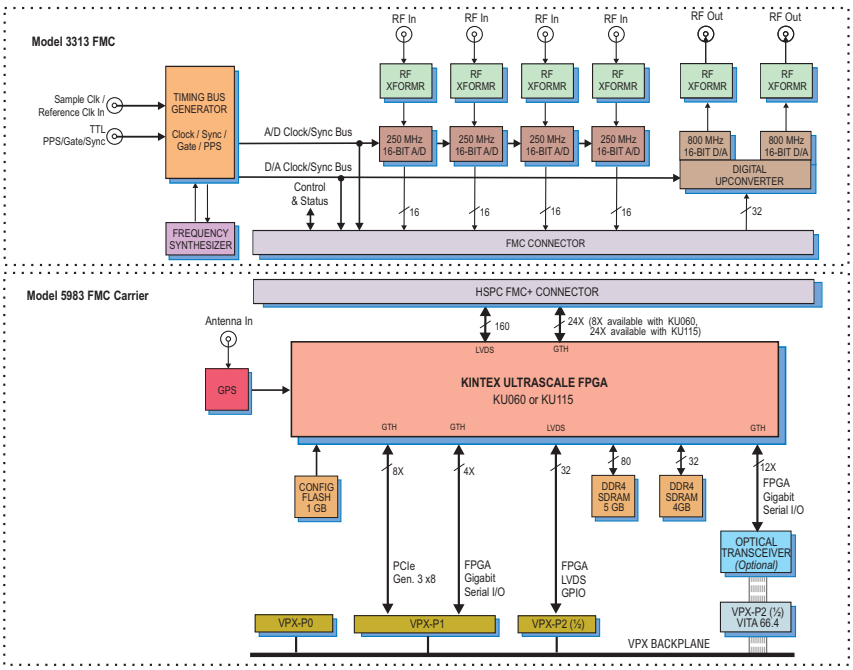
The 5983-313 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

FlexorSet
Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

A/D Acquisition IP Modules

The 5983-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5983-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

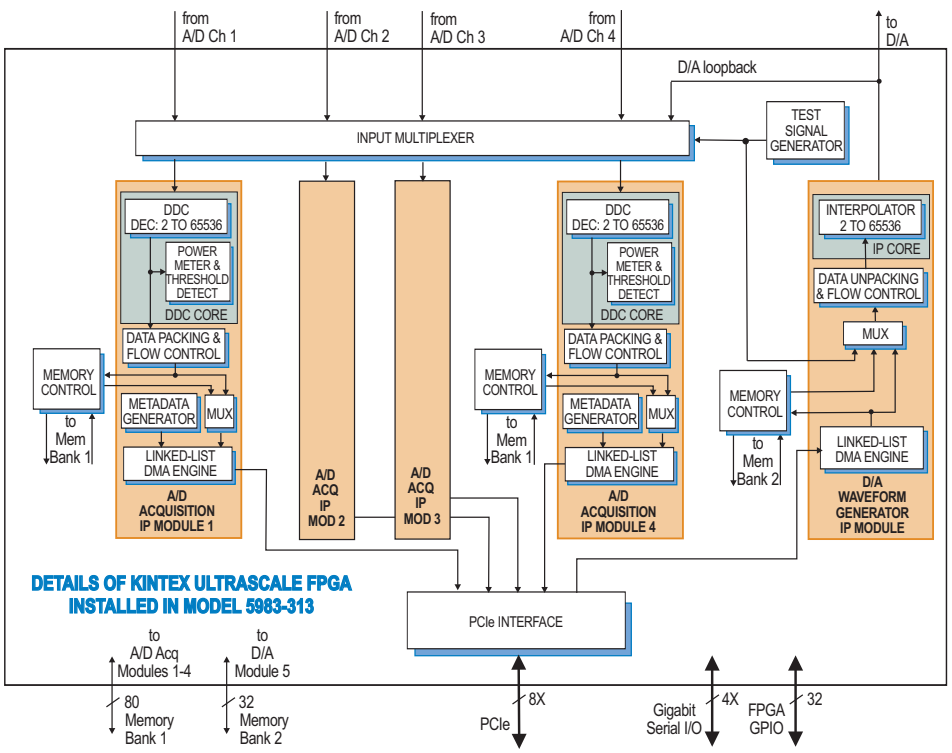
In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983-313 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

➤ The 5983-313 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

PCI Express Interface

The Model 5983-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

4-Channel Digital Downconverter

Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit user-programmable coefficients, 24-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution ➤

FlexorSet Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5983-313	4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpo-lation and Kintex Ultra- Scale FPGA - 3U VPX

Options:

-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Specifications, Continued

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range
- D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU060-2
- **Optional:** Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- **Serial:** 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR4 SDRAM
- **Size:** Two banks, one 4 GB and one 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

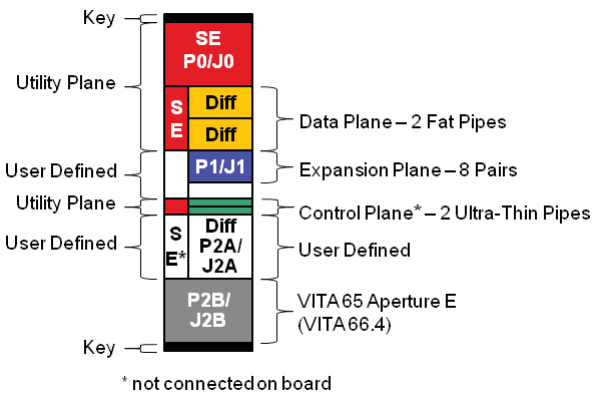
PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1



* not connected on board

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New!

FlexorSet Model 7070-312

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A - x8 PCIe

Model 7070-312

General Information

Model 7070-312 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-312 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

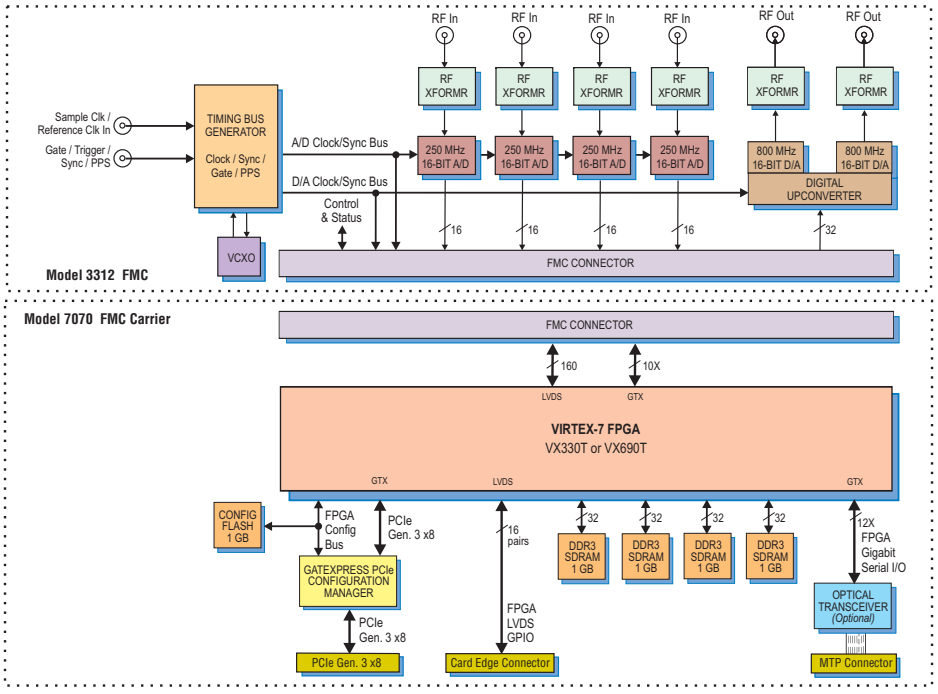
A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A - x8 PCIe

A/D Acquisition IP Modules

The 7070-312 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The 7070-312 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Virtex-7 FPGA

The 7070-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPoptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

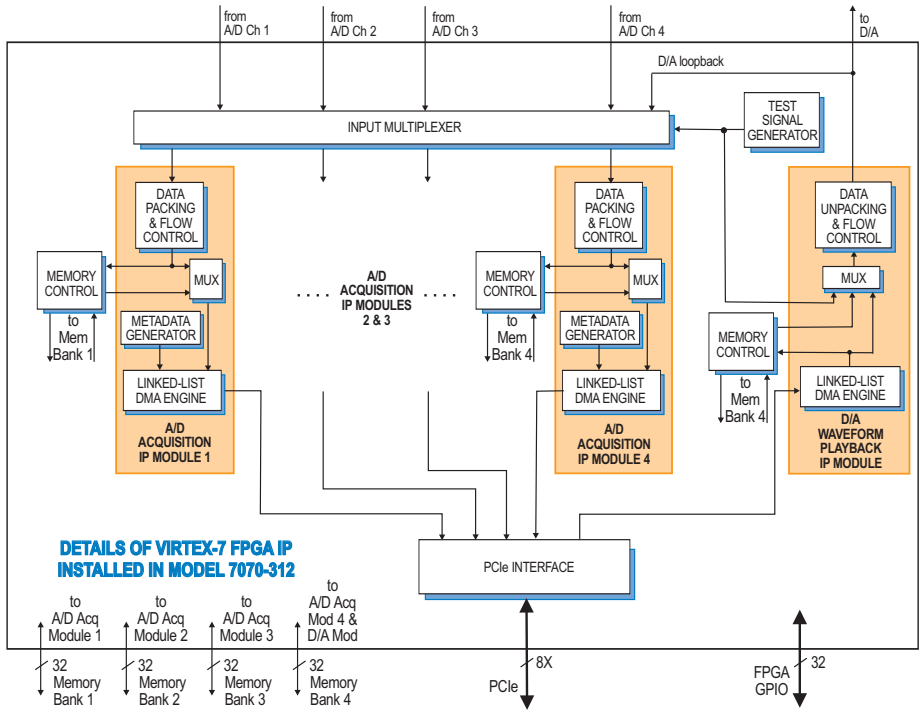
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the ➤



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FlexorSet Model 7070-312

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A - x8 PCIe

PCI Express Interface

The Model 7070-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 7070-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
7070-312	4-Channel 250 MHz A/D, 2-Channel 800 MHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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New!

Model 3312

4-Ch. 250 MHz, 16-bit A/D with DDCs, 2-Ch. 800 MHz, 16-bit D/A with DUC and Extended Interpolation - FMC

FlexorReady Flow Board Support PackageGate Flow

Features

- Sold as the:
  - FlexorSet Model 5973-313
  - FlexorSet Model 7070-313
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U VPX or Model 7070 PCIe Virtex-7 FMC carriers
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3312 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-313 3U VPX or the FlexorSet 7070-313 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loop-back mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

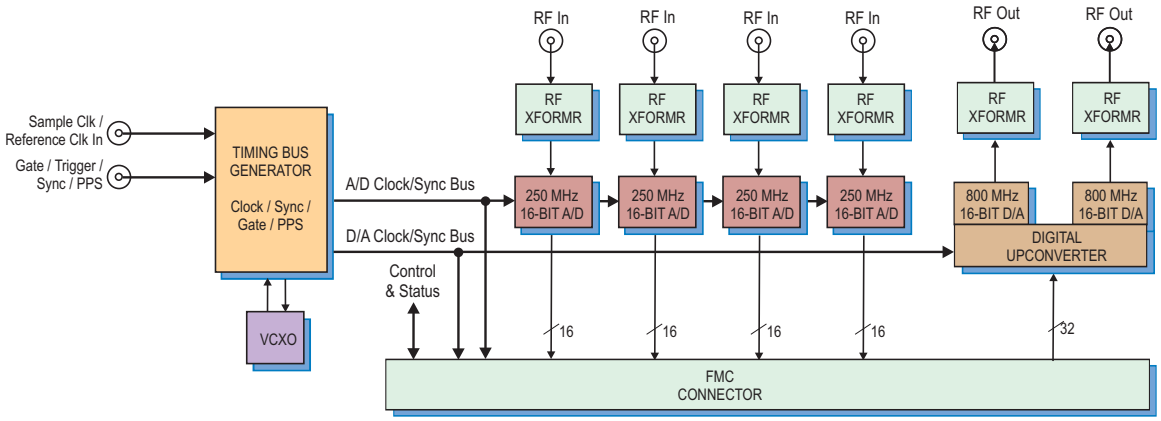
These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's task of identifying and executing on the data.

D/A Waveform Playback IP Module

With the 5973 or the 7070 carrier, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming. ➤



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New!

Model 3312

4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A with DUC - FMC

FlexorReady Flow Board Support PackageGate Flow

Features

- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carriers as FlexorSets
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

The 3312 is available as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-312 3U VPX or the FlexorSet 7070-312 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support for the 3312 when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be best unlocked when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform recorder IP module.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform generator IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

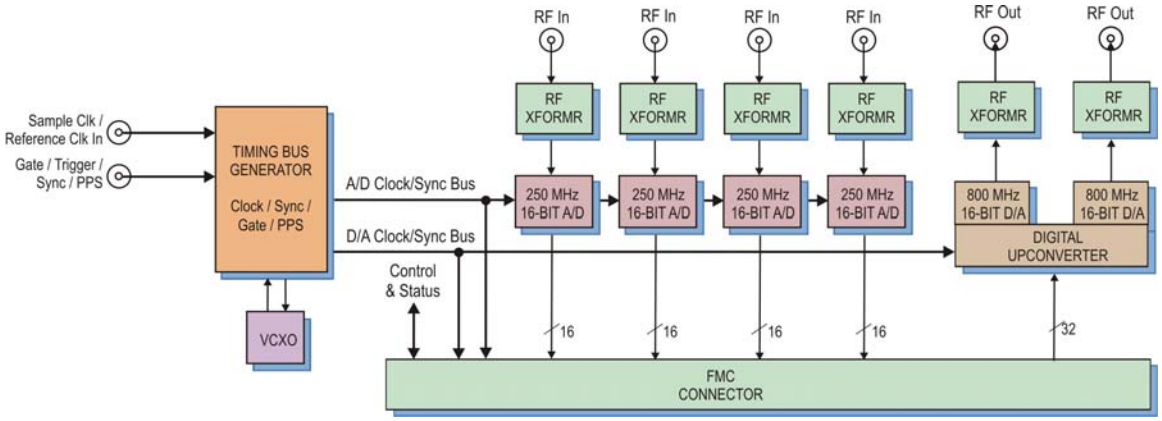
These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's task of identifying and executing on the data.

D/A Waveform Generator IP Module

With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from generator trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 3312

4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A with DUC - FMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
3312	4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A with DUC - FMC module
Options:	
3312-990	Reference design for 3312 installed on Xilinx VC707 Evaluation Kit
FlexorSet	**Description**
5973-312	3U VPX FlexorSet for 3312
5973-313	3U VPX FlexorSet for 3312 with DDCs and interpolator
7070-312	PCIe FlexorSet for 3312
7070-313	PCIe FlexorSet for 3312 with DUCs and interpolator

Contact Pentek for availability of rugged and conduction-cooled versions and other support options

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3312's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3312 or 7070/3312 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3312 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

Model 3312 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
- **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC

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New!

FlexorSet Model 5973-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

Model 5973-313

OnyxFX
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Includes Xilinx Virtex-7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973 is a member of the OnyxFX© family of high-performance 3U VPX baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5973-313 FlexorSet™ combines the Model 5973 and the Model 3312 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The Model 5973-313 includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-313 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful DDC core.

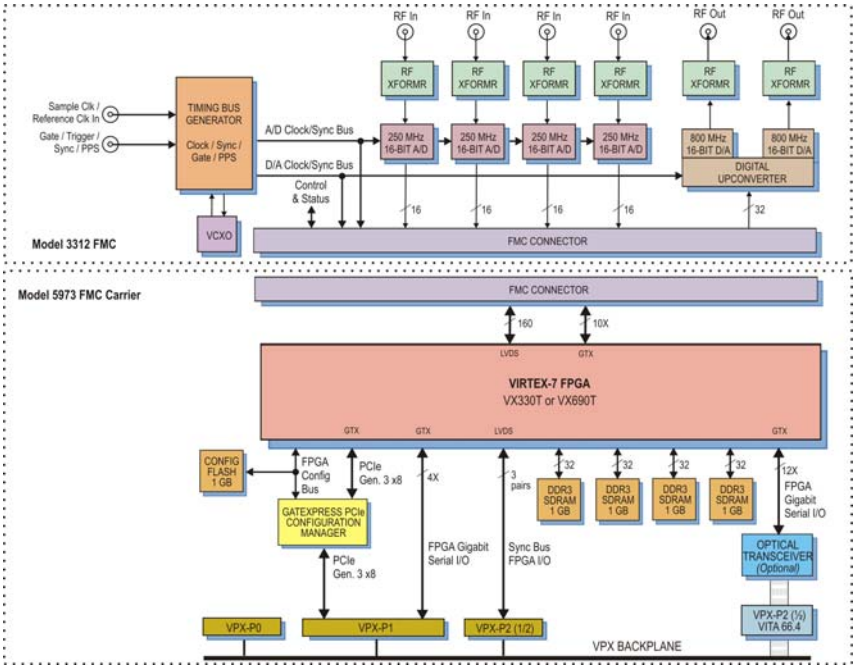
The 5973-313 features a sophisticated D/A waveform recorder IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤



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FlexorSet Model 5973-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

A/D Acquisition IP Modules

The 5973-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5973-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

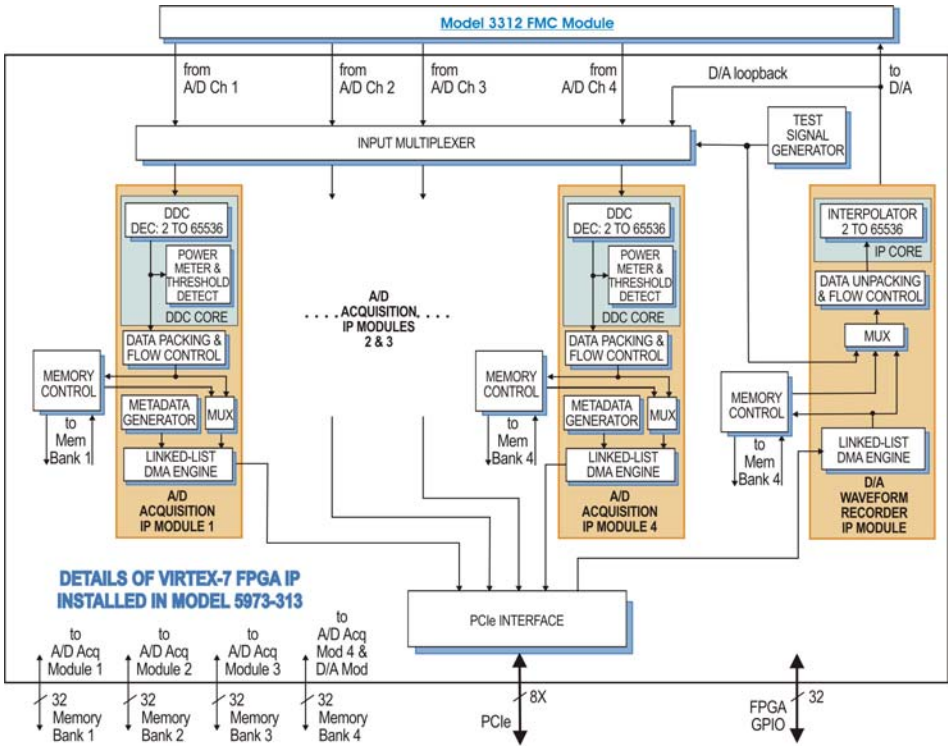
➤ Xilinx Virtex-7 FPGA

The 5973-313 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface. ➤



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4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

➤ GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules. ➤

FlexorSet Model 5973-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model	Description
5973-313	4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpolation and Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical I/O with XC7VX690T FPGA, 4X w. XC7VX330T

Contact Pentek for availability of rugged and conduction-cooled versions

➤ PCI Express Interface

The Model 5973-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5973-313 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

4-Channel Digital Downconverter
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_S
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit user-programmable coefficients, 24-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range
- D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

FlexorSet Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

Model 5983-313

FlexOr

JADEFX

NAVIGATOR Design Suite

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-313 FlexorSet™ combines the Model 5983 and the Model 3313 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-313 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a powerful DDC core.

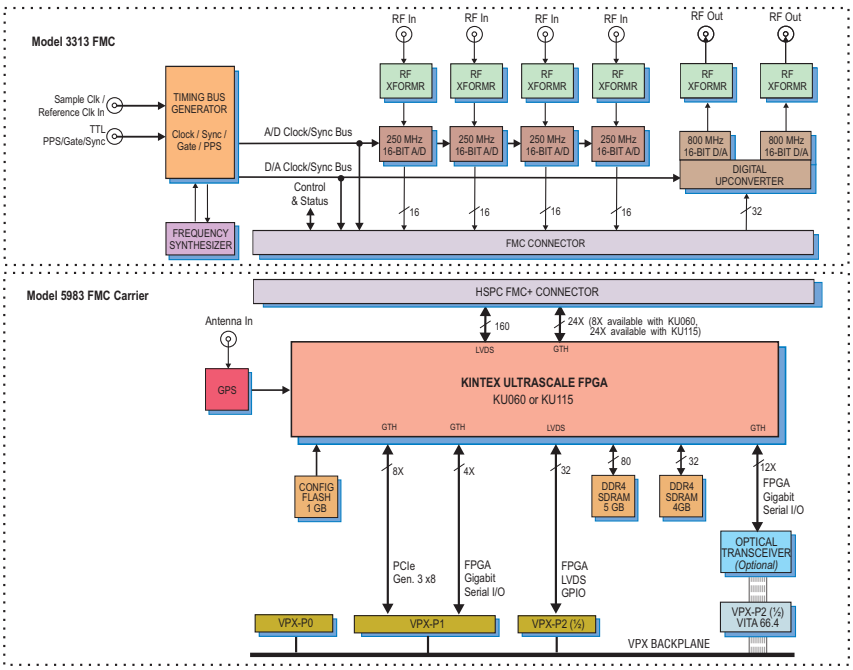
The 5983-313 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

FlexorSet
Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

A/D Acquisition IP Modules

The 5983-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5983-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

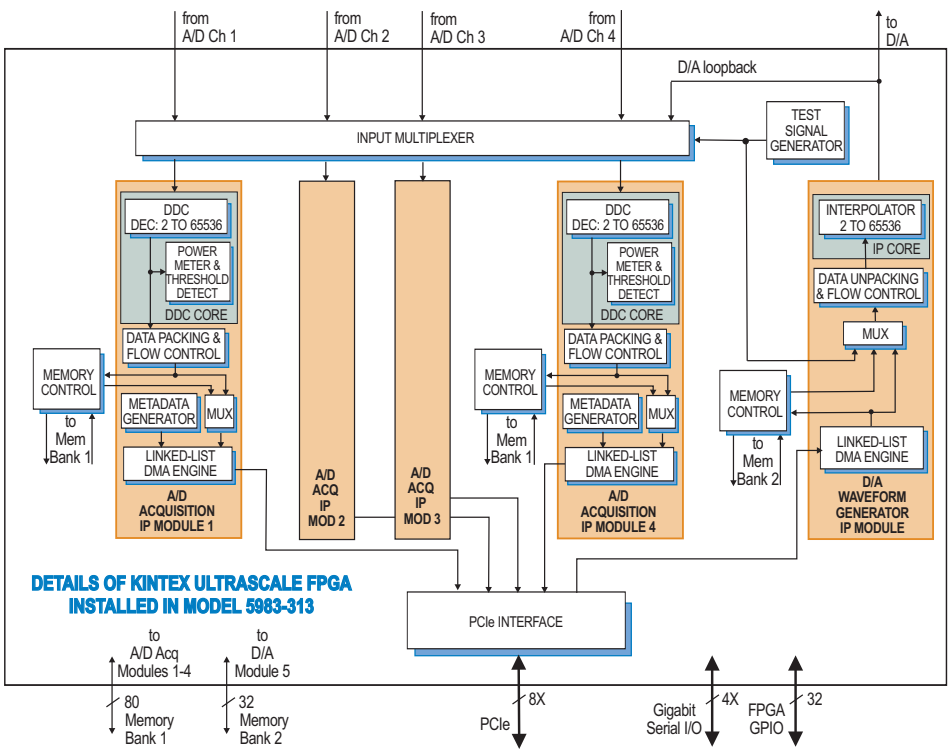
In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983-313 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

➤ The 5983-313 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

PCI Express Interface

The Model 5983-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

4-Channel Digital Downconverter

Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit user-programmable coefficients, 24-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution ➤

New!

FlexorSet Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

Model 7070-313

FlexorGateXpressGateFlowReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 7070-313 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The Model 7070-313 includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-313 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful DDC core.

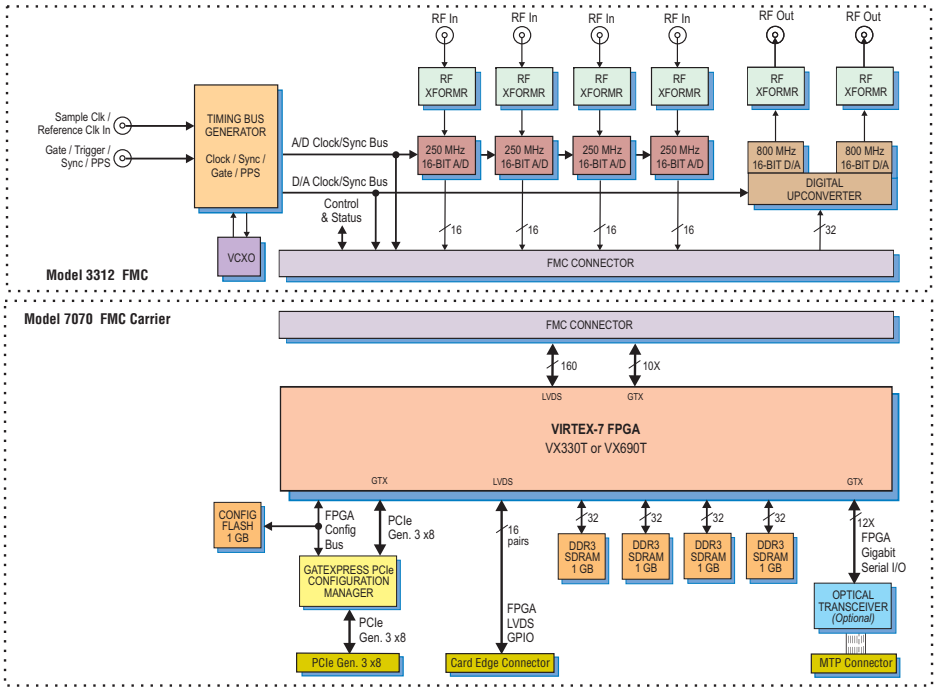
The 7070-313 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

A/D Acquisition IP Modules

The 7070-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The 7070-313 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

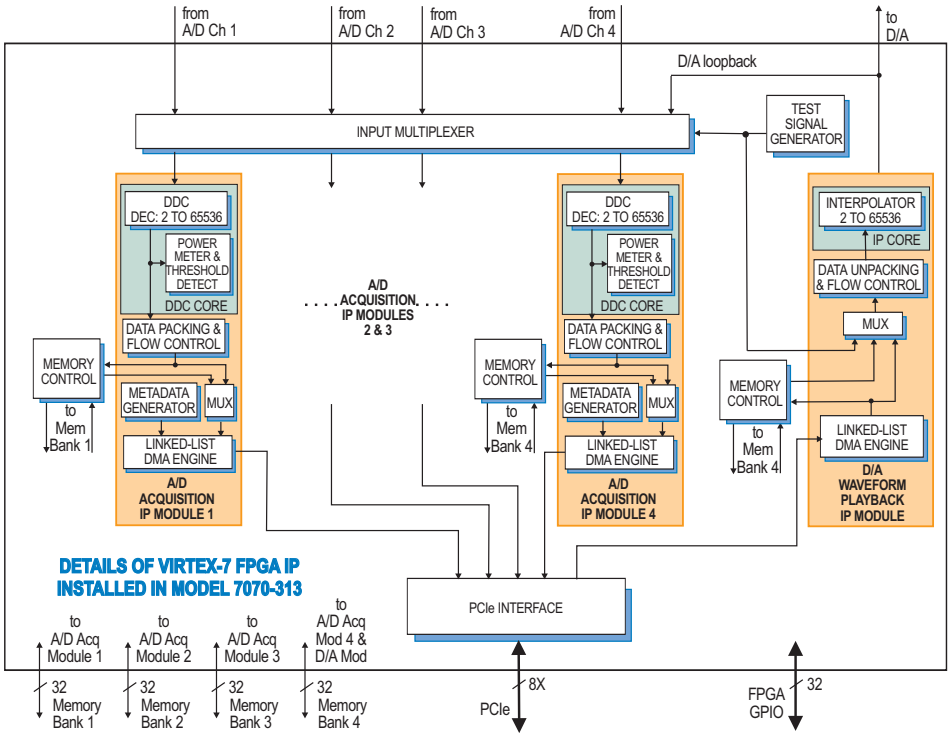
In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ Xilinx Virtex-7 FPGA

The 7070-313 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

➤ GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules. ➤

FlexorSet Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
5973-313	4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpolation and Virtex-7 FPGA -x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O between the FPGA and a card-edge connector for custom I/O
-110	VITA-66.4 12X optical I/O with XC7VX690T FPGA, 4X w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ PCI Express Interface

The Model 7070-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 7070-313 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

4-Channel Digital Downconverter
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_S
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit user-programmable coefficients, 24-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range
- D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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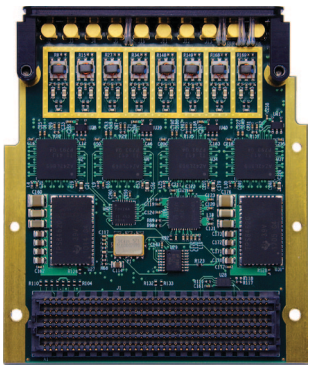
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

Model 3316

8-Channel 250 MHz, 16-bit A/D - FMC



FlexorRT Board Support Package

GateFlow

NAVIGATOR Design Suite

Features

- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 3316 is a multi-channel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3316 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3316

The true performance of the 3316 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

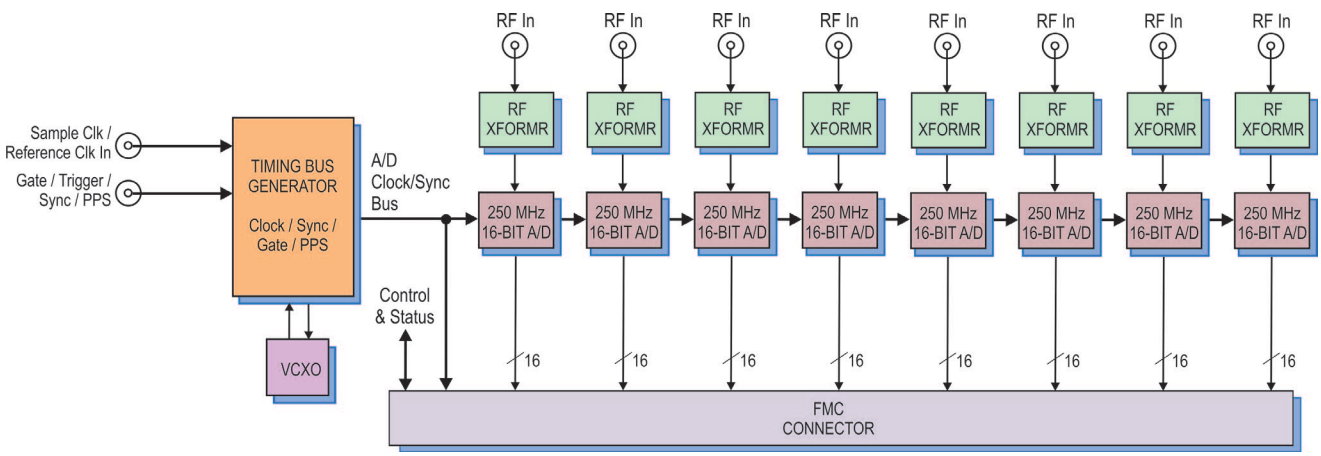
A/D Acquisition IP Modules

With the 3316 installed on a Pentek FMC carrier, the FlexorSet features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's task of identifying and executing on the data. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 3316 — 8-Channel 250 MHz, 16-bit A/D - FMC

SPARK Development Systems

SPARK systems are fully-integrated saving engineers and system integrators the time and expense associated with building and testing a development system. SPARK systems ensure the optimum performance of Pentek boards and are available in 3U VPX **(Model 8267)** and in a PC environment **(Model 8266)**.

Ordering Information

Model	Description
3316	8-Channel 250 MHz 16-bit A/D - FMC module

Options:

3316-990	Reference design for 3316 installed on Xilinx VC707 Evaluation Kit

3U VPX FlexorSet Description

5973-316	8-Channel 250 MHz A/D with Virtex-7 FPGA
5973-317	8-Channel 250 MHz A/D, Virtex-7 FPGA with 8 multiband DDCs and interpolator
5983-317	8-Channel 250 MHz A/D, Kintex UltraScale FPGA with 8 multiband DDCs and interpolator

PCIe FlexorSet Description

7070-316	8-Channel 250 MHz A/D with Virtex-7 FPGA- x8
7070-317	8-Channel 250 MHz A/D, Virtex-7 FPGA with 8 multiband DDCs and interpolator -x8

Contact Pentek for availability of rugged and conduction-cooled versions and other support options

➤ When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3316's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

Board Support Packages

Pentek's BSPs provide control of all the 3316's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a powerful, quick-start platform to create custom applications. BSPs are compatible with Windows and Linux operating systems. ReadyFlow BSP is used with OnyxFX Virtex-7 FPGA carriers and Navigator BSP is used for all new development going forward including the JadeFX Kintex Ultrascale carriers.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the development kit to completely replace the Pentek IP with their own.

GateFlow is used with OnyxFX Virtex-7 FPGA carriers and Navigator FDK is used for all new FPGA development going forward including the JadeFX Kintex UltraScale carriers.

FMC Interface

The Model 3316 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3316 and the FMC carrier.

Model 3316 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin- Count FMC

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Pentek FlexorSet Models

Form Factor	FPGA Type Development Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				5973-313	As above with 4 multiband DDCs & interpolation filters
			3316	5973-316	8 Ch 250 MHz 16-bit A/D
				5973-317	As above with 8 multiband DDCs
			3320	5973-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5973-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
	Kintex UltraScale Navigator BSP Navigator FDK Vivado	5983	3312	5983-313	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317	8 Ch 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5983-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
PCIe	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				7070-313	As above with 4 multiband DDCs & interpolation filters
			3316	7070-316	8 Ch 250 MHz 16-bit A/D
				7070-317	As above with 8 multiband DDCs
			3320	7070-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	7070-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A

New!

FlexorSet Model 5973-316

8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

Model 5973-316

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-316 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-316 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-316 to operate as a turnkey solution without the need to develop any FPGA IP.

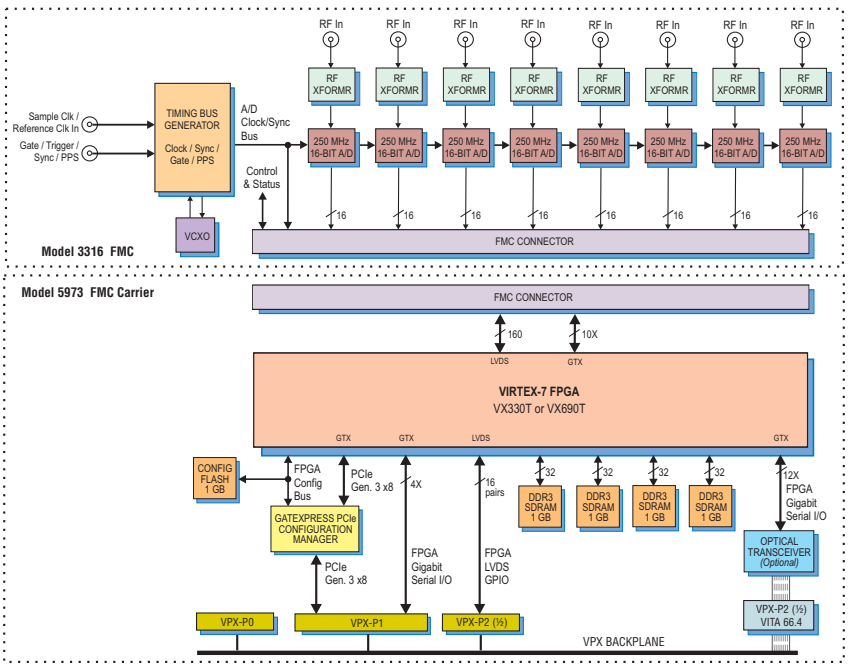
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

➤ Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

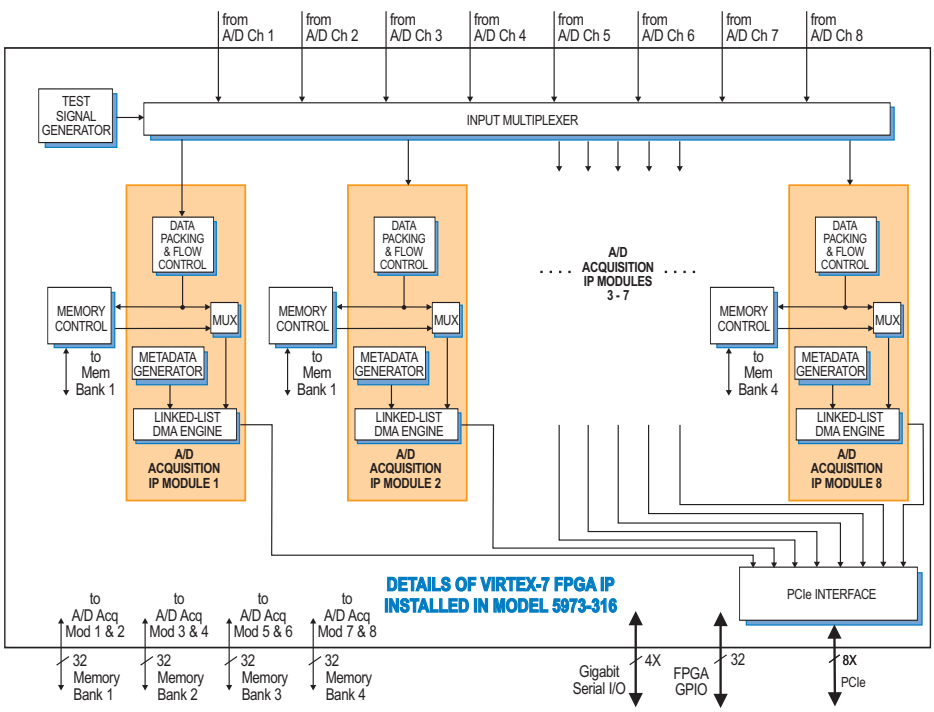
The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. ➤

A/D Acquisition IP Modules

The 5973-316 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

FlexorSet Model 5973-316

8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
5973-316	8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ Memory Resources

The 5973-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 5973-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

FlexorSet Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

Model 5983-317

FlexorSet

JADEFX

NAVIGATOR Design Suite

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB and 5 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

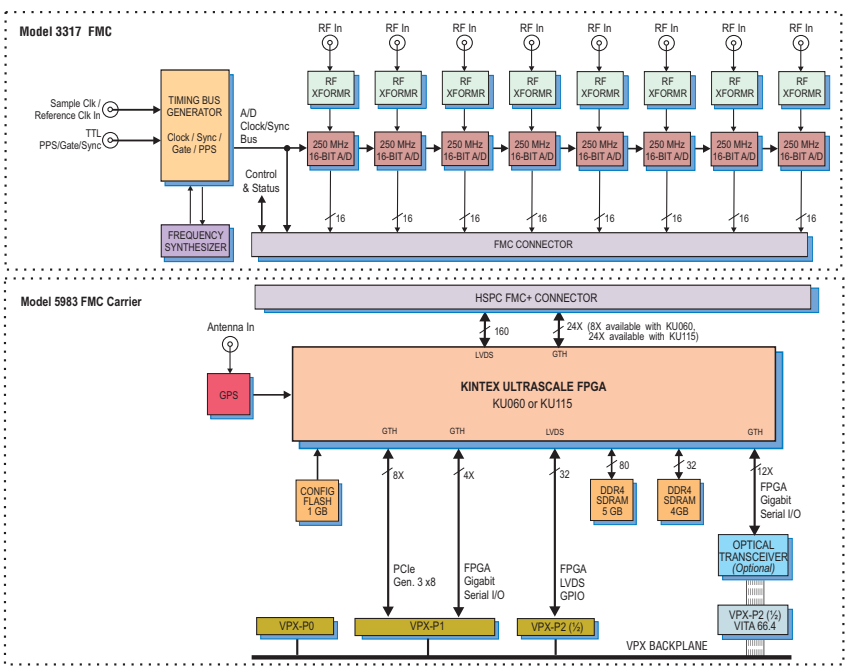
When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface. ➤



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8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

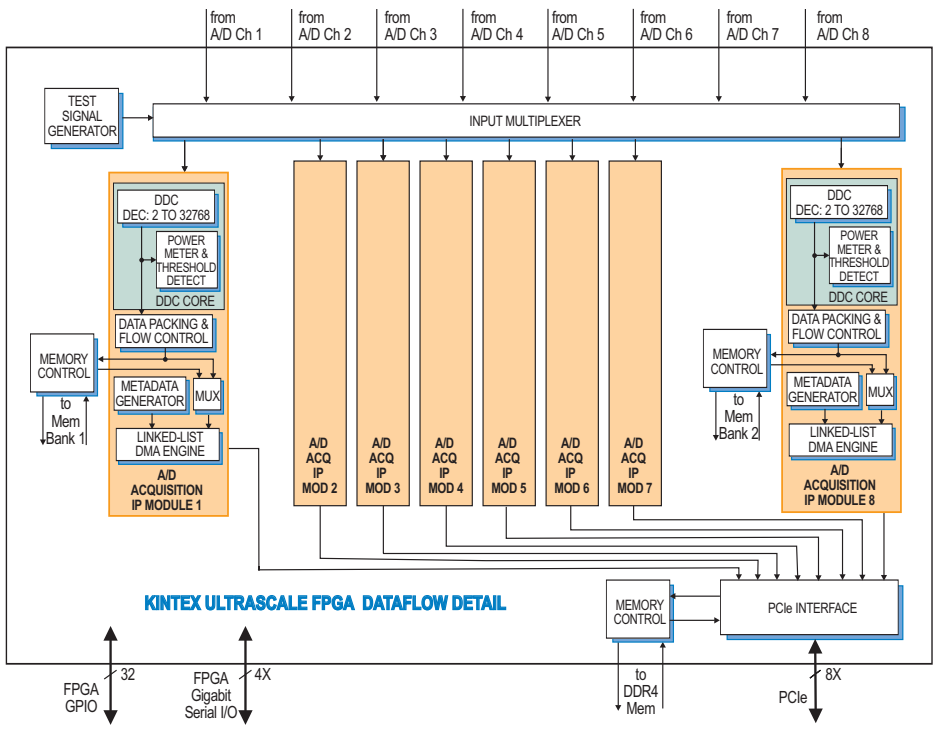
A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Memory Resources

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported. ➤



FlexorSet Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5983-317	8-Channel 250 MHz A/D with DDCs and Kintex Ultra Scale FPGA - 3U VPX
Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

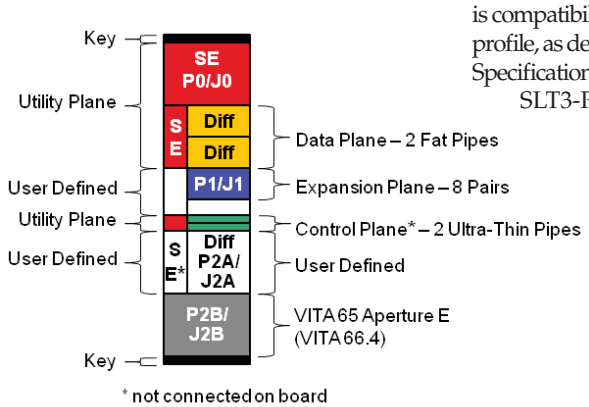
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock



External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU060-2
- **Optional:** Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- **Serial:** 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR4 SDRAM
- **Size:** Two banks, one 4 GB and one 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatibile with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1

New!

FlexorSet Model 7070-316

8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe

Model 7070-316

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 7070-316 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-316 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

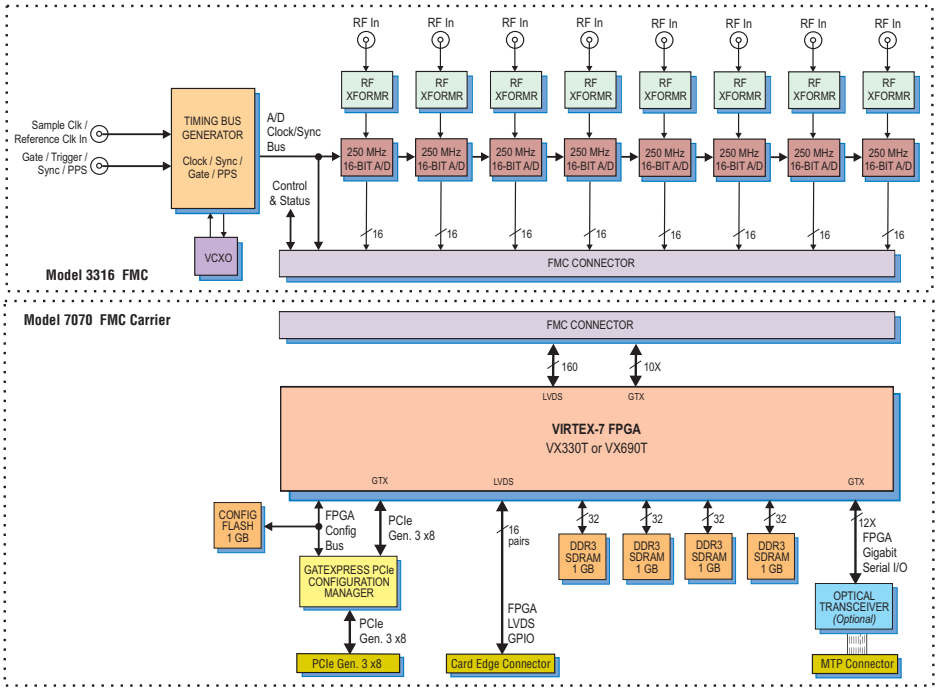
Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed. ➤



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8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe

➤ Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPoptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

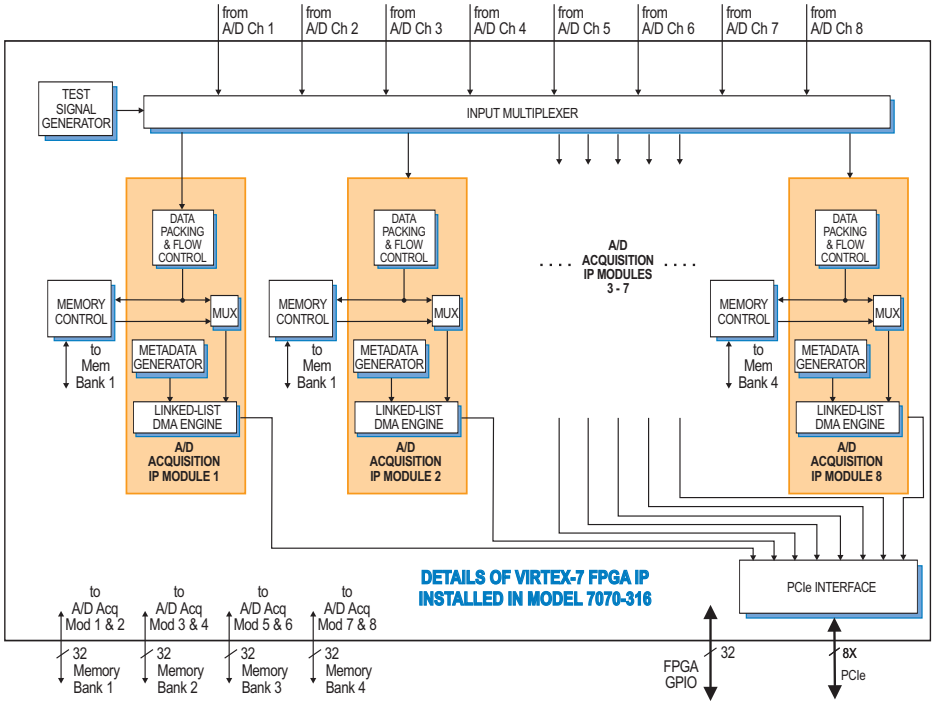
The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. ➤

A/D Acquisition IP Modules

The 7070-316 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



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FlexorSet Model 7070-316

8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
7070-316	8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Memory Resources

The 7070-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 7070-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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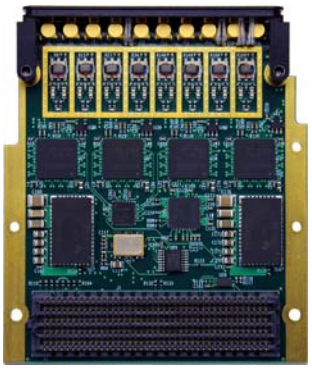
New!

Model 3317

8-Channel 250 MHz, 16-bit A/D with DDCs - FMC



FlexorReady Flow Board Support PackageGate Flow

Features

- Sold as the:
  - FlexorSet Model 5973-317
  - FlexorSet Model 7070-317
- Eight 250 MHz, 16-bit A/Ds
- Eight multiband DDCs
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U VPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available

General Information

The Flexor® Model 3317 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

The 3317 is sold as a complete turnkey data acquisition solution as the FlexorSet™ 5973-317 3U VPX or the FlexorSet 7070-317 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

The 3317 is identical to the 3316 but with different FPGA functionality since it includes DDCs (digital downconverters) when attached to a 5973 or a 7070 FMC carrier.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3317

The true performance of the 3317 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable DDCs, programmable linked-list DMA engines, and a metadata packet creator.

A/D Acquisition IP Modules

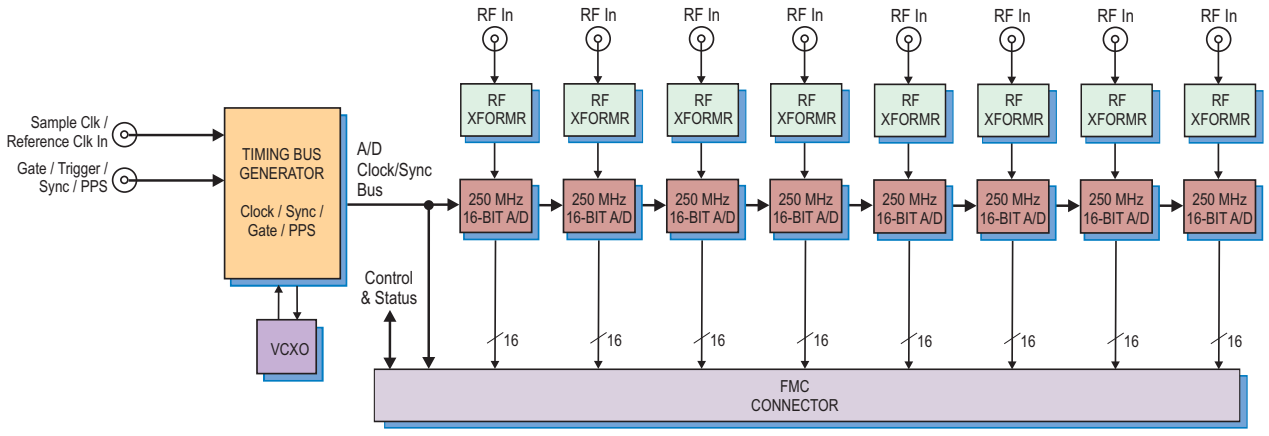
With the 3317 installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's task of identifying and executing on the data.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the FlexorSet to operate as a turnkey solution without the need to develop any FPGA IP. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 3317 — 8-Channel 250 MHz, 16-bit A/D with DDCs - FMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5973-317	8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX
Options:	
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

8267	VPX Development System See 8267 Datasheet for Options

7070-317	8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - x8 PCIe
Options:	
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

8266	PC Development System See 8266 Datasheet for Options

➤ Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized to create larger multiboard systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3317's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973-317 (3U VPX) or 7070-317 (x8 PCIe) IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973-317/7070-317 IP with their own.

FMC Interface

The Model 3317 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3317 and the FMC carrier.

Model 3317 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC

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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

New!

FlexorSet Model 5973-317

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Model 5973-317

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-317 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 5973-317 includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

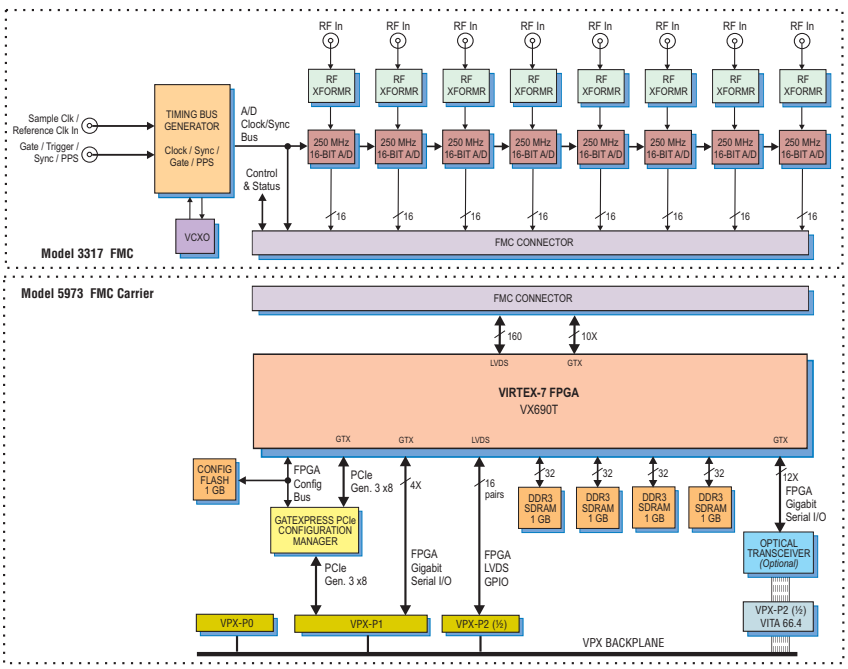
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

➤ Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.

A/D Acquisition IP Modules

The 5973-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

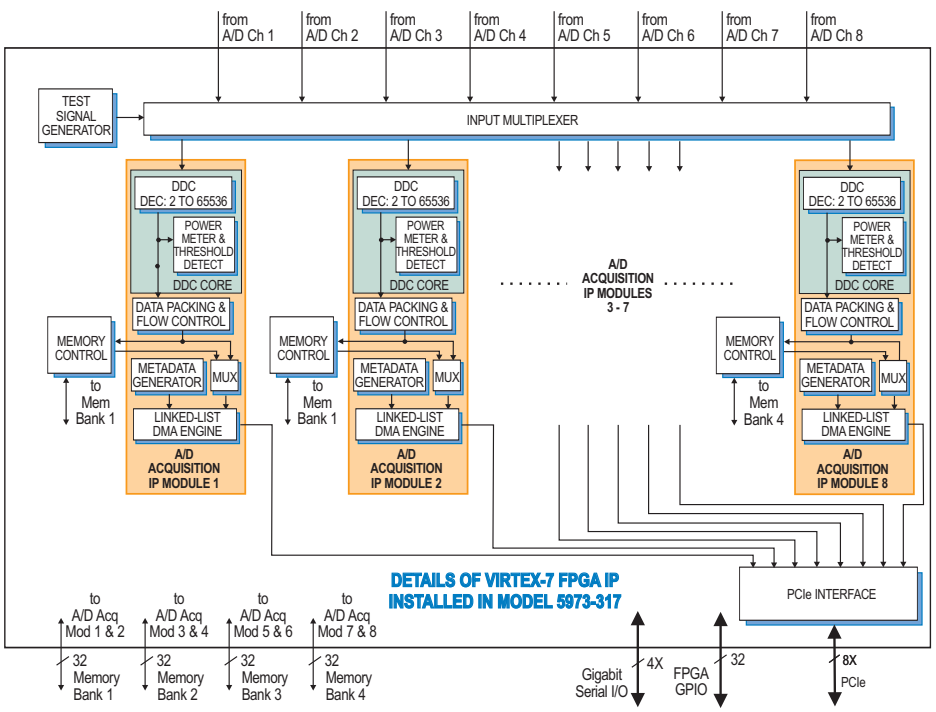
GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Memory Resources

The 5973-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5973-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5973-317	8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX
Options:	
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

FlexorSet Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

Model 5983-317

FlexorSet

JADEFX

NAVIGATOR Design Suite

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB and 5 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

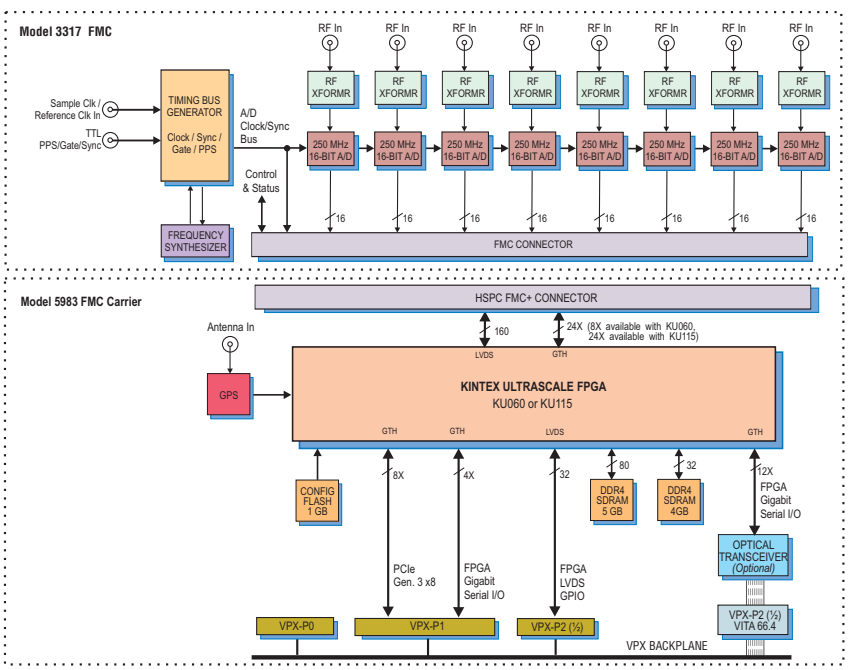
When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

FlexorSet Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

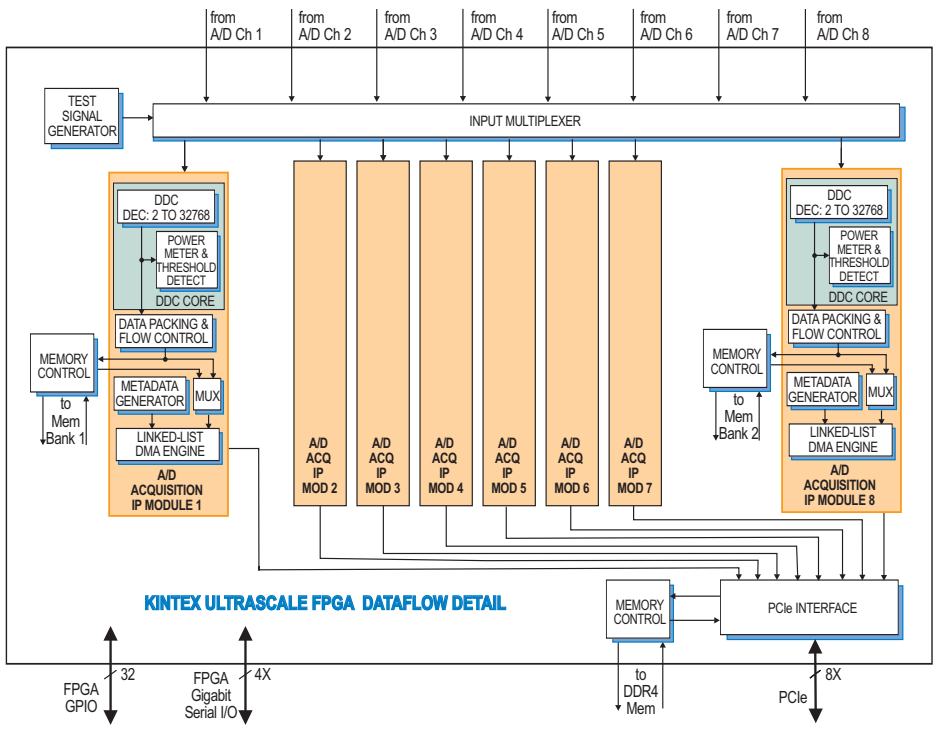
A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Memory Resources

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported. ➤



FlexorSet Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5983-317	8-Channel 250 MHz A/D with DDCs and Kintex Ultra Scale FPGA - 3U VPX
Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

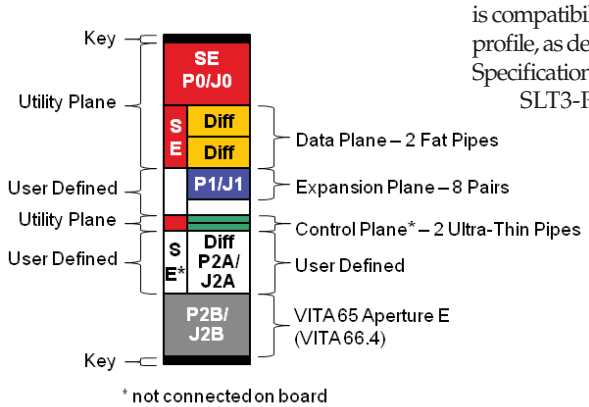
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock



External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU060-2
- **Optional:** Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- **Serial:** 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR4 SDRAM
- **Size:** Two banks, one 4 GB and one 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatibile with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1

New!

FlexorSet Model 7070-317

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

Model 7070-317

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 7070-317 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-317 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-317 to operate as a turnkey solution without the need to develop any FPGA IP.

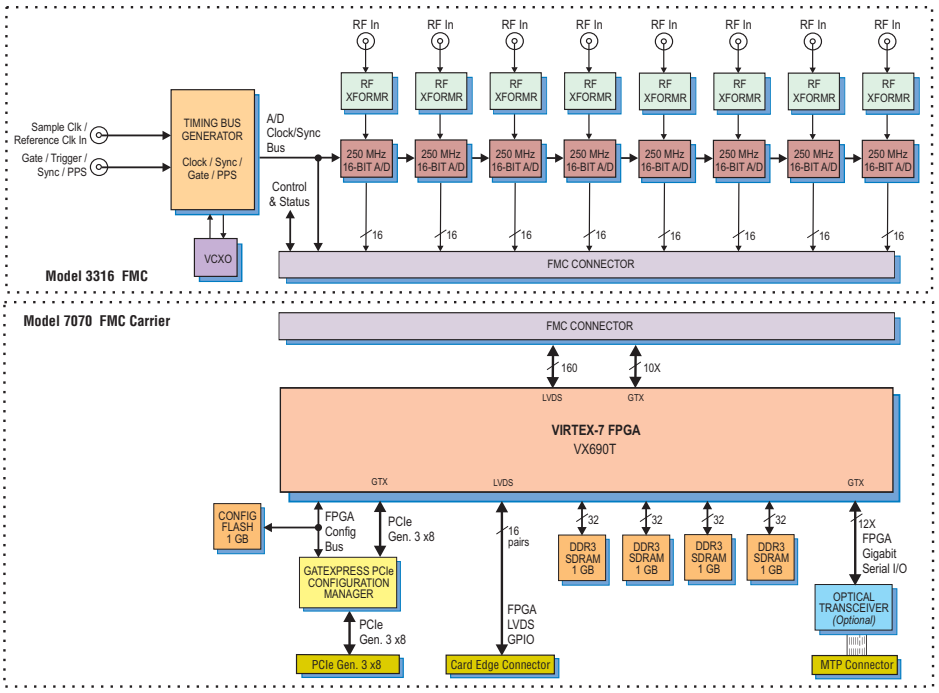
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O. ➤



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8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

➤ Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPoptical connector is presented on the PCIe slot panel.

A/D Acquisition IP Modules

The 7070-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

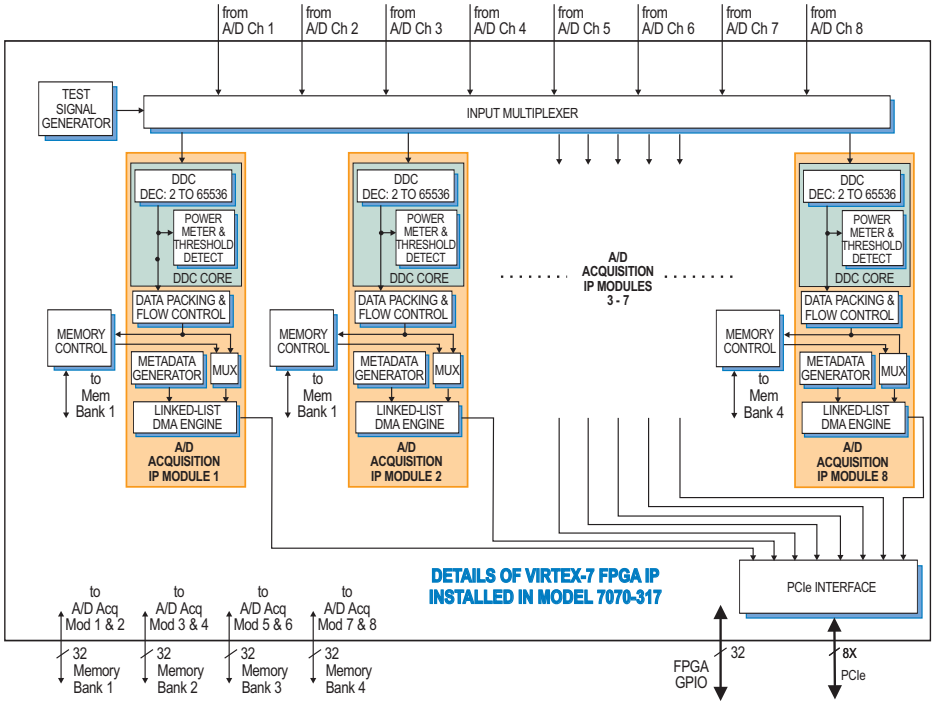
GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 7070-317

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

Memory Resources

The 7070-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 7070-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
7070-317	8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - x8 PCIe
Options:	
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled,

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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New!

Model 3320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

FlexorReadyFlow Board Support PackageGateFlow

Features

- Sold as the:
  - FlexorSet Model 5973-320
  - FlexorSet Model 7070-320
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

The 3320 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-320 3U VPX or the FlexorSet 7070-320 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Performance of the Model 3320

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

A/D and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

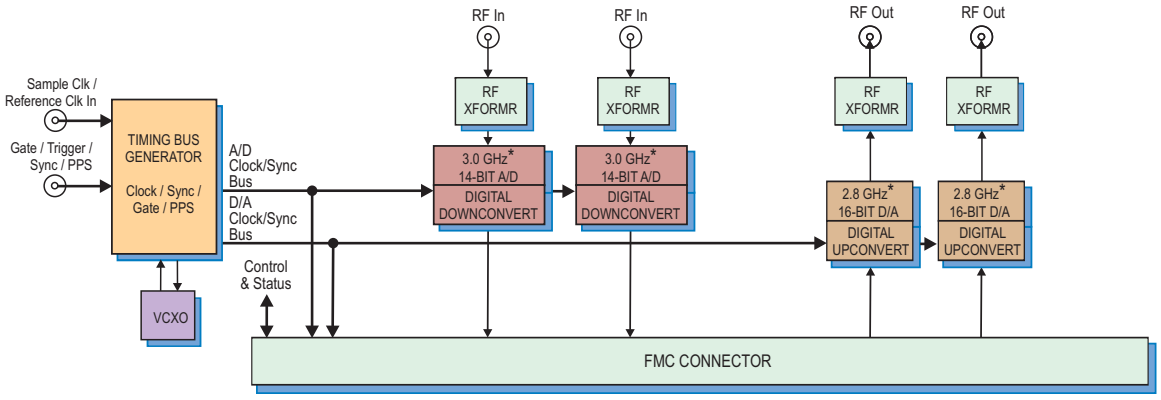
A/D Acquisition IP Modules

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data. ➤



* See last page for configuration profiles

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC39J84 D/As accept two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

D/A Waveform Playback IP Modules

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973 or the 7070, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3320's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/320 or 7070/320 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3320 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier. ➤

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➤ Model 3320 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5973-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

8267	VPX Development System See 8267 Datasheet for Options

7070-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

8266	PC Development System See 8266 Datasheet for Options

Pre-configured Conversion Profiles*

	A/D Converter				D/A Converter		
Converter Sample Rate	Output Resolution	Decimation	Output Data Rate**	Real / Complex	Interpolation	Input Data Rate**	Real / Complex
3.0 GHz	16 bit	4	3.0 GB/sec	complex	n/a	n/a	n/a
2.8 GHz	16 bit	4	2.8 GB/sec	complex	2	5.6 GB/sec	complex
2.8 GHz	16 bit	4	2.8 GB/sec	complex	4	2.8 GB/sec	complex
2.5 GHz	12 bit	bypass	5.0 GB/sec	real	n/a	n/a	n/a
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	4.0 GB/sec	complex
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	2.0 GB/sec	real
1.0 GHz	14 bit	bypass	2.0 GB/sec	real	1	2.0 GB/sec	real

* Other modes can be custom-configured by the user

** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

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New!

FlexorSet Model 5973-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A wth Virtex-7 - 3U VPX

Model 5973-320

FlexorGateXpressGateFlowReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-320 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

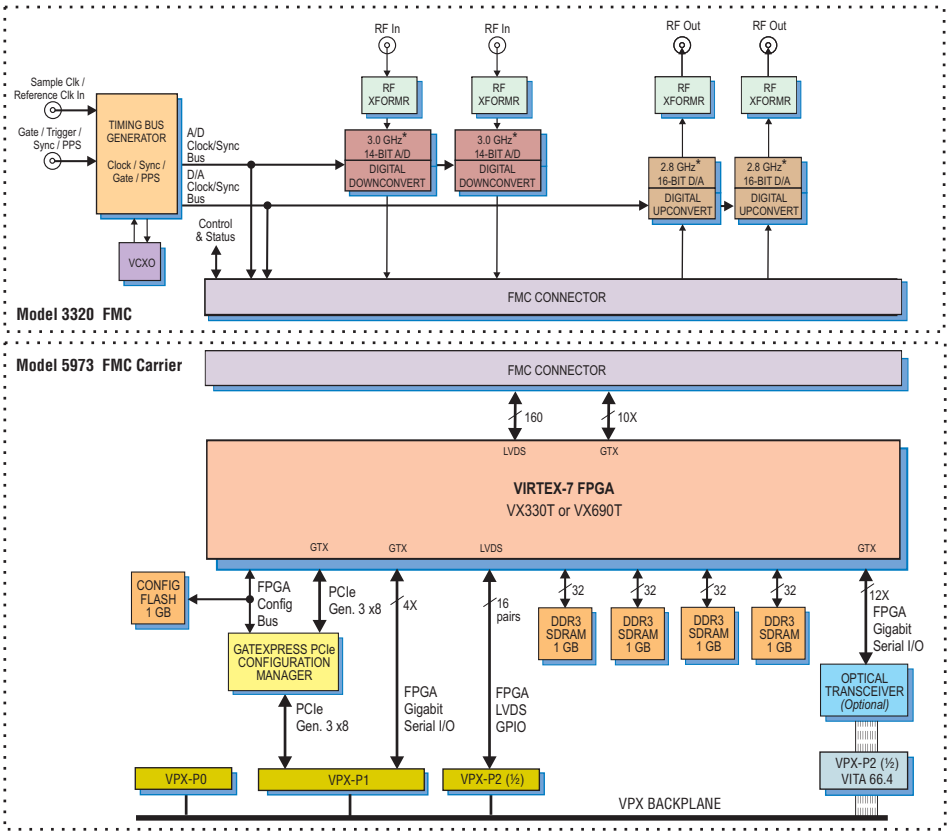
The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. ➤



* See last page for configuration profiles

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A wth Virtex-7 - 3U VPX

A/D Acquisition IP Modules

The 5973-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

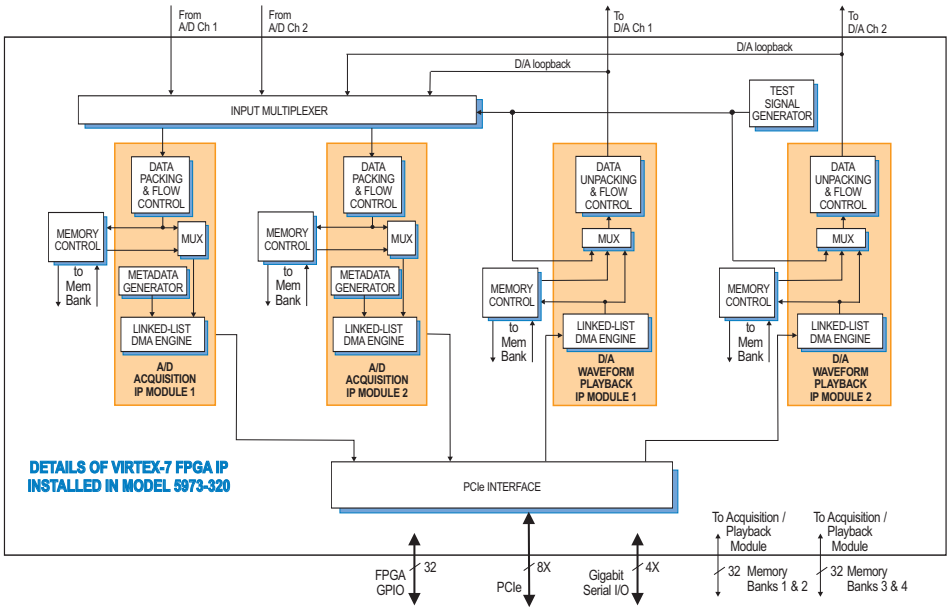
Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

➤ The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 5973-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 5973-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements. ➤

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

FlexorSet Model 5973-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A wth Virtex-7 - 3U VPX

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5973-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

Pre-configured Conversion Profiles*

	A/D Converter				D/A Converter		
Converter Sample Rate	Output Resolution	Decimation	Output Data Rate**	Real / Complex	Interpolation	Input Data Rate**	Real / Complex
3.0 GHz	16 bit	4	3.0 GB/sec	complex	n/a	n/a	n/a
2.8 GHz	16 bit	4	2.8 GB/sec	complex	2	5.6 GB/sec	complex
2.8 GHz	16 bit	4	2.8 GB/sec	complex	4	2.8 GB/sec	complex
2.5 GHz	12 bit	bypass	5.0 GB/sec	real	n/a	n/a	n/a
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	4.0 GB/sec	complex
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	2.0 GB/sec	real
1.0 GHz	14 bit	bypass	2.0 GB/sec	real	1	2.0 GB/sec	real

* Other modes can be custom-configured by the user

** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

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New!

FlexorSet Model 5983-320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

Model 5983-320

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-320 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

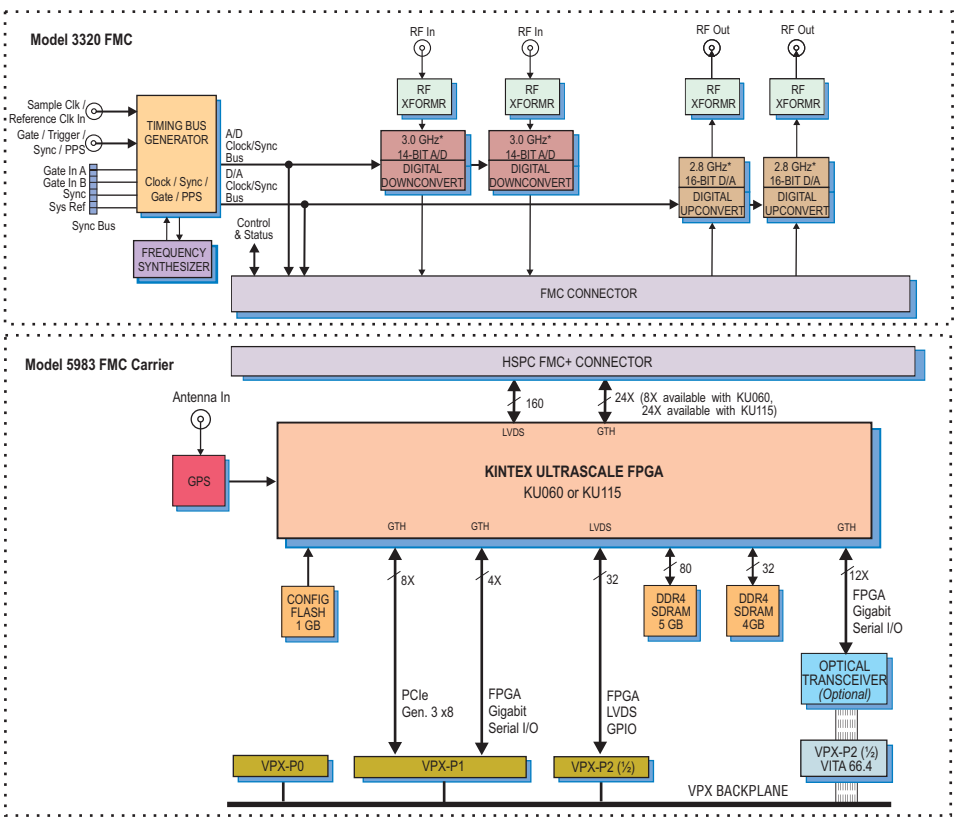
The 5983-320 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP. ➤

Features

- Supports Xilinx Kintex UltraScale FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet
Model 5983-320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 5983-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Modules

The 5983-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-320 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

Memory Resources

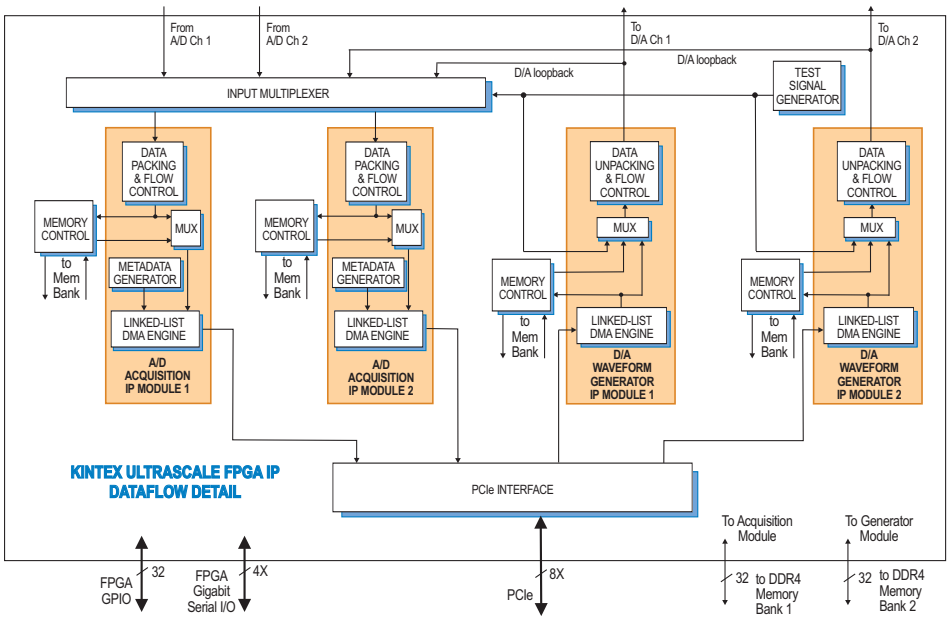
The 5983-320 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the next page for supported modes.➤



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2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

➤ GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See the 3320 preconfigured modes table

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See the 3320 preconfigured modes table

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS ➤

FlexorSet Model 5983-320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ **Field Programmable Gate Array**
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -763: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility:
The Model 5983-320 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

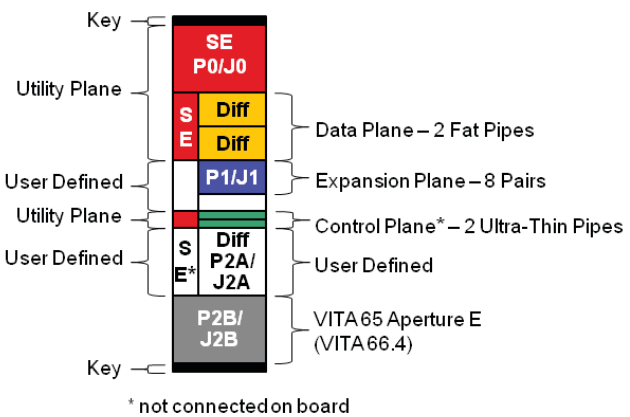
Model	Description
5983-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:

-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options



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New!

FlexorSet Model 7070-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A with Virtex-7 - x8 PCIe

Model 7070-320

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

General Information

Model 7070-320 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

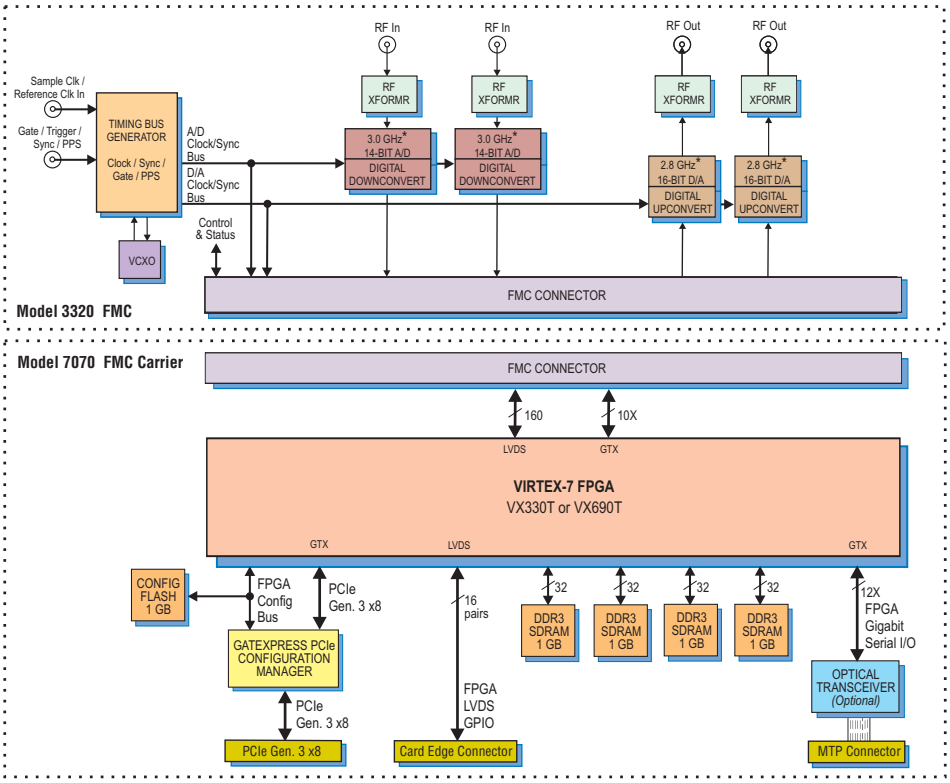
The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. ➤



* See last page for configuration profiles

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 7070-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A with Virtex-7 - x8 PCIe

A/D Acquisition IP Modules

The 7070-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

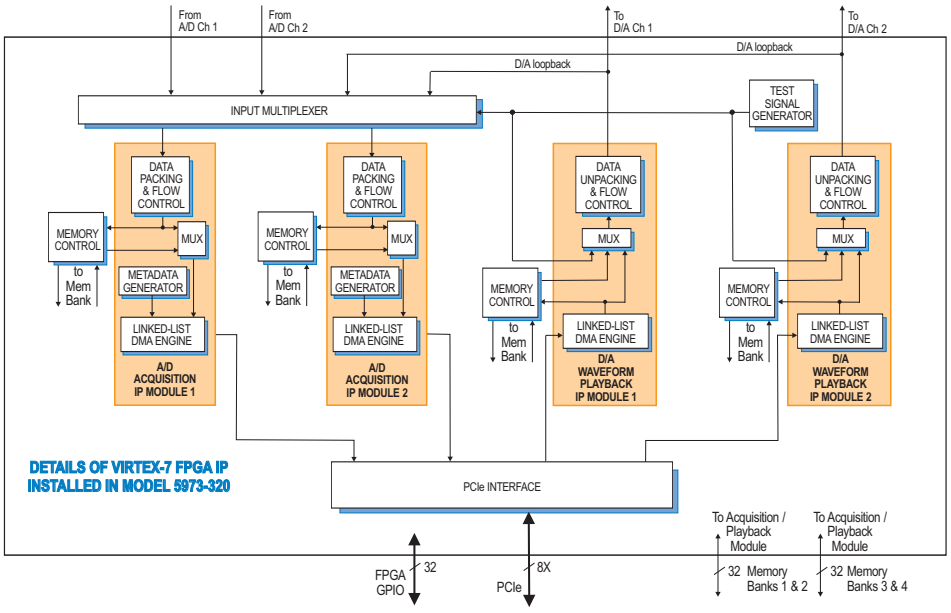
Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. ➤



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➤ The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 7070-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 7070-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements. ➤

FlexorSet Model 7070-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A with Virtex-7 - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pre-configured Conversion Profiles*

	A/D Converter				D/A Converter		
Converter Sample Rate	Output Resolution	Decimation	Output Data Rate**	Real / Complex	Interpolation	Input Data Rate**	Real / Complex
3.0 GHz	16 bit	4	3.0 GB/sec	complex	n/a	n/a	n/a
2.8 GHz	16 bit	4	2.8 GB/sec	complex	2	5.6 GB/sec	complex
2.8 GHz	16 bit	4	2.8 GB/sec	complex	4	2.8 GB/sec	complex
2.5 GHz	12 bit	bypass	5.0 GB/sec	real	n/a	n/a	n/a
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	4.0 GB/sec	complex
2.0 GHz	14 bit	bypass	4.0 GB/sec	real	2	2.0 GB/sec	real
1.0 GHz	14 bit	bypass	2.0 GB/sec	real	1	2.0 GB/sec	real

* Other modes can be custom-configured by the user

** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

Ordering Information

Model	Description
7070-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Model	Description
8266	PC Development System See 8266 Datasheet for Options

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New!

Model 3324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A-FMC

FlexorRT Ready Flow Board Support Package

GateFlow

Features

- Sold as the:
  - FlexorSet Model 5973-324
  - FlexorSet Model 7070-324
- Four 500 MHz, 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz, 16-bit D/As (500 MHz input data rate, 2 GHz output sample rate with interpolation)
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3324 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-324 3U VPX or the FlexorSet 7070-324 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

Performance of the Model 3324

The true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3324 installed on either the 5973 or the 7070 carrier, the board-set features four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

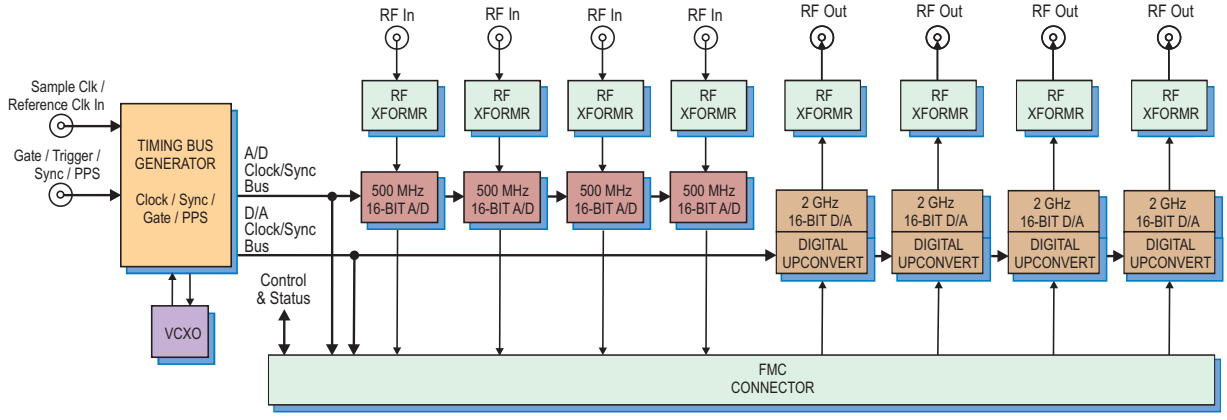
These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

Whith the 5973 or the 7070, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5973-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface
Contact Pentek for availability of rugged and conduction-cooled versions	
8267	VPX Development System See 8267 Datasheet for Options
7070-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T
8266	PC Development System See 8266 Datasheet for Options

➤ Digital Upconverters and D/As

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 1.5 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized and create larger multiboard systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3324's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3324 or 7070/3324 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3324 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3324 and the FMC carrier.

Model 3324 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel connectors

Transformer Type: Coil Craft WBC4-6TLB

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D and D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-pin-count FMC

New!

FlexorSet Model 5973-324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - 3U VPX

Model 5973-324

FlexorSet
GateXpress
GateFlow
ReadyFlow Board Support Package

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input sample rate, 2 GHz output sample rate with interpolation)
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-324 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3324 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

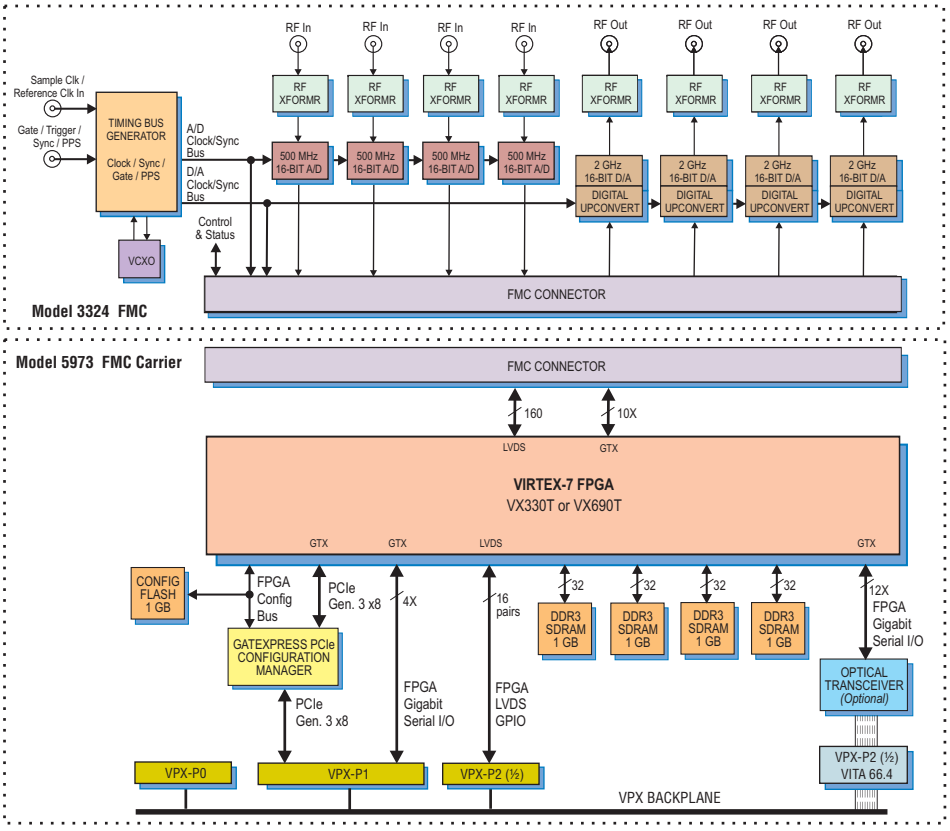
When delivered as an assembled board set, the 5973-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-324 to operate as a turnkey solution without the need to develop any FPGA IP. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 5973-324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - 3U VPX

A/D Acquisition IP Modules

The 5973-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-324 factory-installed functions include four sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

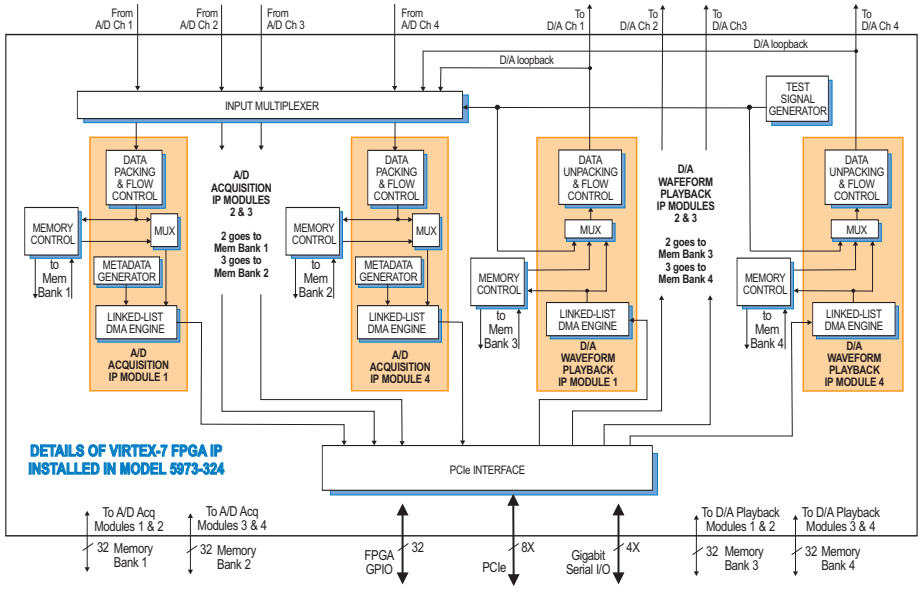
The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 5973-324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - 3U VPX

PCI Express Interface

The Model 5973-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5973-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
5973-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

➤ In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into 500 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full-Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option -110):** VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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www.pentek.com

New!

FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

Model 5983-324

FlexOr

JADEFX

NAVIGATOR Design Suite

Features

- Supports Xilinx Kintex UltraScale FPGA
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input sample rate, 2 GHz output sample rate with interpolation)
- 4 and 5 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Kintex Ultrascale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-324 FlexorSet™ combines the Model 5983 and the Model 3324 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances.

The Flexor Architecture

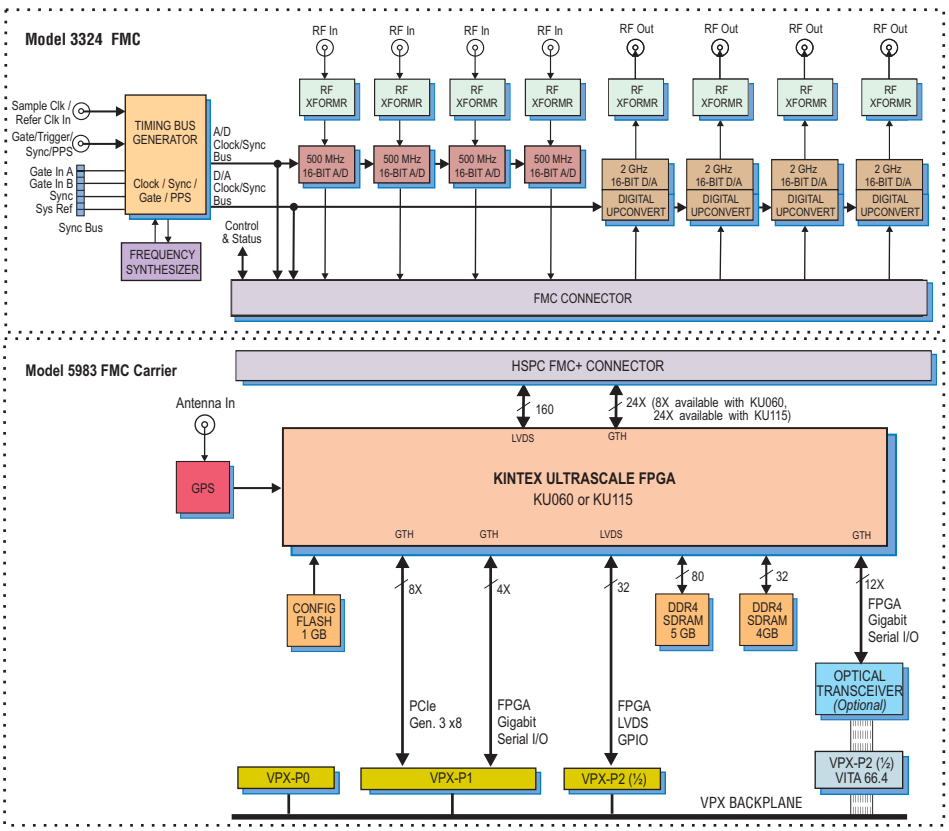
Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-324 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP. ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet
Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 5983-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Recorder IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Recorder IP Modules

The 5983-324 factory-installed functions include four sophisticated D/A Waveform Recorder IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-324 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

Memory Resources

The 5983-324 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

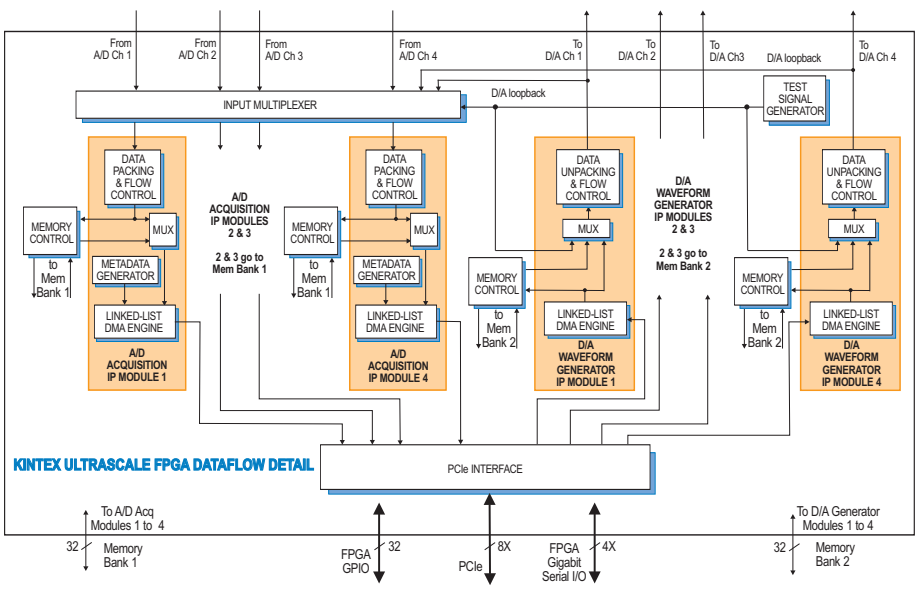
A/D Converter and Downconverter

The front end accepts four analog RF or IF inputs on front-panel connectors with transformer-coupling into Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

Digital Upconverter and D/A

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. ➤



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4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

➤ GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel connectors

Transformer Type: Coil Craft WBC4-6TLB

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks ➤

FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

➤ **External Clock**
Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -763: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-324 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

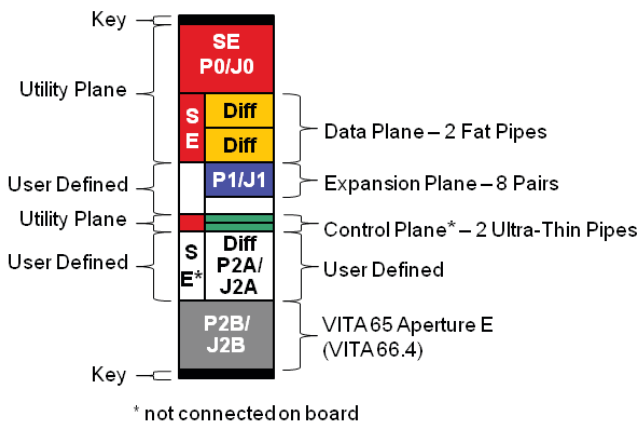
Model	Description
5983-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Kintex UltraScale FPGA - 3U VPX

Options:

-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options



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New!

FlexorSet Model 7070-324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - x8 PCIe

Model 7070-324

FlexorSet
GateXpress
GateFlow
ReadyFlow
Board Support Package

General Information

Model 7070-324 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3324 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

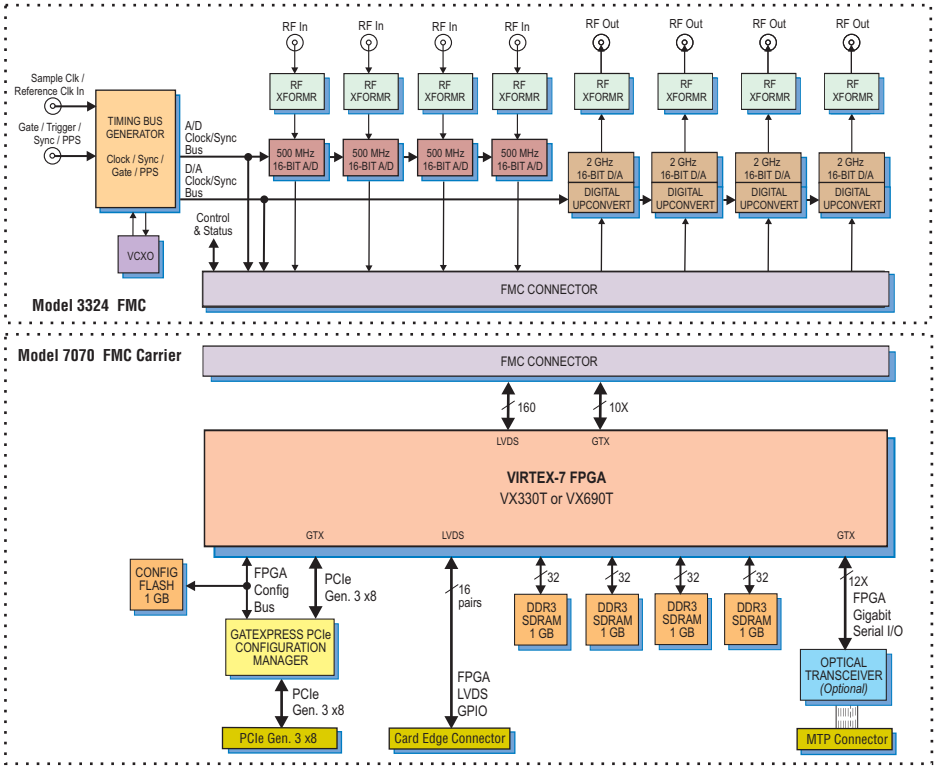
A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their custom ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input data rate, 2 GHz output sample rate with interpolation)
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



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4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - x8 PCIe

A/D Acquisition IP Modules

The 7070-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-324 factory-installed functions include four sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPoptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

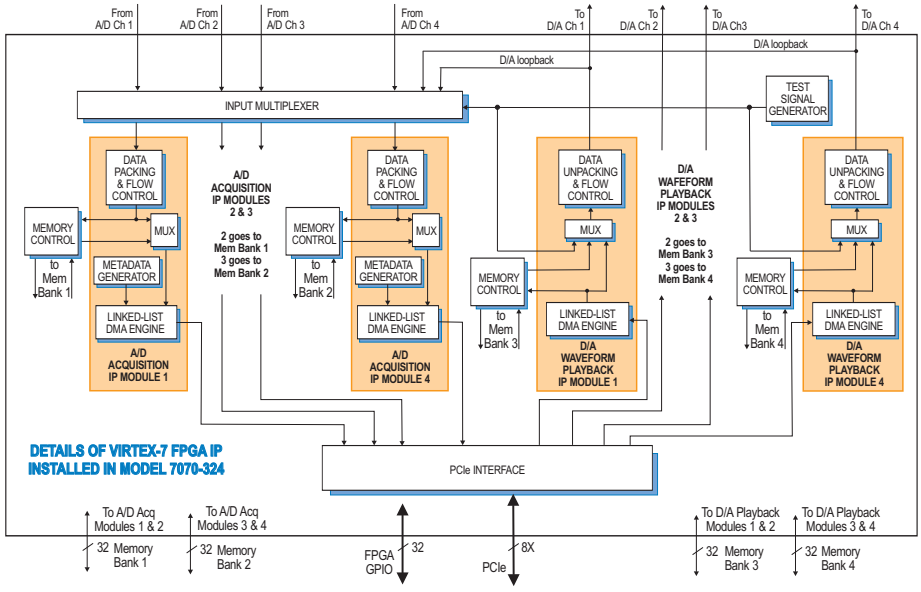
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space ➤



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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
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FlexorSet Model 7070-324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - x8 PCIe

PCI Express Interface

The Model 7070-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 7070-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
7070-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into 500 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full-Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 8266

PC Development System for PCIe Cobalt, Onyx and Flexor Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 4U 19-inch rackmount PC server chassis, 21-inch deep
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box test examples

General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx® and Flexor™ PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

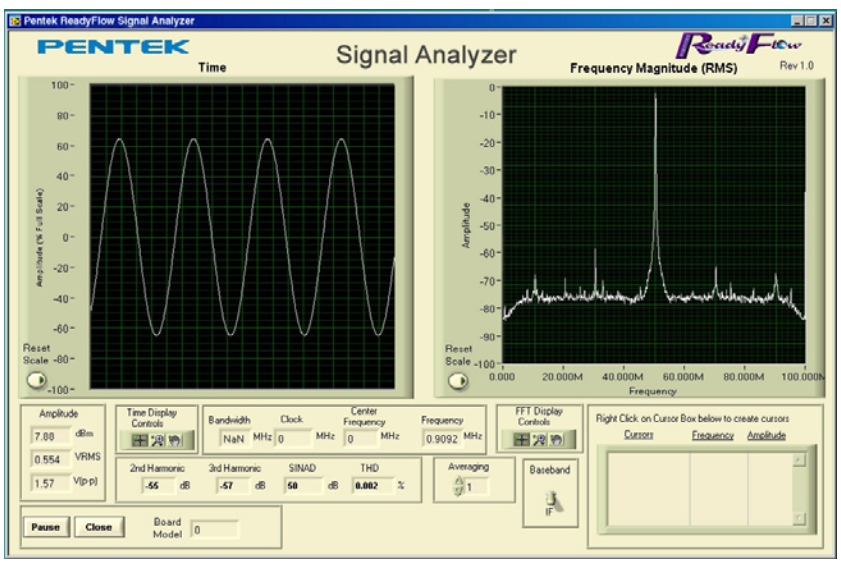
Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19" W x 21" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



Ordering Information

Model	Description
8266	PC Development System for PCIe Cobalt, Onyx and Flexor Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.

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New!

Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

SPARK Development Systems

ReadyFlow Board Support Package

Features

- 9-slot, 4U 19-inch rackmount, 12-inch deep chassis which houses 3U VPX boards
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box ready-to-run examples

Ordering Information

Model	Description
8267	3U VPX Development System for Cobalt, Onyx and Flexor Boards
Options:	
-094	64-bit Linux OS
-095	64-bit Windows 7 OS
-101	Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

General Information

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies gurantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

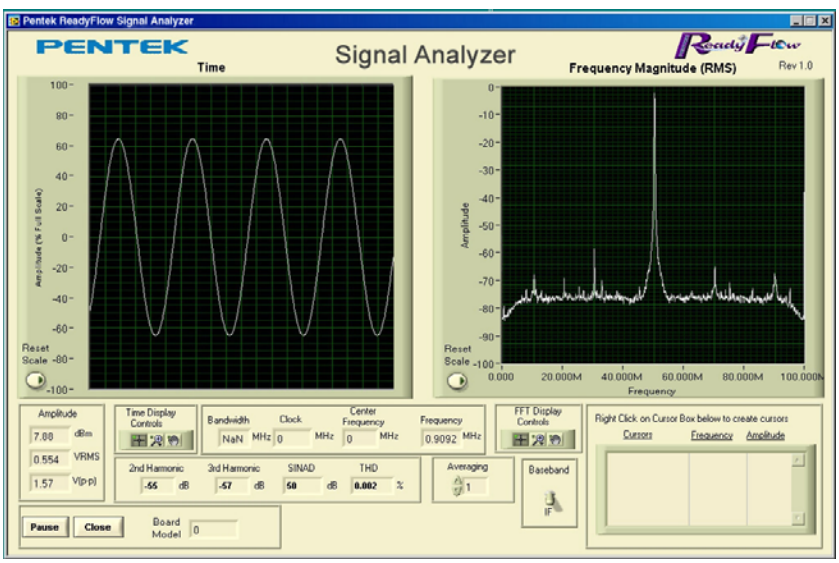
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and extended memory support.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19" W x 12" D x 7" H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.



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New!

Model 3312-990

Reference Design for the Xilinx VC707 Evaluation Kit

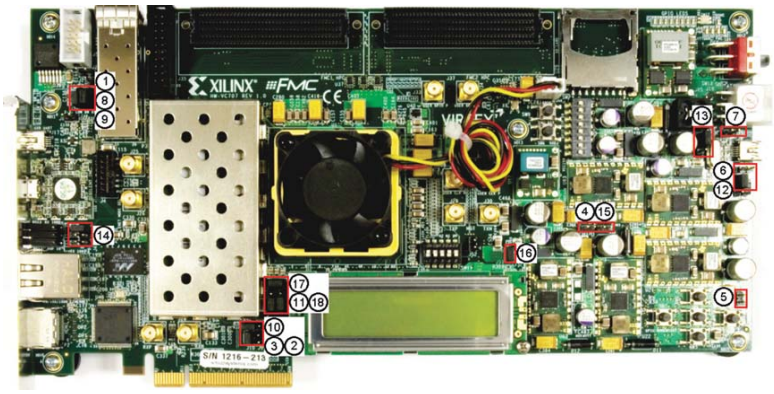
Features

- Supports the Xilinx Virtex-7 FPGA
- Complete development environment with Pentek's reference design
- Supports the Pentek Model 3312 FMC I/O Module

Pentek offers the option -990 reference design with software and IP support for the Pentek Model 3312 when installed on the Xilinx VC707 Evaluation Kit board.

The Virtex®-7 FPGA VC707 Evaluation Kit is a PCIe platform using the Virtex-7 XC7VX485T-2FFG1761C. It includes basic components of hardware, design tools, IP, and preverified reference designs.

When coupled with Pentek's option -990 reference design for the 3312, the user has a complete development environment for custom applications. The industry-standard FPGA Mezzanine Connectors (FMC) are directly compatible with the 3312.



The Xilinx Virtex® -7 FPGA VC707 Evaluation Kit gives designers an easy starting point for evaluating and leveraging devices that deliver breakthrough performance, capacity, and power efficiency. Out of the box, this platform speeds time to market for the full-range of Virtex-7 FPGA-based applications including advanced systems for wired and wireless communications, aerospace and defense. The highly flexible kit combines fully integrated hardware, software, and IP with preverified reference designs that maximize productivity and let designers immediately focus on their unique project requirements.

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

Ordering Information

Model	Description
3312-990	Reference Design for the Xilinx VC707 Evaluation Kit

Please purchase the Xilinx VC707 Evaluation Kit from your Xilinx authorized distributor:
https://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html

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Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We're glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product's environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek's liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at:

Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

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