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TECHNOLOGIES / SOFTWARE

Tools Add Custom IP to RF/IF Signal Recorders' FPGAs

By adding custom IP to the FPGAs in Pentek's Talon recording systems, users can perform real-time, on-the-fly DSP to capture only signals of interest, reducing storage needs and post-processing requirements.

If you design or develop systems for signal-intelligence (SIGINT), communications-intelligence (COMINT), or electronic-intelligence (ELINT) applications, there have likely been times when you needed to insert some custom IP blocks into an COTS RF/IF signal recording system's processing chain. But doing so typically carries the risk of breaking either the existing IP residing on the system's FPGA or the corresponding recording software. Perhaps you've even found yourself resorting to building a recording system from scratch out of desperation, and if so, you probably wouldn't want to again.

Thanks to Pentek's new ArchiTek FPGA Development Suite, you'll never have to. ArchiTek is a comprehensive development environment that lets users add FPGA IP to a selection of Pentek's Talon high-speed, real-time recording systems. If you need threshold detection, spectral filtering, digital down-conversion, signal classification, demodulation, or other DSP techniques, ArchiTek makes adding those sorts of functions a breeze.

ArchiTek harnesses Pentek's Navigator FPGA Development Kit (FDK) and Board Support Package (BSP) to provide a development environment that steps engineers through the process of integrating custom IP into the recorder. Along with the Navigator FDK, ArchiTek provides the foundation and example projects for adding IP to user blocks and creating additional data-path branches from existing data streams. The structured design protects the recorder's standard functionality, reducing development time and risk.

Customers can now add FPGA IP to a recorder for real-time, on-the-fly digital signal processing during the data acquisition process, greatly reducing the time associated with post-processing recorded data. Recording of only critical data also greatly reduces transfer rates, recording capacity requirements, and data offload time.

Using ArchiTek, FPGA developers can add additional recording channels to the system, so users can record both processed and unprocessed data simultaneously. ArchiTek provides extensive documentation and tutorials to assist developers through the customization process, reducing both risk and development time.

Many designers of SIGINT, COMINT, and ELINT systems are either contractors to the mil/aero or defense industries, or working within the military itself, and so their algorithms may be highly classified. The combination of ArchiTek and the Talon recorders enables them to securely insert custom IP into their algorithms.

As an example of a potential use case, many digital communication protocols use spread-spectrum techniques, in which many signal channels are spread across the same frequency span using pseudo-random sequence encoding. Instead of recording the entire frequency span, ArchiTek allows one signal of interest to be extracted using a custom FPGA block so that only that signal is delivered for recording. This can reduce the recording rate and storage capacity by orders of magnitude.

Another SIGINT monitoring application might require signal classification and time stamping of each received transmission. By suitably configuring the classification algorithm within the FPGA using ArchiTek, only the key parameters of each signal need to be recorded instead of the signals themselves, thus dramatically extending the useful mission time. This strategy of real-time processing at the front end also reduces or eliminates post-processing tasks.

The ArchiTek FPGA Development Suite (Model 4818) is currently available for select models of Talon recorders. Contact Pentek for pricing and availability information.

Pentek, www.pentek.com

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